Cat. No. W405-E1-16

SYSMAC CS Series

CS1D-CPU□□HA/H CPU Units
CS1D-CPU□□SA/S CPU Units
CS1D-DPL01/02D Duplex Unit
CS1D-PA/PD□□□ Power Supply Unit

CS1D Duplex System

OPERATION MANUAL

OMRON

NOTE

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CS1D Duplex System
Operation Manual

Revised September 2024

Notice:

OMRON products are manufactured for use according to proper procedures by a qualified operator and only for the purposes described in this manual.

The following conventions are used to indicate and classify precautions in this manual. Always heed the information provided with them. Failure to heed precautions can result in injury to people or damage to property.

⚠ DANGER Indicates an imminently hazardous situation which, if not avoided, will result in death or serious injury. Additionally, there may be severe property damage.

⚠ WARNING Indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury. Additionally, there may be severe property damage.

⚠ Caution Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury, or property damage.

OMRON Product References

All OMRON products are capitalized in this manual. The word “Unit” is also capitalized when it refers to an OMRON product, regardless of whether or not it appears in the proper name of the product.

The abbreviation “Ch,” which appears in some displays and on some OMRON products, often means “word” and is abbreviated “Wd” in documentation in this sense.

The abbreviation “PLC” means Programmable Controller. “PC” is used, however, in some Programming Device displays to mean Programmable Controller.

Visual Aids

The following headings appear in the left column of the manual to help you locate different types of information.

Note Indicates information of particular interest for efficient and convenient operation of the product.

1,2,3... 1. Indicates lists of one sort or another, such as procedures, checklists, etc.

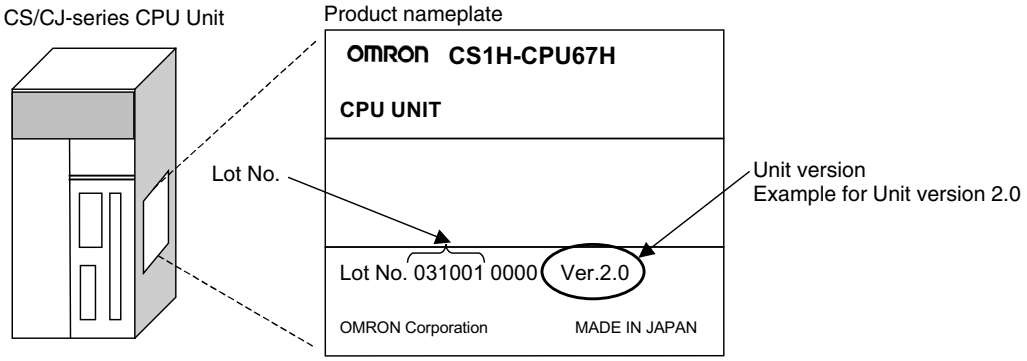
Unit Versions of CS/CJ-series CPU Units

Unit Versions

A “unit version” has been introduced to manage CPU Units in the CS/CJ Series according to differences in functionality accompanying Unit upgrades. This applies to the CS1-H, CJ1-H, CJ1M, and CS1D CPU Units.

Notation of Unit Versions on Products

The unit version is given to the right of the lot number on the nameplate of the products for which unit versions are being managed, as shown below.



- CS1-H, CJ1-H, and CJ1M CPU Units (except for low-end models) manufactured on or before November 4, 2003 do not have a unit version given on the CPU Unit (i.e., the location for the unit version shown above is blank).
- The unit version of the CS1-H, CJ1-H, CJ1M and CS1D-CPU□□S CPU Units begins at version 2.0.
- The unit version of the CS1D-CPU□□H begins at version 1.1.
- The unit version of the CS1D-CPU□□HA/SA begins at version 4.0.
- CPU Units for which a unit version is not given are called *Pre-Ver. □.□ CPU Units, such as Pre-Ver. 2.0 CPU Units* and *Pre-Ver. 1.1 CPU Units.*

Confirming Unit Versions with Support Software

CX-Programmer version 4.0 or later can be used to confirm the unit version using one of the following two methods.

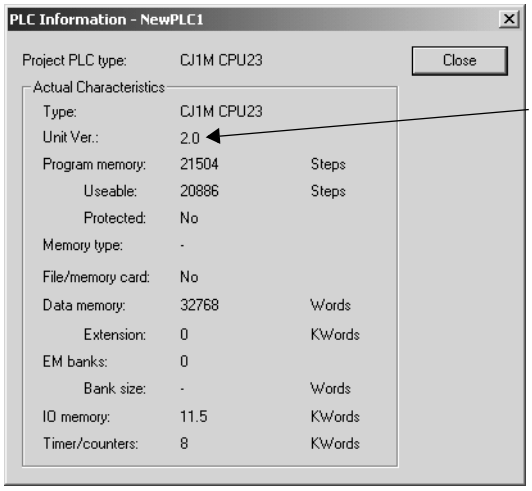
- Using the ***PLC Information***
- Using the ***Unit Manufacturing Information*** (This method can be used for Special I/O Units and CPU Bus Units as well.)

Note CX-Programmer version 3.3 or lower cannot be used to confirm unit versions.

PLC Information

- If you know the device type and CPU type, select them in the *Change PLC* Dialog Box, go online, and select ***PLC - Edit - Information*** from the menus.
- If you don’t know the device type and CPU type, but are connected directly to the CPU Unit on a serial line, select ***PLC - Auto Online*** to go online, and then select ***PLC - Edit - Information*** from the menus.

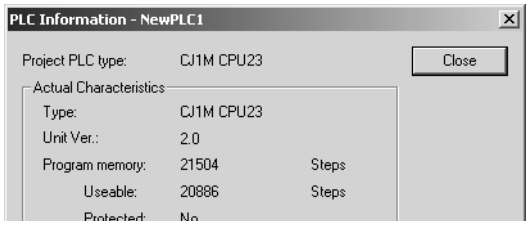
In either case, the following *PLC Information* Dialog Box will be displayed.



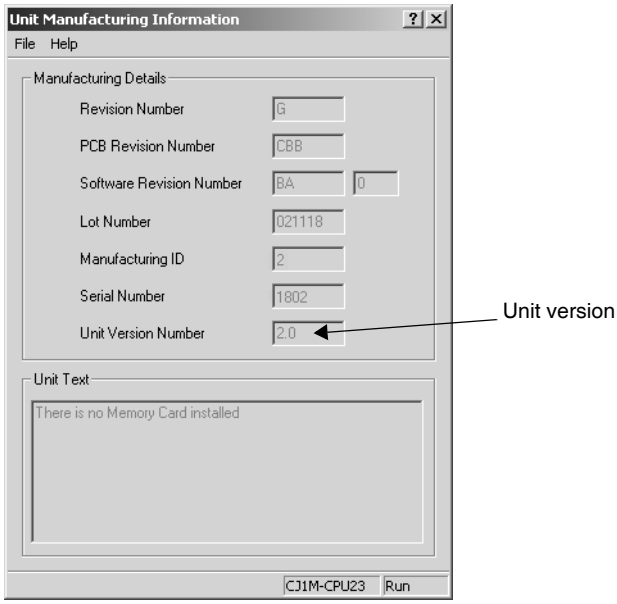
Use the above display to confirm the unit version of the CPU Unit.

Unit Manufacturing Information

In the *IO Table* Window, right-click and select ***Unit Manufacturing information - CPU Unit.***



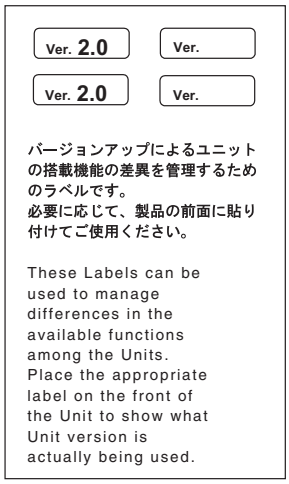
The following *Unit Manufacturing information* Dialog Box will be displayed.



Use the above display to confirm the unit version of the CPU Unit connected online.

Using the Unit Version Labels

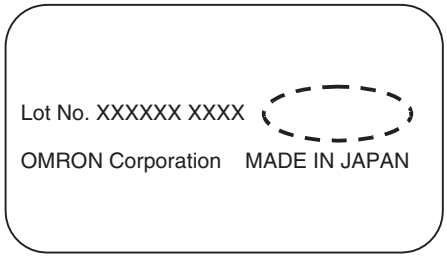
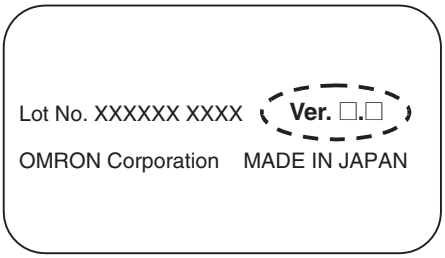
The following unit version labels are provided with the CPU Unit.



These labels can be attached to the front of previous CPU Units to differentiate between CPU Units of different unit versions.

Unit Version Notation

In this manual, the unit version of a CPU Unit is given as shown in the following table.

Product nameplate Meaning	CPU Units on which no unit version is given 	Units on which a version is given (Ver. □.□) 
Designating individual CPU Units (e.g., the CS1H-CPU67H)	Pre-Ver. 2.0 CS1-H CPU Units	CS1H-CPU67H CPU Unit Ver. □.□
Designating groups of CPU Units (e.g., the CS1-H CPU Units)	Pre-Ver. 2.0 CS1-H CPU Units	CS1-H CPU Units Ver. □.□
Designating an entire series of CPU Units (e.g., the CS-series CPU Units)	Pre-Ver. 2.0 CS-series CPU Units	CS-series CPU Units Ver. □.□

System Configuration Support by Unit Version

System configuration	CS1D-CPU□□HA/H/P						CS1D-CPU□□SA/S		
	Pre-Ver. 1.1	Ver. 1.1	Ver. 1.2	Ver. 1.3	Ver. 1.4	Ver. 4.0	Ver. 2.0	Ver. 2.1	Ver. 4.0
Duplex CPU, Dual I/O Expansion System	---	---	---	OK	OK	OK	---	---	---
Duplex CPU, Single I/O Expansion System	OK	OK	OK	OK	OK	OK	---	---	---
Single CPU System	---	---	---	---	---	---	OK	OK	OK

Note 1. OK: Supported, ---: Not supported

2. Only CS1D-CPU□□H/P CPU Units with unit version 1.3 or later support the Duplex CPU, Dual I/O Expansion System. If a Dual I/O Expansion System is connected to a CPU Unit with an earlier unit version, an I/O bus error will occur and the PLC will not operate.

Function Support by Unit Version

CS1D CPU Units

Function		CS1D-CPU□□H/P				CS1D-CPU□□HA		CS1D-CPU□□S	CS1D-CPU□□SA
		Duplex-CPU Systems						Single CPU Systems	
		Pre-Ver. 1.1	Ver. 1.1	Ver. 1.2	Ver. 1.3 to 1.4	Ver. 4.0		Ver. 2.0 to 2.1	Ver.4.0
						With Duplex CPU Compatible Setting	Without Duplex CPU Compatible Setting		
Functions unique to CS1D CPU Units	Duplex CPU Units	OK	OK	OK	OK	OK	OK	---	---
	Online Unit Replacement using a Programming Device	OK	OK	OK	OK	OK	OK	OK	OK
	Duplex Power Supply Units	OK	OK	OK	OK	OK	OK	OK	OK
	Duplex Controller Link Units	OK	OK	OK	OK	OK	OK	OK	OK
	Duplex Ethernet Units	---	OK	OK	OK	OK	OK	OK	OK
	Unit Removal without a Programming Device	---	---	OK	OK	OK	OK	---	---
	Removal/Addition of Units without a Programming Device (See note 2.)	---	---	---	OK (See note 2.)	OK (See note 2.)	OK (See note 2.)	---	---
	Duplex Connecting Cables	---	---	---	OK (See notes 4.)	OK (See notes 4.)	OK (See notes 4.)	---	---
	Online Addition of Units and Backplanes	---	---	---	OK (See notes 3 and 4.)	OK (See notes 3 and 4.)	OK (See notes 3 and 4.)	---	---
	Online Addition of Duplex Unit	---	---	---	OK (See notes 4.)	OK (See notes 4.)	OK (See notes 4.)	---	---
Downloading Individual Tasks		---	---	---	---	---	---	OK	OK
Improved Read Protection Using Passwords		---	---	---	---	---	---	OK	OK
Write Protection from FINS Commands Sent to CPU Units via Networks		---	---	---	---	---	---	OK	OK
Online Network Connections without I/O Tables		---	---	---	---	---	---	OK	OK
Communications through a Maximum of 8 Network Levels		---	---	---	---	---	---	OK	OK
Connecting Online to PLCs via NS-series PTs		---	---	---	---	---	---	OK	OK

Function		CS1D-CPU□□H/P				CS1D-CPU□□HA		CS1D-CPU□□S	CS1D-CPU□□SA
		Duplex-CPU Systems						Single CPU Systems	
		Pre-Ver. 1.1	Ver. 1.1	Ver. 1.2	Ver. 1.3 to 1.4	Ver. 4.0		Ver. 2.0 to 2.1	Ver.4.0
						With Duplex CPU Compatible Setting	Without Duplex CPU Compatible Setting		
Setting First Slot Words		---	---	---	---	---	---	OK for up to 64 groups	OK for up to 64 groups
Automatic Transfers at Power ON without a Parameter File		---	---	---	---	---	---	OK	OK
Operation Start/End Times		---	OK	OK	OK	OK	OK	OK	OK
Automatic Allocation of Communications Ports		---	---	---	OK	OK	OK	OK	OK
New Application Instructions	MILH, MILR, MILC	---	---	---	---	---	---	OK	OK
	=DT, <>DT, <DT, <=DT, >DT, >=DT	---	---	---	---	---	---	OK	OK
	BCMP2	---	---	---	---	---	---	OK	OK
	GRY	---	---	---	---	---	---	OK	OK
	TPO	---	---	---	---	---	---	OK	OK
	DSW, TKY, HKY, MTR, 7SEG	---	---	---	---	---	---	OK	OK
	EXPLT, EGATR, ESATR, ECHRD, ECHWR	---	---	---	---	---	---	OK	OK
	Reading/Writing CPU Bus Units with IORD/IOWR Instructions	---	---	---	---	---	---	OK	OK

Note

1. OK: Supported, ---: Not supported
2. Supported only by CPU Duplex Dual Expansion Systems.
   If the *Removal/Addition of Units without a Programming Device* function is selected in a Duplex CPU, Single I/O Expansion System, the function will operate as the earlier *Unit Removal without a Programming Device* function.
3. Basic I/O Units and Special I/O Units can be added for the *Online Addition of Units and Backplanes* function. CPU Units cannot be added.
4. Expansion Backplanes cannot be added with a Duplex CPU, Single I/O Expansion System.
5. Supported only by CPU Duplex Dual Expansion Systems.

Function	CS1D-CPU□□H/P		CS1D-CPU□□HA	CS1D-CPU□□S		CS1D-CPU□□SA
	Duplex-CPU Systems			Single CPU Systems		
	Pre-Ver. 1.1 to 1.3	Ver. 1.4	Ver. 4.0	Ver. 2.0	Ver. 2.1	Ver.4.0
Read protection using extended passwords	---	OK	OK	---	OK	OK
Disabling password input after five consecutive incorrect passwords	---	OK	OK	---	OK	OK
Auxiliary Area notification of production lot number	---	OK	OK	---	OK	OK
Function Block (FB) Function	---	---	OK	---	---	OK

Function		CS1D-CPU□□H/P		CS1D-CPU□□HA	CS1D-CPU□□S		CS1D-CPU□□SA
		Duplex-CPU Systems			Single CPU Systems		
		Pre-Ver. 1.1 to 1.3	Ver. 1.4	Ver. 4.0	Ver. 2.0	Ver. 2.1	Ver.4.0
PLC Setup: Communications Instruction Setting within FB: Retransmission Cycle Response Monitor Time: Communications Instruction within FB DeviceNet Communications Instruction within FB		---	---	OK	---	---	OK
Serial Gateway Function (Conversion from FINS to CompoWay/F in the Built-in Serial Port)		---	---	---	---	---	---
Comment Memory (in the Built-in Flash Memory) Function		---	---	OK	---	---	OK
Extension of Simple Backup Targets	The following files in the comment memory are also the target for simple backup. • Symbol table file • Comment file • Program index file	---	---	OK	---	---	OK
TXDU, RXDU (Communications are enabled in the no-protocol mode in serial communications unit with unit version 1.2 or later)		---	---	---	---	---	OK
GETID (Special Instructions for Function Blocks)		---	---	OK	---	---	OK
Instruction Function Addition	TXD, RXD Instruction (Communications are enabled in the no-protocol mode in serial communications board with unit version 1.2 or later)	---	---	---	---	---	OK
Free Running Timer Function (System Timer after Power is Turned ON)		---	---	OK	---	---	OK
Use of Newly Added Special Instructions	Numerical value → ASCII conversion instruction, ASCII → numerical value conversion instruction (NUM4, NUM8, NUM16, STR4, STR8, STR16)	---	---	OK	---	---	OK
	Text file write instruction (TWRIT)	---	---	OK	---	---	OK
Improved Function Block (FB) Function	Function block (FB) online editing	---	---	OK	---	---	OK
	Support for in-out variable (array specification is possible for in-out variable)	---	---	OK	---	---	OK
	STRING data (type) and string processing function is supported in Structured Text	---	---	OK	---	---	OK
Structured Text can be used in a task program		---	---	OK	---	---	OK
SFC language can be used in a task program		---	---	OK	---	---	OK

Unit Versions and Programming Devices

The following tables show the relationship between unit versions and CX-Programmer versions.

Unit Versions and Programming Devices

OK: Available, ---: Unavailable

CPU Unit	Functions		CX-Programmer						Programming Console
			Ver. 3.3 or lower	Ver. 4.0 to 6.0	Ver. 6.1	Ver. 7.0 to 8.0	Ver. 9.6	Ver. 9.7	
CS1D CPU Units for Single CPU Systems, Unit Ver. 2.0	Functions upgraded in Unit Ver. 2.0	Using new functions	---	OK	OK	OK	OK	OK	OK
		Not using new functions					OK	OK	
CS1D Simplex CPU Unit Ver. 2.1	Functions upgraded in Unit Ver. 2.1	Using new functions	---	---	---	---	OK	OK	---
		Not using new functions	---	OK	OK	OK	OK	OK	OK
CS1D CPU Units for Duplex CPU Systems, Unit Ver.1.1	Functions upgraded in Unit Ver. 1.1	Using new functions	---	OK	OK	OK	OK	OK	OK
		Not using new functions	OK	OK	OK	OK	OK	OK	
CS1D Duplex CPU Unit Ver. 1.2	Functions upgraded in Unit Ver. 1.2	Using new functions	---	---	OK	OK	OK	OK	
		Not using new functions	OK	OK	OK	OK	OK	OK	
CS1D Duplex CPU Unit Ver. 1.3	Functions upgraded in Unit Ver. 1.3	Using new functions	---	---	---	OK (See note 1.)	OK	OK	OK (See note 2.)
		Not using new functions	OK	OK	OK	OK	OK	OK	
CS1D Duplex CPU Unit Ver. 1.4	Functions upgraded in Unit Ver. 1.4	Using new functions	---	---	---	---	OK	OK	---
		Not using new functions	OK	OK	OK	OK	OK	OK	OK (See note 2.)
CS1D Simplex CPU Unit Ver. 4.0	Functions upgraded in Unit Ver. 4.0	Using new functions	---	---	---	---	---	OK	---
		Not using new functions	---	OK	OK	OK	OK	OK	OK
CS1D Duplex CPU Unit Ver. 4.0	Functions upgraded in Unit Ver. 4.0	Using new functions	---	---	---	---	---	OK	---
		Not using new functions	---	---	---	---	---	OK	OK (See note 2.)
	When changed to CS1D-CPU □□H by Duplex CPU compatible setting	This is a CS1D CPU Unit for Duplex CPU Systems with unit version 1.4, and the relationship with the Programming Device is same as unit version 1.1 to 1.4.							

Note 1. CX-Programmer Ver. 7.0 can be used by expanding the Unit's functions using the auto update function.

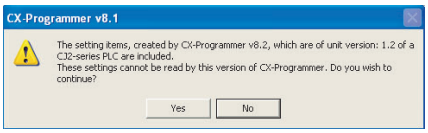
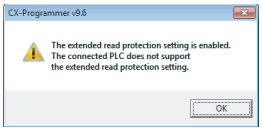
2. Online function addition of the Unit is not supported.

Device Type Setting

The unit version does not affect the setting made for the device type on the CX-Programmer. Select the device type as shown in the following table regardless of the unit version of the CPU Unit.

Series	CPU Unit group	CPU Unit model	Device type setting on CX-Programmer Ver. 4.0 or higher
CS Series	CS1-H CPU Units	CS1G-CPU□□H	CS1G-H
		CS1H-CPU□□H	CS1H-H
	CS1D CPU Units for Duplex CPU Systems	CS1D-CPU□□H	CS1D-H (or CS1H-H)
		CS1D-CPU□□HA	CS1D-H
	CS1D CPU Units for Single CPU Systems	CS1D-CPU□□S	CS1D-S
		CS1D-CPU□□SA	CS1D-S
CJ Series	CJ1-H CPU Units	CJ1G-CPU□□H	CJ1G-H
		CJ1H-CPU□□H	CJ1H-H
	CJ1M CPU Units	CJ1M-CPU□□	CJ1M

Troubleshooting Problems with Unit Versions on the CX-Programmer

Problem	Cause	Solution
 After the above message is displayed, a compiling error will be displayed on the *Compile* Tab Page in the Output Window.	An attempt was made using CX-Programmer version 4.0 or higher to download a program containing instructions supported only by CPU Units Ver. 2.0 or later to a Pre-Ver. 2.0 CPU Units.	Check the program or change the CPU Unit being downloaded to a CPU Unit Ver. 2.0 or later.
	An attempt was made using CX-Programmer version 4.0 or higher to download a PLC Setup containing settings supported only by CPU Units Ver. 2.0 or later (i.e., not set to their default values) to a Pre-Ver. 2.0 CPU Units.	Check the settings in the PLC Setup or change the CPU Unit being downloaded to a CPU Unit Ver. 2.0 or later.
"????" is displayed in a program transferred from the PLC to the CX-Programmer.	CX-Programmer version 3.3 or lower was used to upload a program containing instructions supported only by CPU Units Ver. 2.0 or later from a CPU Unit Ver. 2.0 or later.	The new instructions cannot be uploaded using CX-Programmer version 3.3 or lower. Use CX-Programmer version 4.0 or higher.
 The above error is displayed when a project file is read.	An attempt was made to read a project file for an unsupported unit version.	Click the **Yes** Button to initialize unsupported settings and read the file. Click the **No** Button to cancel reading the project file.
 The above warning is displayed when going online.	An attempt was made to go online with an earlier version of a CPU Unit for a project file that contains an extended read protection setting that is supported only by a newer version of the CPU Unit.	Change the protection setting in the PLC Properties Dialog Box. Or, replace the CPU Unit with which you need to go online with a higher version of CPU Unit.

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About this Manual:

This manual describes the installation and operation of the CS1D Duplex Programmable Controllers (PLCs) and includes the sections described below. The CS Series and CJ Series are subdivided as shown in the following table.

Unit	CS Series	CJ Series
CPU Units	CS1-H CPU Units: CS1H-CPU□□H CS1G-CPU□□H	CJ1-H CPU Units: CJ1H-CPU□□H CJ1G-CPU□□H CJ1-H Loop-control CPU Units: CJ1G-CPU□□H
	CS1 CPU Units: CS1H-CPU□□-EV1 CS1G-CPU□□-EV1	CJ1 CPU Units: CJ1G-CPU□□-EV1
	CS1D CPU Units: CS1D-CPU□□H CS1D-CPU□□S CS1D Process-control CPU Units: CS1D-CPU□□P	CJ1M CPU Units: CJ1M-CPU□□
Basic I/O Units	CS-series Basic I/O Units	CJ-series Basic I/O Units
Special I/O Units	CS-series Special I/O Units	CJ-series Special I/O Units
CPU Bus Units	CS-series CPU Bus Units	CJ-series CPU Bus Units
Power Supply Units	CS-series Power Supply Units CS1D Power Supply Units	CJ-series Power Supply Units

Please read this manual and all related manuals listed in the table on the next page and be sure you understand information provided before attempting to install or use CS1D-CPU□□HA/SA/H/S CPU Units in a PLC System.

Process-control CPU Units refer to CPU Units with the models CS1D-CPU□□P. Each Process-control CPU Unit consists of a CS1D-CPU□□H CS1D CPU Unit and a CS1D-LCB05D Loop Control Board as a set.

Precautions provides general precautions for using the CS1D Programmable Controllers (PLCs) and related devices, including the CS1D-CPU□□H CPU Units for Duplex CPU Systems, CS1D-CPU□□S CPU Units for Single CPU Systems, CS1D-DPL01 Duplex Unit, and CS1D-PA/PD□□□ Power Supply Unit.

Section 1 introduces the special features and functions of the CS1D Duplex PLCs and describes the differences between these PLCs and other PLCs.

Section 2 provides the specifications, defines the nomenclature, and describes the functions of CS1D PLCs.

Section 3 describes the basic operation of a Duplex System.

Section 4 outlines the steps required to assemble and operate a CS1D Duplex PLC system.

Section 5 describes how to install a PLC System, including mounting the various Units and wiring the System. Be sure to follow the instructions carefully. Improper installation can cause the PLC to malfunction, resulting in very dangerous situations.

Section 6 describes the settings in the PLC Setup and how they are used to control CPU Unit operation.

Section 7 describes I/O allocations to Basic I/O Units, Special I/O Units, and CPU Bus Units, and data exchange with Units.

Section 8 describes the structure and functions of the I/O Memory Areas and Parameter Areas.

Section 9 describes the internal operation of the CPU Unit and the cycle used to perform internal processing.

Section 10 provides information on hardware and software errors that occur during PLC operation.

Section 11 provides inspection and maintenance information.

The Appendices provide Unit specifications, Auxiliary Area words and bits, a memory map of internal addresses, and PLC Setup coding sheets, RS-232C port connection information, and precautions when upgrading a system to duplex operation with CS1D PLCs

About this Manual, Continued

Name	Cat. No.	Contents
SYSMAC CS Series CS1D-CPU□□HA/H CPU Units CS1D-CPU□□SA/S CPU Units CS1D-DPL01/02D Duplex Unit CS1D-PA/PD□□□ Power Supply Unit Duplex System Operation Manual	W405	Provides an outline of and describes the design, installation, maintenance, and other basic operations for a Duplex System based on CS1D CPU Units. (This manual)
SYSMAC CS/CJ/NSJ Series CS1G/H-CPU□□-EV1, CS1G/H-CPU□□H, CS1D-CPU□□HA/H, CS1D-CPU□□SA/S, CJ1G-CPU□□, CJ1M-CPU□□, CJ1G-CPU□□P, CJ1G/H-CPU□□H, NSJ□-□□□□(B)-G5D, NSJ□-□□□□(B)-M3D Programmable Controllers Programming Manual	W394	This manual describes programming and other methods to use the functions of the CS/CJ-series PLCs and NSJ Controllers.
SYSMAC CS/CJ/NSJ Series CJ2H-CPU6□-EIP, CJ2H-CPU6□, CJ2M-CPU□□, CS1G/H-CPU□□H, CS1G/H-CPU□□-EV1, CS1D-CPU□□HA/H, CS1D-CPU□□SA/S, CJ1H-CPU□□H-R, CJ1G/H-CPU□□H, CJ1G-CPU□□P, CJ1M-CPU□□, CJ1G-CPU□□, NSJ□-□□□□(B)-G5D, NSJ□-□□□□(B)-M3D Programmable Controllers Instructions Reference Manual	W474	Provides detailed descriptions of the instructions. When programming, use this manual together with the manuals for your CPU Unit.
SYSMAC CS/CJ Series CQM1H-PRO01-E, C200H-PRO27-E, CQM1-PRO01-E Programming Consoles Operation Manual	W341	Provides information on how to program and operate CS/CJ-series PLCs using a Programming Console.
SYSMAC CS/CJ/CP/NSJ Series CS1G/H-CPU□□-EV1, CS1G/H-CPU□□H, CS1D-CPU□□HA/H, CS1D-CPU□□SA/S, CJ1H-CPU□□H-R, CJ1G-CPU□□, CJ1M-CPU□□, CJ1G-CPU□□P, CJ1G/H-CPU□□H, CJ2H-CPU6□-EIP, CJ2H-CPU6□, CJ2M-CPU□□, CS1W-SCU□□-V1, CS1W-SCB□□-V1, CJ1W-SCU□□-V1, CP1H-X□□□□-□, CP1H-XA□□□□-□, CP1H-Y□□□□-□, CP1L-M/L□□□-□, CP1E-E□□D□-□, CP1E-N□□D□-□, NSJ□-□□□□(B)-G5D, NSJ□-□□□□(B)-M3D Communications Commands Reference Manual	W342	Describes the communications commands used with CS-series, CJ-series, and CP-series PLCs and NSJ Controllers.
SYSMAC CXONE-AL□□D-V4 CX-Programmer Ver. 9.□ Operation Manual	W446	Describes operating procedures for the CX-Programmer Support Software running on a Windows computer.
SYSMAC CX-Programmer Ver. 9.□ CXONE-AL□□D-V4 Operation Manual: Function Blocks/Structured Text	W447	Describes specifications and procedures required to use function blocks and structured text functions.
SYSMAC CXONE-AL□□D-V4 CX-Protocol Operation Manual	W344	Describes the use of the CX-Protocol to create protocol macros as communications sequences to communicate with external devices.
SYSMAC CS/CJ Series Loop Control Boards/Process-control CPU Units/Loop-control CPU Units CS1W-LCB01/LCB05, CS1D-CPU□□P, CJ1G-CPU42P, CJ1G-CPU43P/44P/45P Operation Manual	W406	Provides information on how to operate CS1 Loop Control Boards, including descriptions of the installation, maintenance, and other basic operations.
CS1D-ETN21D Ethernet Unit Operation Manual	W430	Provides information on how to operateCS1D Ethernet Units, including descriptions of the installation, maintenance, and other basic operations.

⚠WARNING Failure to read and understand the information provided in this manual may result in personal injury or death, damage to the product, or product failure. Please read each section in its entirety and be sure you understand the information provided in the section and related sections before attempting any of the procedures or operations given.

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PRECAUTIONS

This section provides general precautions for using the CS1D Programmable Controllers (PLCs) and related devices, including the CS1D-CPU□□HA/H CPU Units for Duplex CPU Systems, CS1D-CPU□□SA/S CPU Units for Single CPU Systems, CS1D-DPL01 Duplex Unit, and CS1D-PA/PD□□□ Power Supply Unit.

The information contained in this section is important for the safe and reliable application of Programmable Controllers. You must read this section and understand the information contained before attempting to set up or operate a PLC system.

1 Intended Audience

This manual is intended for the following personnel, who must also have knowledge of electrical systems (an electrical engineer or the equivalent).

- Personnel in charge of installing FA systems.
- Personnel in charge of designing FA systems.
- Personnel in charge of managing FA systems and facilities.

2 General Precautions

The user must operate the product according to the performance specifications described in the operation manuals.

Before using the product under conditions which are not described in the manual or applying the product to nuclear control systems, railroad systems, aviation systems, vehicles, combustion systems, medical equipment, amusement machines, safety equipment, and other systems, machines, and equipment that may have a serious influence on lives and property if used improperly, consult your OMRON representative.

Make sure that the ratings and performance characteristics of the product are sufficient for the systems, machines, and equipment, and be sure to provide the systems, machines, and equipment with double safety mechanisms.

This manual provides information for programming and operating the Unit. Be sure to read this manual before attempting to use the Unit and keep this manual close at hand for reference during operation.

⚠ WARNING It is extremely important that a PLC and all PLC Units be used for the specified purpose and under the specified conditions, especially in applications that can directly or indirectly affect human life. You must consult with your OMRON representative before applying a PLC System to the above-mentioned applications.

3 Safety Precautions

⚠ WARNING The CPU Unit refreshes I/O even when the program is stopped (i.e., even in PROGRAM mode). Confirm safety thoroughly in advance before changing the status of any part of memory allocated to I/O Units, Special I/O Units, or CPU Bus Units. Any changes to the data allocated to any Unit may result in unexpected operation of the loads connected to the Unit. Any of the following operation may result in changes to memory status.

- Transferring I/O memory data to the CPU Unit from a Programming Device.
- Changing present values in memory from a Programming Device.
- Force-setting/-resetting bits from a Programming Device.
- Transferring I/O memory files from a Memory Card or EM file memory to the CPU Unit.
- Transferring I/O memory from a host computer or from another PLC on a network.

⚠ WARNING Do not attempt to take any Unit apart while the power is being supplied. Doing so may result in electric shock.

⚠ WARNING Do not touch any of the terminals or terminal blocks while the power is being supplied. Doing so may result in electric shock.

⚠ WARNING Do not attempt to disassemble, repair, or modify any Units. Any attempt to do so may result in malfunction, fire, or electric shock.

⚠ WARNING Do not touch the Power Supply Unit while power is being supplied or immediately after power has been turned OFF. Doing so may result in electric shock.

⚠ WARNING Provide safety measures in external circuits (i.e., not in the Programmable Controller), including the following items, to ensure safety in the system if an abnormality occurs due to malfunction of the PLC or another external factor affecting the PLC operation. Not doing so may result in serious accidents.

With a CS1D System operating in Duplex Mode, operation will be stopped and all outputs will be turned OFF in the following circumstances.

- When self-diagnosis simultaneously detects an error in both the active and standby CPU Units.
- When a severe failure alarm (FALS) instruction is simultaneously executed in both the active and standby CPU Units.
- When self-diagnosis detects an error in Simplex Mode or when it detects an error during duplex initialization for Duplex Mode.
- When a severe failure alarm (FALS) instruction is executed in Simplex Mode or during duplex initialization for Duplex Mode.

Unexpected operation, however, may still occur for errors in the I/O control section, errors in I/O memory, and other errors that cannot be detected by the self-diagnosis function. As a countermeasure for all such errors, external safety measures must be provided to ensure safety in the system.

⚠ WARNING The PLC outputs may remain ON or OFF due to deposition or burning of the output relays or destruction of the output transistors. As a countermeasure for such problems, external safety measures must be provided to ensure safety in the system.

⚠ WARNING When the 24-V DC output (service power supply to the PLC) is overloaded or short-circuited, the voltage may drop and result in the outputs being turned OFF. As a countermeasure for such problems, external safety measures must be provided to ensure safety in the system.

⚠ WARNING **Anti-virus protection**
Install the latest commercial-quality antivirus software on the computer connected to the control system and maintain to keep the software up-to-date.

⚠WARNING Security measures to prevent unauthorized access

Take the following measures to prevent unauthorized access to our products.

- Install physical controls so that only authorized personnel can access control systems and equipment.
- Reduce connections to control systems and equipment via networks to prevent access from untrusted devices.
- Install firewalls to shut down unused communications ports and limit communications hosts and isolate control systems and equipment from the IT network.
- Use a virtual private network (VPN) for remote access to control systems and equipment.
- Adopt multifactor authentication to devices with remote access to control systems and equipment.
- Set strong passwords and change them frequently.
- Scan virus to ensure safety of USB drives or other external storages before connecting them to control systems and equipment.

⚠WARNING Data input and output protection

Validate backups and ranges to cope with unintentional modification of input/output data to control systems and equipment.

- Checking the scope of data
- Checking validity of backups and preparing data for restore in case of falsification and abnormalities
- Safety design, such as emergency shutdown and fail-soft operation in case of data tampering and abnormalities

⚠WARNING Data recovery

Backup data and keep the data up-to-date periodically to prepare for data loss.

⚠WARNING When using an intranet environment through a global address, connecting to an unauthorized terminal such as a SCADA, HMI or to an unauthorized server may result in network security issues such as spoofing and tampering.
You must take sufficient measures such as restricting access to the terminal, using a terminal equipped with a secure function, and locking the installation area by yourself.

⚠WARNING When constructing an intranet, communication failure may occur due to cable disconnection or the influence of unauthorized network equipment.
Take adequate measures, such as restricting physical access to network devices, by means such as locking the installation area.

⚠WARNING When using a device equipped with the SD Memory Card function, there is a security risk that a third party may acquire, alter, or replace the files and data in the removable media by removing the removable media or unmounting the removable media.
Please take sufficient measures, such as restricting physical access to the Controller or taking appropriate management measures for removable media, by means of locking the installation area, entrance management, etc., by yourself.

⚠ **Caution** Confirm safety before transferring data files stored in the file memory (Memory Card or EM file memory) to the I/O area (CIO) of the CPU Unit using a peripheral tool. Otherwise, the devices connected to the output unit may malfunction regardless of the operation mode of the CPU Unit.

⚠ **Caution** Fail-safe measures must be taken by the customer to ensure safety in the event of incorrect, missing, or abnormal signals caused by broken signal lines, momentary power interruptions, or other causes. Serious accidents may result from abnormal operation if proper measures are not provided.

⚠ **Caution** Execute online edit only after confirming that no adverse effects will be caused by extending the cycle time. Otherwise, the input signals may not be readable.

⚠ **Caution** The CS1D CPU Units automatically back up the user program and parameter data to flash memory when these are written to the CPU Unit. I/O memory (including the DM, EM, and HR Areas), however, is not written to flash memory. Particularly, the DM, EM, and HR Areas and symbols set to be retained using function blocks can be held during power interruptions with a battery. If there is a battery error, the contents of these areas may not be accurate after a power interruption. If the contents of the DM, EM, and HR Areas and symbols set to be retained using function blocks are used to control external outputs, prevent inappropriate outputs from being made whenever the Battery Error Flag (A40204) is ON. Areas such as the DM, EM, and HR Areas and symbols set to be retained using function blocks, the contents of which can be held during power interrupts, is backed up by a battery. If a battery error occurs, the contents of the areas that are set to be held may not be accurate even though a memory error will not occur to stop operation. If necessary for the safety of the system, take appropriate measures in the ladder program whenever the Battery Error Flag (A40204) turns ON, such as resetting the data in these areas.

⚠ **Caution** Confirm safety at the destination node before transferring a program to another node or changing contents of the I/O memory area. Doing either of these without confirming safety may result in injury.

⚠ **Caution** Tighten the screws on the terminal block of the AC Power Supply Unit to the torque specified in the operation manual. The loose screws may result in burning or malfunction.

⚠ **Caution** Caution is required when connecting peripheral devices, such as a personal computer, to the PLC when Units with non-isolated power supplies, such as the CS1W-CLK12/CLK52(-V1)/CLK13/CLK53, that are connected to an external power supply are mounted to the PLC. If the 24-V side is grounded on the external power supply, a short will be created if the 0-V side of the peripheral device is grounded. When connecting peripheral devices, either ground the 0-V side of the external power supply or do not ground the external power supply at all.

4 Operating Environment Precautions

⚠ **Caution** Do not operate the control system in the following locations:

- Locations subject to direct sunlight.
- Locations subject to temperatures or humidity outside the range specified in the specifications.
- Locations subject to condensation as the result of severe changes in temperature.
- Locations subject to corrosive or flammable gases.
- Locations subject to dust (especially iron dust) or salts.
- Locations subject to exposure to water, oil, or chemicals.
- Locations subject to shock or vibration.

⚠ **Caution** Take appropriate and sufficient countermeasures when installing systems in the following locations:

- Locations subject to static electricity or other forms of noise.
- Locations subject to strong electromagnetic fields.
- Locations subject to possible exposure to radioactivity.
- Locations close to power supplies.

⚠ **Caution** The operating environment of the PLC System can have a large effect on the longevity and reliability of the system. Improper operating environments can lead to malfunction, failure, and other unforeseeable problems with the PLC System. Be sure that the operating environment is within the specified conditions at installation and remains within the specified conditions during the life of the system.

5 Application Precautions

Observe the following precautions when using the PLC System.

- Do not use the C200H/CS-series Power Supply Units (C200H-P□□□□) in a CS1D PLC. System operation will not be dependable and may stop.
- Do not use a CS1D Power Supply Unit (CS1D-PA/PD□□□) for any PLC other than a CS1D PLC. Operational errors and burning will result.
- If duplex Power Supply Units are to be used, calculate the current consumption so that the system will be able to operate with a single Power Supply Unit in case an error occurs in the other Power Supply Unit. If two different kinds of Power Supply Units are to be used, calculate the current consumption using the output of the smaller-capacity Power Supply Unit.
- In a CS1D Duplex CPU System, always mount the CS1D-CPU□□HA/P/H CPU Units for Duplex CPU Systems to the CS1D-BC052/BC042D CPU Backplane. Faulty operation will occur if any other CPU Unit is mounted.
- In a CS1D Single CPU System, always mount a CS1D-CPU□□SA/S CPU Unit for Single CPU Systems to the CS1D-BC82S CPU Backplane. Faulty operation will occur if any other CPU Unit is mounted.
- Do not mount a CS1D-CPU□□HA/SA/P/H/S CPU Unit to a CS1W-BC□□ (non-CS1D) CPU Backplane. Otherwise, faulty operation will occur.
- The cycle time will be increased over the normal cycle time whenever duplex operation is initialized, including when power is turned ON, when the initialization button is pressed, when operation is started, and when data is transferred. The increase will be a maximum of 190 ms for the CS1D-CPU65H, 520 ms for the CS1D-CPU67HA/H and 900 ms for the CS1D-CPU68HA. Set the monitoring time (10 to 40,000 ms, default: 1 s) for the cycle time high enough to allow for this increase. Also, confirm that the system will operate correctly and safely even for the maximum cycle time, including the increase for duplex initialization.
- If operation switches from Duplex Mode to Simplex Mode, processing to synchronize the active and standby CPU Units will no longer be performed, resulting in a shorter cycle time. The more instructions requiring synchronization (such as IORF, DLNK, IORD, IOWR, PID, RXD, FREAD, FWRIT and TWRIT) are used, the greater the difference between Duplex Mode and Simplex Mode operation will be (with Duplex Mode having the longer cycle time). Confirm that the system will operate correctly and safely even for the cycle time in both Simplex and Duplex Modes.
- If the active CPU Unit is switched when PTs or host computers are connected to the RS-232C port on both the active and standby CPU Units, communications may be interrupted momentarily. Always enable retry process in communications programs at the PTs or host computers.
- Before replacing a Unit online, always disable the operation of all connected external devices before starting the replacement procedure. Unexpected outputs from the Unit being replaced may result in unexpected operation of controlled devices or systems.
- Always following the procedures provided in the operation manual when performing online replacement.
- When replacing a Unit online, always replace it with a Unit that has the same specifications.

- When replacing a Duplex Unit online in a Duplex CPU, Dual I/O Expansion System, always follow the procedure provided in this operation manual.
- When replacing a Connecting Cable or Expansion Unit online in a Duplex CPU, Dual I/O Expansion System, always follow the procedure provided in this operation manual.
- When using duplex Connecting Cables in a Duplex CPU, Dual I/O Expansion System, always use cables that are the same length.
- In a Duplex CPU, Dual I/O Expansion System, do not connect two Connecting Cables to Expansion Backplanes that are in different operating levels. Doing so may cause improper operation.
- Before removing a Unit during operation without a PLC Programming Device (CX-Programmer or a Programming Console), always confirm that the Removal of a Unit without a Programming Device or Removal/Addition of Units without a Programming Device function is enabled in the PLC Setup. If a Unit is removed while the PLC Setup is not set to enable Unit removal without a Programming Device, an I/O bus error will occur and the PLC (CPU Unit) will stop operating.
- When a Unit has been removed during operation without a PLC Programming Device (CX-Programmer or a Programming Console), data transferred from the removed Unit to the CPU Unit may be invalid. If an invalid data transfer will adversely affect the system, use a Programming Device to replace the Unit online.
- When the Removal of a Unit without a Programming Device or Removal/Addition of Units without a Programming Device function is enabled in the PLC Setup and a Special I/O Unit has been removed, the Special I/O Unit Area words allocated to that Unit for data transfer (to and from the CPU Unit) will be cleared. If the loss of the Special I/O Unit Area data will adversely affect the system, disable these functions in the PLC Setup and use a Programming Device to replace the Unit online. (When a Programming Device is used to replace the Unit online, the data in the Special I/O Unit Area is retained while the Unit is removed.)
- An I/O bus error, which can be caused by a Unit malfunction, is normally a fatal error that stops operation. When he Removal of a Unit without a Programming Device or Removal/Addition of Units without a Programming Device function is enabled in the PLC Setup, the I/O bus error will be treated as a non-fatal error and PLC (CPU Unit) will not stop operating. If there are any Units that will adversely affect the system if an I/O bus error occurs, do not enable these functions in the PLC Setup.
- Do not turn ON the Maintenance Start Bit (A80015) continuously from the ladder program. As long as the Maintenance Start Bit is ON, errors will not be generated even if there are Unit malfunctions, so the system may be adversely affected.

  Note The Maintenance Start Bit is provided to prevent non-fatal errors from occurring during Unit removal without a Programming Device.
- Do not turn ON the Online Replacement Completed Bit (A80215) continuously from the ladder program. If the Unit is mounted while the Online Replacement Completed Bit is ON, the PLC (CPU Unit) may stop operating.

  Note The Online Replacement Completed Bit is provided to restart the data exchange between the replaced Unit and CPU Unit. After a Unit has been replaced without a Programming Device, turn ON the Online Replacement Completed Bit to restart the data exchange.

- Always turn OFF the reserved pin (RSV) of the Duplex Unit's Communications Setting DIP Switch.
- Never connect pin 6 (5-V power supply) on the RS-232C port on the CPU Unit to any device other than an NT-AL001, CJ1W-CIF11 Adapter, or NV3W-M□20L Programmable Terminal. The external device or the CPU Unit may be damaged.
- You must use the CX-Programmer (programming software that runs on Windows) if you need to program more than one task. A Programming Console can be used to program only one cyclic task. A Programming Console can, however, be used to edit multitask programs originally created with the CX-Programmer.

⚠ **WARNING** Always heed these precautions. Failure to abide by the following precautions could lead to serious or possibly fatal injury.

- Always connect to a ground of 100 Ω or less when installing the Units. Not connecting to a ground of 100 Ω or less may result in electric shock.
- A ground of 100 Ω or less must be installed when shorting the GR and LG terminals on the Power Supply Unit.
- Always turn OFF the power supply to the PLC before attempting any of the following. Not turning OFF the power supply may result in malfunction or electric shock.
  - Mounting or dismounting Power Supply Units, I/O Units, CPU Units, Inner Boards, or any other Units.
  - Assembling the Units.
  - Setting DIP switches or rotary switches.
  - Connecting cables or wiring the system.
  - Connecting or disconnecting the connectors.

⚠ **Caution** Failure to abide by the following precautions could lead to faulty operation of the PLC or the system, or could damage the PLC or PLC Units. Always heed these precautions.

- The user program and parameter area data in the CPU Units are backed up in the built-in flash memory. The BKUP indicator will light on the front of the CPU Unit when the backup operation is in progress. Do not turn OFF the power supply to the CPU Unit when the BKUP indicator is lit. The data will not be backed up if power is turned OFF.
- The PLC Setup is set to specify using the mode set on the Programming Console and a Programming Console is not connected, the CPU Unit will start in RUN mode. This is the default setting in the PLC Setup. (A CS1 CPU Unit will start in PROGRAM mode under the same conditions.)
- When creating an AUTOEXEC.IOM file from a Programming Device (a Programming Console or the CX-Programmer) to automatically transfer data at startup, set the first write address to D20000 and be sure that the size of data written does not exceed the size of the DM Area. When the data file is read from the Memory Card at startup, data will be written in the CPU Unit starting at D20000 even if another address was set when the AUTOEXEC.IOM file was created. Also, if the DM Area is exceeded (which is possible when the CX-Programmer is used), the remaining data

will be written to the EM Area. Refer to information on file operations in the *CS/CJ Series Programming Manual* for details.

- Always turn ON power to the PLC before turning ON power to the control system. If the PLC power supply is turned ON after the control power supply, temporary errors may result in control system signals because the output terminals on DC Output Units and other Units will momentarily turn ON when power is turned ON to the PLC.
- Fail-safe measures must be taken by the customer to ensure safety in the event that outputs from Output Units remain ON as a result of internal circuit failures, which can occur in relays, transistors, and other elements.
- Fail-safe measures must be taken by the customer to ensure safety in the event of incorrect, missing, or abnormal signals caused by broken signal lines, momentary power interruptions, or other causes.
- Interlock circuits, limit circuits, and similar safety measures in external circuits (i.e., not in the Programmable Controller) must be provided by the customer.
- Do not turn OFF the power supply to the PLC when data is being transferred. In particular, do not turn OFF the power supply when reading or writing a Memory Card. Also, do not remove the Memory Card when the BUSY indicator is lit. To remove a Memory Card, first press the memory card power supply switch and then wait for the BUSY indicator to go out before removing the Memory Card.
- If the I/O Hold Bit is turned ON, the outputs from the PLC will not be turned OFF and will maintain their previous status when the PLC is switched from RUN or MONITOR mode to PROGRAM mode. Make sure that the external loads will not produce dangerous conditions when this occurs. (When operation stops for a fatal error, including those produced with the FALS(007) instruction, all outputs from Output Unit will be turned OFF and only the internal output status will be maintained.)
- The contents of the DM, EM, and HR Areas in the CPU Unit are backed up by a Battery. If the Battery voltage drops, this data may be lost. Provide countermeasures in the program using the Battery Error Flag (A40204) to re-initialize data or take other actions if the Battery voltage drops.
- When supplying power at 200 to 240 V AC, always remove the metal jumper from the voltage selector terminals on the Power Supply Unit (except for Power Supply Units with wide-range specifications). The product will be destroyed and must be replaced if 200 to 240 V AC is supplied while the metal jumper is attached. Refer to *5-4 Wiring Methods* for details.
- Always use the power supply voltages specified in the operation manuals. An incorrect voltage may result in malfunction or burning.
- Take appropriate measures to ensure that the specified power with the rated voltage and frequency is supplied. Be particularly careful in places where the power supply is unstable. An incorrect power supply may result in malfunction.
- Install external breakers and take other safety measures against short-circuiting in external wiring. Insufficient safety measures against short-circuiting may result in burning.
- Install the Units as far away as possible from devices that generate strong, high-frequency noise.
- Do not apply voltages to the Input Units in excess of the rated input voltage. Excess voltages may result in burning.

- Do not apply voltages or connect loads to the Output Units in excess of the maximum switching capacity. Excess voltage or loads may result in burning.
- Disconnect the functional ground terminal when performing withstand voltage tests. Not disconnecting the functional ground terminal may result in burning.
- Install the Units properly as specified in the operation manuals. Improper installation of the Units may result in malfunction.
- Be sure that all the Backplane mounting screws, terminal block screws, and cable connector screws are tightened to the torque specified in the relevant manuals. Incorrect tightening torque may result in malfunction.
- Always remove any dustproof labels that are on the top of the Units when they are shipped before you tum ON the power supply. If the labels are not removed, heat will accumulate and malfunctions may occur.
- Do not allow wire clippings, shavings, or other foreign material to enter any Unit. Otherwise, Unit burning, failure, or malfunction may occur. Cover the Units or take other suitable countermeasures, especially during wiring work.
- Use crimp terminals for wiring. Do not connect bare stranded wires directly to terminals. Connection of bare stranded wires may result in burning.
- Wire all connections correctly.
- Double-check all wiring and switch settings before turning ON the power supply. Incorrect wiring may result in burning.
- Mount Units only after checking terminal blocks and connectors completely.
- Be sure that the terminal blocks, Memory Units, expansion cables, and other items with locking devices are properly locked into place. Improper locking may result in malfunction.
- Check switch settings, the contents of the DM Area, and other preparations before starting operation. Starting operation without the proper settings or data may result in an unexpected operation.
- Check the user program for proper execution before actually running it on the Unit. Not checking the program may result in unexpected operation.
- Confirm that no adverse effect will occur in the system before attempting any of the following. Not doing so may result in an unexpected operation.
    - Changing the operating mode of the PLC (including the setting of the startup operating mode).
    - Force-setting/force-resetting any bit in memory.
    - Changing the present value of any word or any set value in memory.
- Resume operation only after transferring to the new CPU Unit the contents of the DM Area, HR Area, and other data required for resuming operation. Not doing so may result in an unexpected operation.
- Do not pull on the cables or bend the cables beyond their natural limit. Doing either of these may break the cables.
- Do not place objects on top of the cables or other wiring lines. Doing so may break the cables.
- Do not use commercially available RS-232C personal computer cables. Always use the special cables listed in this manual or make cables according to manual specifications. Using commercially available cables may damage the external devices or CPU Unit.

- When replacing parts, be sure to confirm that the rating of a new part is correct. Not doing so may result in malfunction or burning.
- Before touching a Unit, be sure to first touch a grounded metallic object in order to discharge any static build-up. Not doing so may result in malfunction or damage.
- When transporting or storing circuit boards, cover them in antistatic material to protect them from static electricity and maintain the proper storage temperature.
- Do not touch circuit boards or the components mounted to them with your bare hands. There are sharp leads and other parts on the boards that may cause injury if handled improperly.
- Do not short the battery terminals or charge, disassemble, heat, or incinerate the battery. Do not subject the battery to strong shocks. Doing any of these may result in leakage, rupture, heat generation, or ignition of the battery. Dispose of any battery that has been dropped on the floor or otherwise subjected to excessive shock. Batteries that have been subjected to shock may leak if they are used.
- UL standards required that batteries be replaced only by experienced technicians. Do not allow unqualified persons to replace batteries.
- Dispose of the product and batteries according to local ordinances as they apply. Have qualified specialists properly dispose of used batteries as industrial waste.

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- Separate the line ground terminal (LG) from the functional ground terminal (GR) on the Power Supply Unit before performing withstand voltage tests or insulation resistance tests.
- Do not drop the product or subject it to excessive vibration or shock.
- Both duplex Ethernet Units will be reset and communications will temporarily stop when I/O tables are created or transferred or Units are added online in a system that uses duplex Ethernet with the CS1D. Confirm that the system will not be adversely affected before executing these operations.

6 Conformance to EU Directives

6-1 Applicable Directives

- EMC Directives
- Low Voltage Directive

6-2 Concepts

EMC Directives

OMRON devices that comply with EU Directives also conform to the related EMC standards so that they can be more easily built into other devices or the overall machine. The actual products have been checked for conformity to EMC standards (see the following note). Whether the products conform to the standards in the system used by the customer, however, must be checked by the customer.

EMC-related performance of the OMRON devices that comply with EU Directives will vary depending on the configuration, wiring, and other conditions of the equipment or control panel on which the OMRON devices are installed. The customer must, therefore, perform the final check to confirm that devices and the overall machine conform to EMC standards.

Note Applicable EMC (Electromagnetic Compatibility) standards are as follows:

EMS (Electromagnetic Susceptibility): EN61131-2 or EN61000-6-2
EMI (Electromagnetic Interference): EN61000-6-4
(Radiated emission: 10-m regulations)

Low Voltage Directive

Always ensure that devices operating at voltages of 50 to 1,000 V AC and 75 to 1,500 V DC meet the required safety standards for the PLC (EN61131-2).

6-3 Conformance to EU Directives

The CS1D Duplex PLCs comply with EU Directives. To ensure that the machine or device in which the CS1D Duplex PLC is used complies with EU Directives, the PLC must be installed as follows:

1,2,3...

1. The CS1D Duplex PLC must be installed within a control panel.
2. You must use reinforced insulation or double insulation for the DC power supplies used for the communications power supply and I/O power supplies.
3. CS1D Duplex PLCs complying with EU Directives also conform to the Common Emission Standard (EN61000-6-4). Radiated emission characteristics (10-m regulations) may vary depending on the configuration of the control panel used, other devices connected to the control panel, wiring, and other conditions. You must therefore confirm that the overall machine or equipment complies with EU Directives.

6-4 Relay Output Noise Reduction Methods

The CS1D Duplex PLCs conforms to the Common Emission Standards (EN61000-6-4) of the EMC Directives. However, noise generated by relay output switching may not satisfy these Standards. In such a case, a noise filter must be connected to the load side or other appropriate countermeasures must be provided external to the PLC.

Countermeasures taken to satisfy the standards vary depending on the devices on the load side, wiring, configuration of machines, etc. Following are examples of countermeasures for reducing the generated noise.

Countermeasures

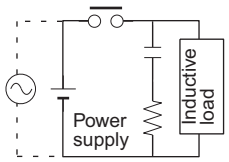
(Refer to EN61000-6-4 for more details.)

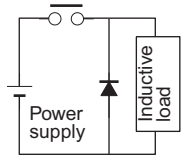
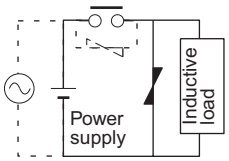
Countermeasures are not required if the frequency of load switching for the whole system with the PLC included is less than 5 times per minute.

Countermeasures are required if the frequency of load switching for the whole system with the PLC included is more than 5 times per minute.

Countermeasure Examples

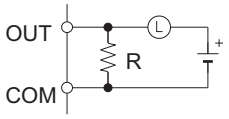
When switching an inductive load, connect an surge protector, diodes, etc., in parallel with the load or contact as shown below.

Circuit	Current		Characteristic	Required element
	AC	DC		
CR method 	Yes	Yes	If the load is a relay or solenoid, there is a time lag between the moment the circuit is opened and the moment the load is reset. If the supply voltage is 24 or 48 V, insert the surge protector in parallel with the load. If the supply voltage is 100 to 200 V, insert the surge protector between the contacts.	The capacitance of the capacitor must be 1 to 0.5 μF per contact current of 1 A and resistance of the resistor must be 0.5 to 1 Ω per contact voltage of 1 V. These values, however, vary with the load and the characteristics of the relay. Decide these values from experiments, and take into consideration that the capacitance suppresses spark discharge when the contacts are separated and the resistance limits the current that flows into the load when the circuit is closed again. The dielectric strength of the capacitor must be 200 to 300 V. If the circuit is an AC circuit, use a capacitor with no polarity.

Circuit	Current		Characteristic	Required element
	AC	DC		
Diode method 	No	Yes	The diode connected in parallel with the load changes energy accumulated by the coil into a current, which then flows into the coil so that the current will be converted into Joule heat by the resistance of the inductive load. This time lag, between the moment the circuit is opened and the moment the load is reset, caused by this method is longer than that caused by the CR method.	The reversed dielectric strength value of the diode must be at least 10 times as large as the circuit voltage value. The forward current of the diode must be the same as or larger than the load current. The reversed dielectric strength value of the diode may be two to three times larger than the supply voltage if the surge protector is applied to electronic circuits with low circuit voltages.
Varistor method 	Yes	Yes	The varistor method prevents the imposition of high voltage between the contacts by using the constant voltage characteristic of the varistor. There is time lag between the moment the circuit is opened and the moment the load is reset. If the supply voltage is 24 or 48 V, insert the varistor in parallel with the load. If the supply voltage is 100 to 200 V, insert the varistor between the contacts.	---

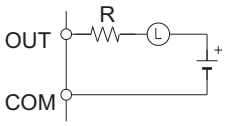
When switching a load with a high inrush current such as an incandescent lamp, suppress the inrush current as shown below.

Countermeasure 1



Providing a dark current of approx. one-third of the rated value through an incandescent lamp

Countermeasure 2



Providing a limiting resistor

SECTION 1
Features and System Configuration

This section introduces the features and system configuration of a CS1D Duplex PLC System.

1-1 CS1D Duplex System Overview and Features

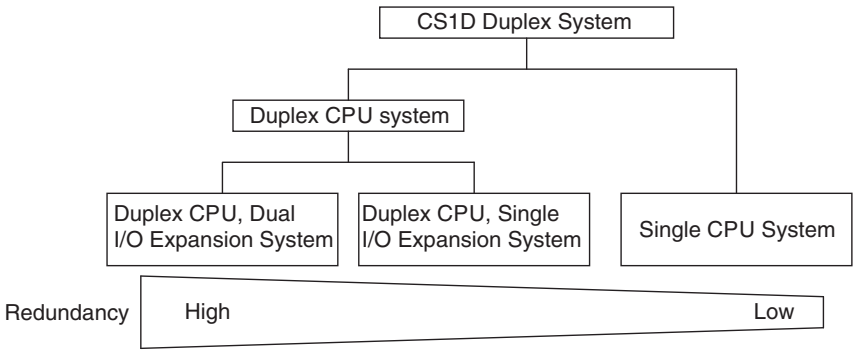
1-1-1 CS1D Duplex System Overview

The CS1D Duplex System is a highly reliable Programmable Controller (PLC) System. By providing duplex CPU Units, Power Supply Units, and Communications Units, the CS1D can continue control operations and be restored with no need to shut down the entire system in the event of an error or malfunction.

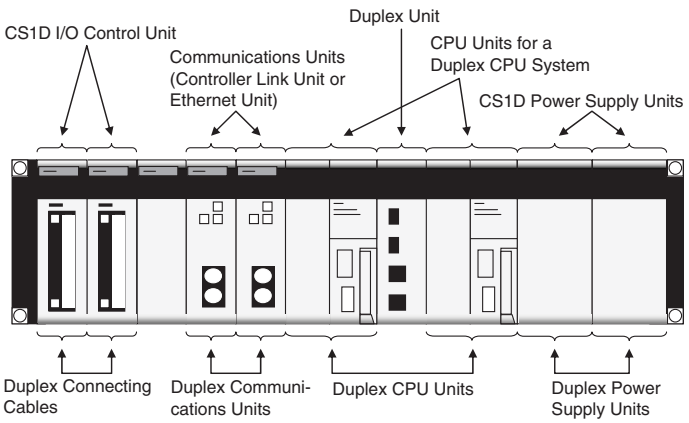
Select from either of two Duplex Systems: A Duplex CPU System or a Single CPU System. A Duplex CPU System includes two CPU Units. Even if an error occurs in the active CPU Unit, the standby CPU Unit continues operation, thus preventing a system shutdown. The Single CPU System uses a single CPU Unit. In either System, duplex Power Supply Units or Communications Units can be used to provide high reliability in the event of an error in the power supply system or the active Communications Unit.

It is now possible to select a Duplex CPU with duplex Connecting Cables (Dual I/O Expansion System), as well as the previously available Duplex CPU with a single Connecting Cable (Single I/O Expansion System).

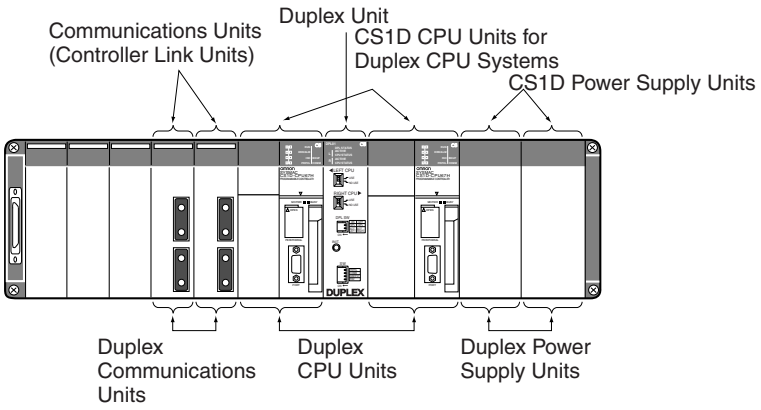
CS1D Duplex System Configurations



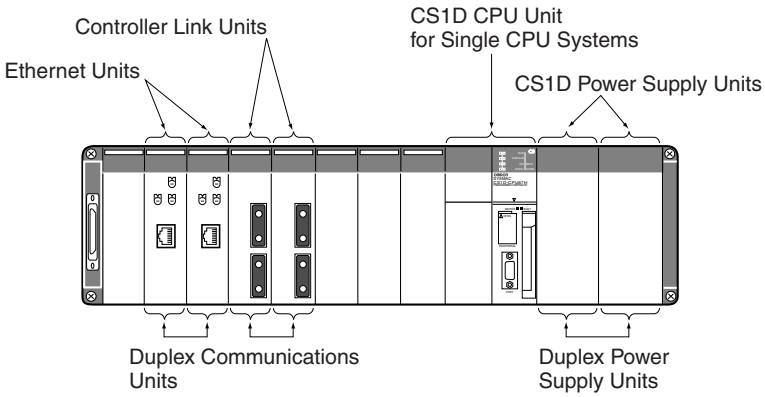
Duplex CPU, Dual I/O Expansion System



Duplex CPU, Single I/O Expansion System



Single CPU System



1-1-2 CS1D Duplex System Features

Duplex CPU Systems

Two CPU Units and one Duplex Unit are mounted.

The two CPU Units always run the same user's program. One of them executes the system I/O while the other remains on standby. If an error (see note) occurs in the controlling CPU Unit (called the active CPU Unit), control is switched to the other CPU Unit (called the standby CPU Unit), and operation continues. (The system will stop, however, if the same error occurs in the standby CPU Unit, or if another operation switching error or a fatal error occurs.)

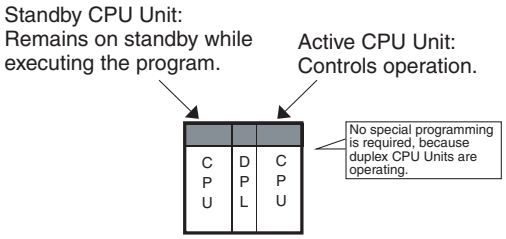
Note Operation will be taken over by the standby CPU Unit for any of the following operation switching errors: CPU error, memory error, cycle time overrun error, program error, FALS error, or fatal Inner Board error. (A fatal Inner Board error applies only to Process-control CPU Units.)

Using the Hot Standby Method

With the hot standby method, the standby CPU Unit operates with the same status as the active CPU Unit. Using this method provides the following benefits.

1,2,3... 1. There is no need to incorporate special programming for duplex operations, such as programming to switch when an error occurs, and thus there is no need for the duplex setup to be considered in individual parameter settings.

2. The time required for switching when an error occurs is shortened, enabling operation to be continued without any interruption.



Automatic Recovery to Duplex Mode

With existing Duplex CPU Systems (such as the CVM1D), it is necessary to manually return the system to Duplex Mode after a CPU Unit error occurs during operation in Duplex Mode and operation is switched to Simplex Mode.

With the CS1D Duplex System, operation is automatically returned to the original Duplex Mode when the error that caused the switch to Simplex Mode is cleared.

Unmanned duplex operation can be continued even when incidental errors occur temporarily due to causes such as noise.

Single CPU Systems

Although only a single CPU Unit is mounted, duplex Power Supply Units, duplex Communications Units, and online Unit replacement are possible.

Duplex Power Supply Units

Power is always supplied in parallel from two Power Supply Units. Even if one of the Power Supply Units breaks down, the other one continues providing power automatically. Power Supply Unit models for AC power and DC power are both available, and a combination of both types can be used. A Power Supply Unit that malfunctions or for which a broken line occurs can be confirmed by means of flags in the AR Area. If a Power Supply Unit malfunctions, it can be replaced online without turning OFF the power supply or stopping operation.

Duplex Communications Units

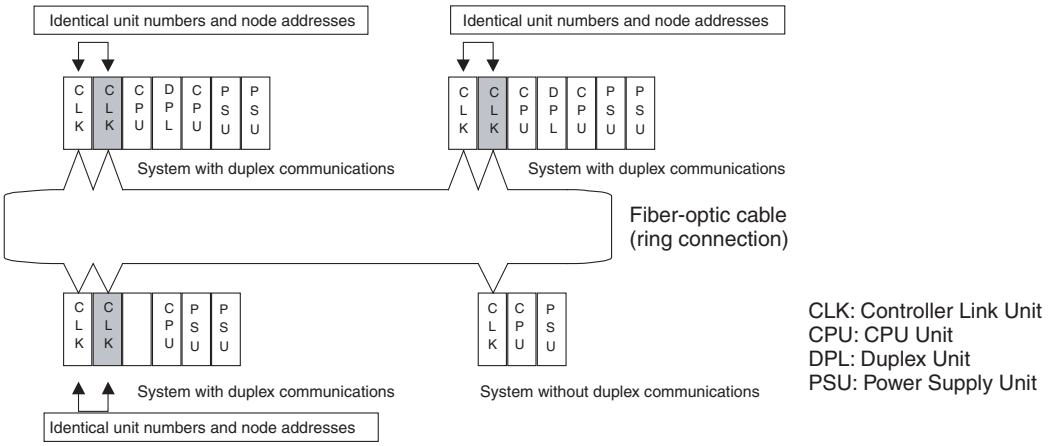
Duplex Controller Link Units Using Active/ Standby Units

Two Communications Units (see note) are connected by fiber-optic cable. If one of the Units stops communicating, the other one continues communications.

Note The following Communications Units support duplex operation: The CS1W-CLK12-V1/CLK13 (H-PCF Cable) and the CS1W-CLK52-V1/CLK53 (GI Cable) Controller Link Units.

As shown in the following diagram, two Controller Link Units are mounted in a single network with identical unit numbers and node addresses. One of the Controller Link Units is in standby mode.

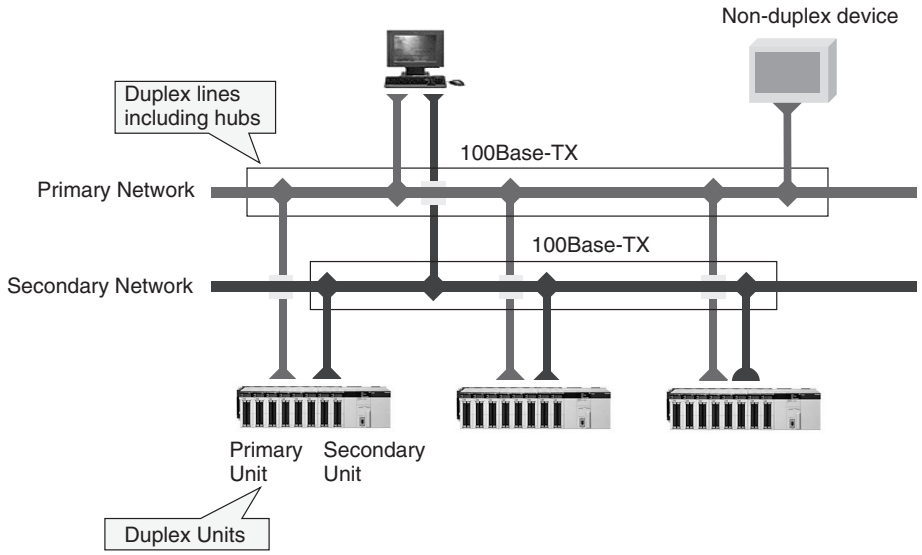
When an error is detected at the active Controller Link Unit, the standby Controller Link Unit switches to active operating status. This allows communications to continue without the node being disconnected.



Duplex Ethernet Units Using Primary/Secondary Lines

Using duplex Ethernet Units and redundant communications lines increases the reliability of the network. The communications lines use a primary line and a secondary line, to which Ethernet Units are connected. Normally the primary communications line is used, but operation will switch to the secondary communications line automatically if an error occurs in the primary communications line or the primary Ethernet Unit, thereby allowing continuous communications.

- Duplex Ethernet Units do not require duplex programming considerations. The CPU Unit select the Unit to use as the send destination.
- Ethernet Units use 100Base-TX and support high-speed communications.



Note Duplex operation of Ethernet Units for a Duplex CPU System requires a CS1D CPU Unit Ver. 1.1 or later and CX-Programmer Ver. 4.0 or higher. Duplex operation of Ethernet Units for a Single CPU System is possible for any CS1D CPU Unit for Single CPU Systems, but CX-Programmer Ver. 4.0 or higher is required.

Duplex CPU, Dual I/O Expansion System (Duplex CPU System Only)

A more reliable system can be configured by expanding the Duplex CPU System.

Note A Duplex CPU, Dual I/O Expansion System requires compatible Duplex Units, CPU Backplane, Expansion Backplanes, I/O Control Units, I/O Interface Units, and Duplex CPU Units with unit version 1.3 or later.

Duplex Connecting Cables When the Connecting Cable between the CPU Rack and Expansion Racks is duplexed, the system can continue operating through the second Cable if one Cable is damaged or disconnected.

Online Replacement of Duplex Units If a Duplex Unit fails, the faulty Unit can now be replaced online. (The PLC operates in simplex mode while the Duplex Unit is being replaced.)

Replacement of Basic and Special I/O Units without a Programming Device If the *Removal/Addition of Units without a Programming Device* function is enabled in advance, Units can be removed and mounted without any CX-Programmer or Programming Console operations.

Online Addition of Units and Expansion Backplanes A CX-Programmer operation can be used to add a Basic I/O Unit, Special I/O Unit, or Expansion Backplane to an existing Rack. An operating Rack can be expanded without stopping the Rack.

CS Series Compatibility

The CS1D CPU Units (CS1D-CPU□□HA/SA/H/S) are based on the architecture of CS1-H CPU Units and can use the same programs and Units as the CS1 and CS1-H CPU Units.

For a comparison of functions between the CS1D and CS1-H Units, refer to *Appendix E Precautions in Replacing CS1-H PLCs with CS1D PLCs*.

Online Replacement of CPU Units

CPU Units can be replaced online without stopping system operation.

Online Replacement of Basic I/O Units, Special I/O Units, and CPU Bus Units

Basic I/O Units, Special I/O Units, and CPU Bus Units can be replaced online by using Programming Console or CX-Programmer operations (see note). In particular, with Duplex Communications Units (e.g., Ethernet Units and Controller Link Units, optical ring type, token ring mode). Communications Units can be replaced without disconnecting the node or interrupting communications.

Note
1. Online Unit replacement is possible with CX-Programmer Ver. 3.1 or higher.
2. When CS1D CPU Units with unit version 1.3 or later are being used and the *Removal/Addition of Units without a Programming Device* function has been enabled in advance, Units can be replaced without any CX-Programmer or Programming Console operations.

1-1-3 Functions in Upgraded Version of the CS1D-CPU□□HA/SA

As for the CS1D-CPU□□HA/SA, the following functions have been added to the CS1D-CPU□□H/S.

Function Blocks (FB)

Function blocks (FB) conforming to IEC 61131-3 are supported. Use of function blocks is determined by the user.

Note IEC 61131-3 is an international standard for programmable logic controllers (PLC) established by the International Electro-technical Commission (IEC). This standard is divided into seven parts, of which Part 3 *Programming Languages* (IEC 61131-3) provides regulations for programming PLCs.

Function blocks can be created with CX-Programmer Ver. 9.7 or higher by the user and pasted into normal programs. The standard function blocks provided by OMRON in the OMRON FB Library can also be pasted into normal programs. Function blocks enable standard processing to be simply inserted into a program as a single unit. Function blocks provide the following features.

- Function block algorithms can be written using ladder programming or structured text (see note).

  Note Structured text is a high level textual language designed for industrial control (primarily PLCs) stipulated in IEC 61131-3. The structured text supported by CX-Programmer Ver. 5.0 conforms to IEC 61131-1.
- A single function block that has been created can be stored in a library for easy reuse of standard processing.
- Programs that contain function blocks (ladder programming or structured text), can also be uploaded or downloaded in the same way as normal programs that do not contain function blocks. Tasks that include function blocks, however, cannot be downloaded in task units (although they can be uploaded).
- Array (one-dimensional) variables are supported, making it easier to handle data specific to an application.

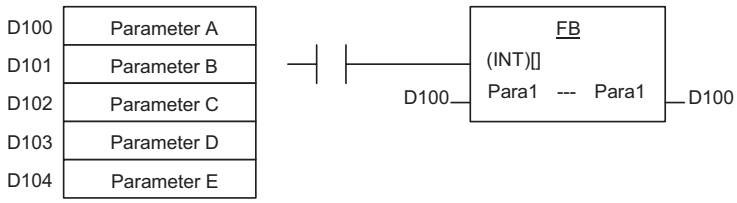
Moreover, the following functions can also be performed in function blocks (FB).

Online Editing of Function Blocks

Function block definitions can be changed during operation. This allows function block definitions to be quickly corrected during debugging. It also allows function blocks to be used more easily in systems that operate 24 hours a day.

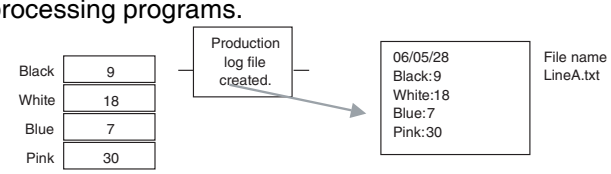
Input-Output Variables in Function Blocks

Input-output variables can be used to passed large quantities of data, such as table data.



Text String Support in Function Blocks

Text strings can be used in ST programming to easily create text string processing programs.



FB to Create Production Log File

```
stBlack := INT_TO_STRING(Data[0]);      (* Convert black quantity to string *)
stWhite := INT_TO_STRING(Data[1]);      (* Convert white quantity to string *)
stBlue := INT_TO_STRING(Data[2]);       (* Convert blue quantity to string *)
stPink := INT_TO_STRING(Data[3]);       (* Convert pink quantity to string *)

GetDate(stDay)                          (* Get date text *)

stMessage := stDay  + '$N' + 'Black : '+ stBlack + '$N' + 'White : '+ stWhite + '$N' + 'Blue : '+ stBlue + '$N' + 'Pink : '+ stPink + '$N';

WRITE_TEXT(stMessage, '¥LineA', '', 0);     (* Create production log LineA.txt *)
```

FB to Create Date Text

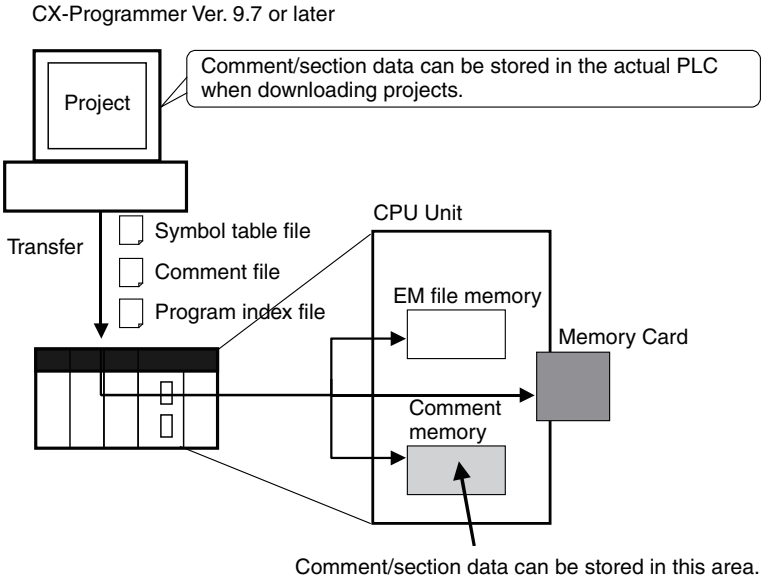
```
(* ================================================================
     Name: Generate Date Text
     Function: To create text data for yy/mm/dd

     (C)Copyright OMRON Corporation 2006 All Rights Reserved.
================================================================ *)


stYYMM := WORD_TO_STRING(YYMM);     (* Create yymm text *)
stDDHH := WORD_TO_STRING(DDHH);     (* Create ddhh text *)

stDay := insert(stYYMM,'/',2) + '/' + left(stDDHH,2);
                    (* Insert / between yy and mm; extract only dd and combine *)
```

Comment Memory (in Internal Flash Memory)

A comment memory is provided within the CPU Unit's internal flash memory. Therefore, the following comment/section data can be stored in and read from comment memory even if neither Memory Card nor EM file memory are available.

- Symbol table files (including CX-Programmer symbol names and I/O comments)
- Comment files (CX-Programmer rung comments and other comments)

- Program index files (CX-Programmer section names, section comments, and program comments)



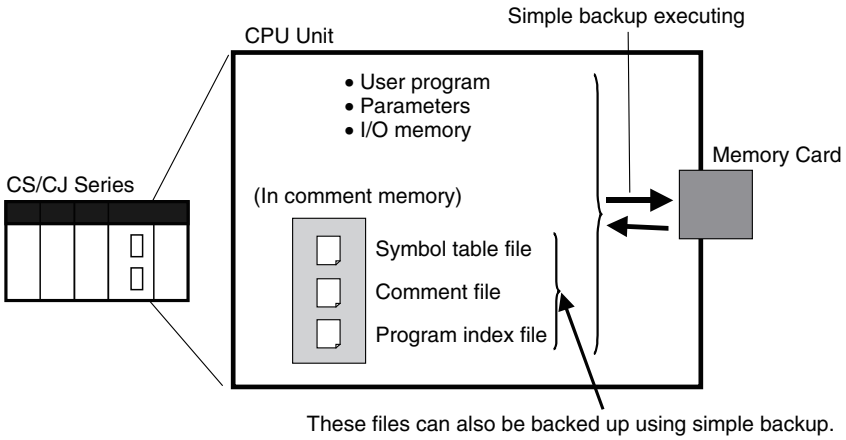
When downloading projects using the CX-Programmer Ver. 9.7, either of the following storage locations can be selected as the transfer destination for comment data and section data.

- Memory Card
- EM file memory
- Comment memory (in CPU Unit's internal flash memory)

Simple Backup Data Expanded

The following files stored in comment memory can be backed up to a Memory Card when a simple backup operation is executed, or the files can be restored to comment memory from the Memory Card.

- Symbol table files (including CX-Programmer symbol names and I/O comments)
- Comment files (CX-Programmer rung comments and other comments)
- Program index files (CX-Programmer section names, section comments, and program comments)



This enables backup/restoration of all data in the CPU Unit including I/O comments if an error occurs or when adding a CPU Unit with the same specifications without requiring a Programming Device.

Free Running Timer

The system timers used after the power is turned ON are contained in the following Auxiliary Area words.

Name	Address	Function	Access
10-ms Incrementing Free Running Timer	A000	This word contains the system timer used after the power is turned ON. 0000 hex is set when the power is turned ON and this value is automatically incremented by 1 every 10 ms. The value returns to 0000 hex after reaching FFFF hex (655,350 ms), and then continues to be automatically incremented by 1 every 10 ms.	Read-only
100-ms Incrementing Free Running Timer	A001	This word contains the system timer used after the power is turned ON. 0000 hex is set when the power is turned ON and this value is automatically incremented by 1 every 100 ms. The value returns to 0000 hex after reaching FFFF hex (6,553,500 ms), and then continues to be automatically incremented by 1 every 100 ms.	Read-only
1-s Incrementing Free Running Timer	A002	This word contains the system timer used after the power is turned ON. 0000 hex is set when the power is turned ON and this value is automatically incremented by 1 every second. The value returns to 0000 hex after reaching FFFF hex (65,535 s), and then continues to be automatically incremented by 1 every second.	Read-only

Note The timer will continue to be incremented when the operating mode is switched to RUN mode.

Example: The interval can be counted between processing A and processing B without requiring timer instructions. This is achieved by calculating the difference between the value in A000 for processing A and the value in A000 for processing B. The interval is counted in 10 ms units.
CPU Units with unit version 4.0 and later also have a 1-s timer in A002, which is incremented by 1 every 1 s.

New Special Instructions and Functions

The following new instructions and instruction functions have been added. For details, refer to the CS/CJ Series Instructions Reference Manual (W474). These new instructions are supported by the CX-Programmer Ver. 9.7 or higher only.

- Serial communications instructions (CS1D-CPU□□SA only):
  Supporting no-protocol communications with Serial Communications Units with unit version 1.2 or later:
  TXDU(256): TRANSMIT VIA SERIAL COMMUNICATIONS UNIT
  RXDU(255): RECEIVE VIA SERIAL COMMUNICATIONS UNIT
  Supporting no-protocol communications with Serial Communications Boards with unit version 1.2 or later:
  TXD(236): TRANSMIT
  RXD(235): RECEIVE

- Special Instructions for function blocks:
  GET VARIABLE ID instruction (GETID):
  Outputs the FINS command variable type (data area) code and word address for the specified variable or address.
- Numerical value to ASCII conversion instructions and ASCII to numerical value conversion instructions:
  4/8/16-digit numerical value to ASCII data conversion instruction (STR4/STR8/STR16):
  Convert the numerical data (4/8/16-digit hexadecimals) to the ASCII data (4/8/16 characters).
  ASCII data to 4/8/16-digit numerical value conversion instruction (NUM4/NUM8/NUM16):
  Convert the ASCII data (4/8/16 characters) to the numerical data (4/8/16-digit hexadecimals).

Duplex CPU Compatible Setting (CS1D-CPU67HA Only)

The Duplex CPU Compatible Setting on the CS1D-CPU67HA enables the CPU Unit duplexity with the CS1D-CPU65H or CS1D-CPU67H.

1-2 System Configuration

1-2-1 CS1D Duplex Systems

Duplex Functions

The following duplex functions are supported by a CS1D Duplex System.

Duplex function		Support					
		(CS1D-CPU□□HA)	Duplex CPU System (CS1D-CPU□□H)				Single CPU System (CS1D-CPU□□S) (CS1D-CPU□□SA)
		Unit Ver. 4.0	Unit Ver. 1.3 to 1.4	Unit Ver. 1.2	Unit Ver. 1.1	Pre-Ver. 1.1	
Duplex CPU Units (with Duplex Inner Boards) (See note 1.)		Yes	Yes	Yes	Yes	Yes	No
Duplex Power Supply Units (See note 2.)		Yes	Yes	Yes	Yes	Yes	Yes
Duplex Communications Units (See note 3.)	Controller Link Units	Yes	Yes	Yes	Yes	Yes	Yes
	Ethernet Units	Yes	Yes	Yes	Yes	No	
Duplex Connecting Cables (See note 4.)		Yes	Yes	No	No	No	No
Online Unit Replacement using a Programming Device		Yes	Yes	Yes	Yes	Yes	Yes
Unit Removal without a Programming Device		Yes	Yes	Yes	No	No	No
Removal/Addition of Units without a Programming Device (See note 4.)		Yes	Yes	No	No	No	No
Online Addition of Duplex Unit (See note 4.)		Yes	Yes	No	No	No	No
Online Addition of Units and Backplanes (See notes 4 and 5.)		Yes	Yes	No	No	No	No

Note 1. The only Duplex Inner Boards that can be used are the ones built into the the Process-control CPU Units. Process-control CPU Units consist of a CPU Unit for Duplex CPU Systems with a built-in Loop Control Board (Inner Board). The following two types are available. The Loop Control Boards cannot be removed from these CPU Units.

Process-control CPU Unit	CPU Unit	Loop Control Board
CS1D-CPU65P	CS1D-CPU65H	CS1D-LCB05D
CS1D-CPU67P	CS1D-CPU67H	

Details on the CPU Units are provided in this manual. For details on the Loop Control Boards, refer to the *Loop Control Boards Operation Manual* (W406) and the *Loop Control Board Function Block Reference Manual* (W407).

2. A single Power Supply Unit can also be used, but it must be the CS1D Power Supply Unit
3. A single Communications Unit can also be used, but it must be a CS-series Communications Unit. Duplex Units can also be used for both Controller Link Units and Ethernet Units at the same time.
4. In a Duplex CPU, Dual I/O Expansion System, an Expansion Backplane can be added in addition to Basic I/O Units and Special I/O Units. (CPU Bus Units cannot be added.)
5. In a Duplex CPU, Single I/O Expansion System, only Basic I/O Units and Special I/O Units can be added. (Expansion Backplanes and CPU Bus Units cannot be added.)

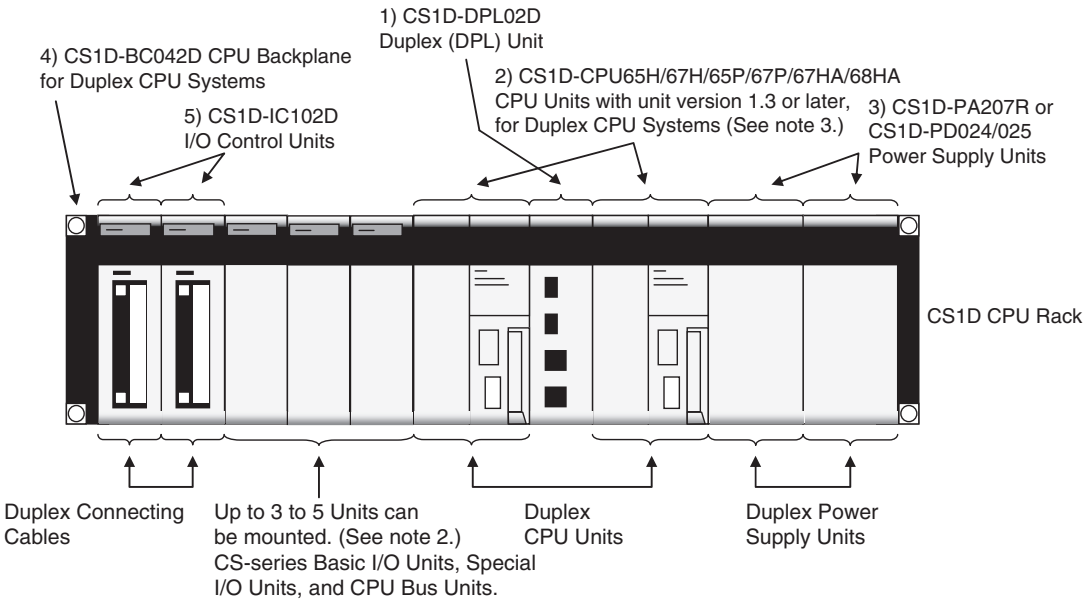
The Two Modes in a CS1D Duplex CPU System

A CS1D Duplex CPU System can be operated in either Duplex Mode or Simplex Mode.

- Duplex Mode
  In Duplex Mode, the CPU Units are placed in duplex system status. If a fatal error occurs in the active CPU Unit, control is switched to the standby CPU Unit and operation continues.
- Simplex Mode
  In Simplex Mode, a single CPU Unit controls operation.

System Configuration

CS1D CPU Rack for a Duplex CPU, Dual I/O Expansion System



Note

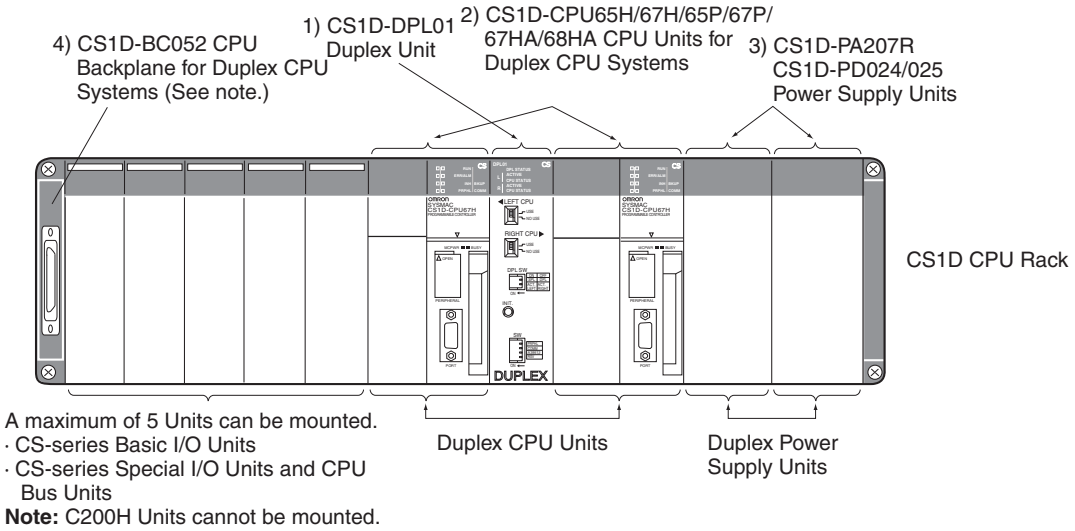
1. C200H-series Units cannot be mounted.
2. The maximum number of Units depends on the number of CS1D I/O Control Units that are mounted.
3. The only CPU Units that can be mounted are CPU Units for a CS1D Duplex System with a unit version 1.3 or later. If a CPU Unit with unit version

1.2 or earlier is mounted, an I/O bus error will occur and the system will not operate.

	Name	Model number	Contents
1	Duplex Unit (Especially for a Duplex CPU, Dual I/O Expansion System)	CS1D-DPL02D	The Duplex Unit is the Unit that controls duplex system operation. It monitors for errors and switches operation when an error occurs. This Duplex Unit can be replaced online. This Duplex Unit cannot be used in a Duplex CPU, Single I/O Expansion System.
2	CPU Units for Duplex CPU Systems (Unit version 1.3 or later)	CS1D-CPU67HA CS1D-CPU68HA CS1D-CPU65H CS1D-CPU67H CS1D-CPU65P CS1D-CPU67P	CPU Units for Duplex CPU System are designed especially for a Duplex CPU System. Two CPU Units of the identical model are mounted. CPU Units with unit version 1.3 or later are required. CPU Units on which the Duplex CPU Compatible Setting has been changed can be used. These CPU Units cannot be used in a Single CPU System.
3	CS1D Power Supply Units	CS1D-PA207R CS1D-PD024 CS1D-PD025	CS1D Power Supply Units are designed especially for a Duplex System. Two Power Supply Units are mounted to a CPU Rack, Expansion Rack, or Long-distance Expansion Rack for a duplex power supply configuration. When not configuring a duplex power supply, only one Power Supply Unit is mounted.
4	CPU Backplane for Duplex CPU Systems (Especially for a Duplex CPU, Dual I/O Expansion System)	CS1D-BC042D	A CPU Backplane for Duplex CPU System is used in a Duplex CPU System. It allows the mounting of Duplex CPU Units, Duplex Power Supply Units, and Duplex Communications Units, as well as online Unit replacement and online Duplex Unit replacement. These Backplanes cannot be used as Backplanes for Long-distance Expansion Racks.
5	CS1D I/O Control Unit (Especially for a Duplex CPU, Dual I/O Expansion System)	CS1D-IC102D	These Units are required to create a Duplex CPU, Dual I/O Expansion System. The Connecting Cables can be duplexed by using two of these Units. These I/O Control Units cannot be used in a Duplex CPU, Single I/O Expansion System.

Note When using a Memory Card in Duplex Mode, mount it in the active CPU Unit. (Duplex Memory Card operation is not possible.) Duplex EM File Memory operation is possible.

CS1D CPU Rack for a Duplex CPU, Single I/O Expansion System

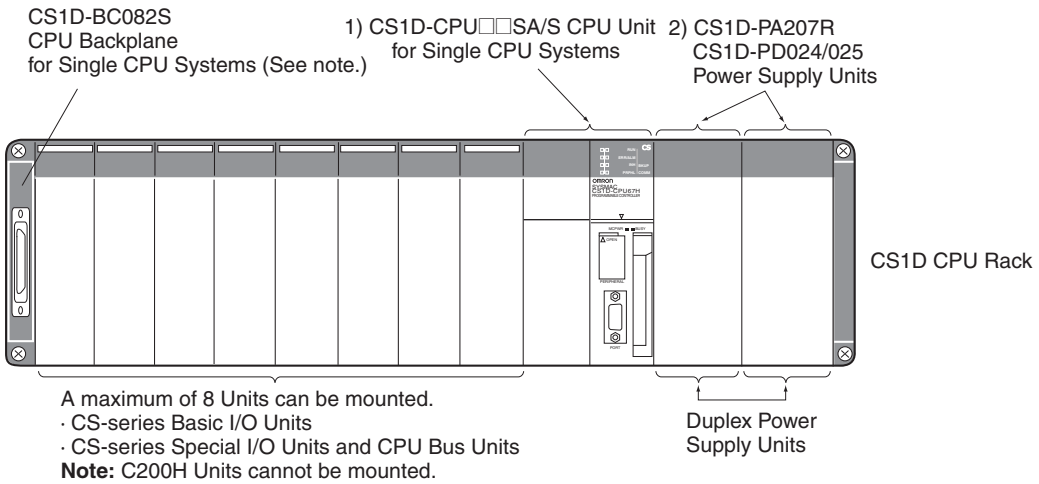


Note: C200H Units cannot be mounted.

	Name	Model number	Contents
1	Duplex Unit (Especially for a Duplex CPU, Single I/O Expansion System)	CS1D-DPL01	The Duplex Unit is the Unit that controls duplex system operation. It monitors for errors and switches operation when an error occurs. This Duplex Unit cannot be used in a Duplex CPU, Dual I/O Expansion System.
2	CPU Units for Duplex CPU Systems	CS1D-CPU67HA CS1D-CPU68HA CS1D-CPU65H CS1D-CPU67H CS1D-CPU65P CS1D-CPU67P	CPU Units for Duplex CPU System are designed especially for a Duplex CPU System. Two CPU Units of the identical model are mounted. CPU Units on which the Duplex CPU Compatible Setting has been changed can be used. These CPU Units cannot be used in a Single CPU System.
3	CS1D Power Supply Units	CS1D-PA207R CS1D-PD024 CS1D-PD025	CS1D Power Supply Units are designed especially for a Duplex System. Two Power Supply Units are mounted to a CPU Rack, Expansion Rack, or Long-distance Expansion Rack for a duplex power supply configuration. When not configuring a duplex power supply, only one Power Supply Unit is mounted.
4	CPU Backplane for Duplex CPU Systems (Especially for a Duplex CPU, Single I/O Expansion System)	CS1D-BC052	A CPU Backplane for Duplex CPU System is used in a Duplex CPU System. It allows Duplex CPU Units, Duplex Power Supply Units, and Duplex Communications Units to be mounted, and enables online Unit replacement. This Backplane cannot be used in a Duplex CPU, Dual I/O Expansion System.

Note When using a Memory Card in Duplex Mode, mount it in the active CPU Unit. (Duplex Memory Card operation is not possible.) Duplex EM File Memory operation is possible.

CS1D CPU Rack for a Single CPU System

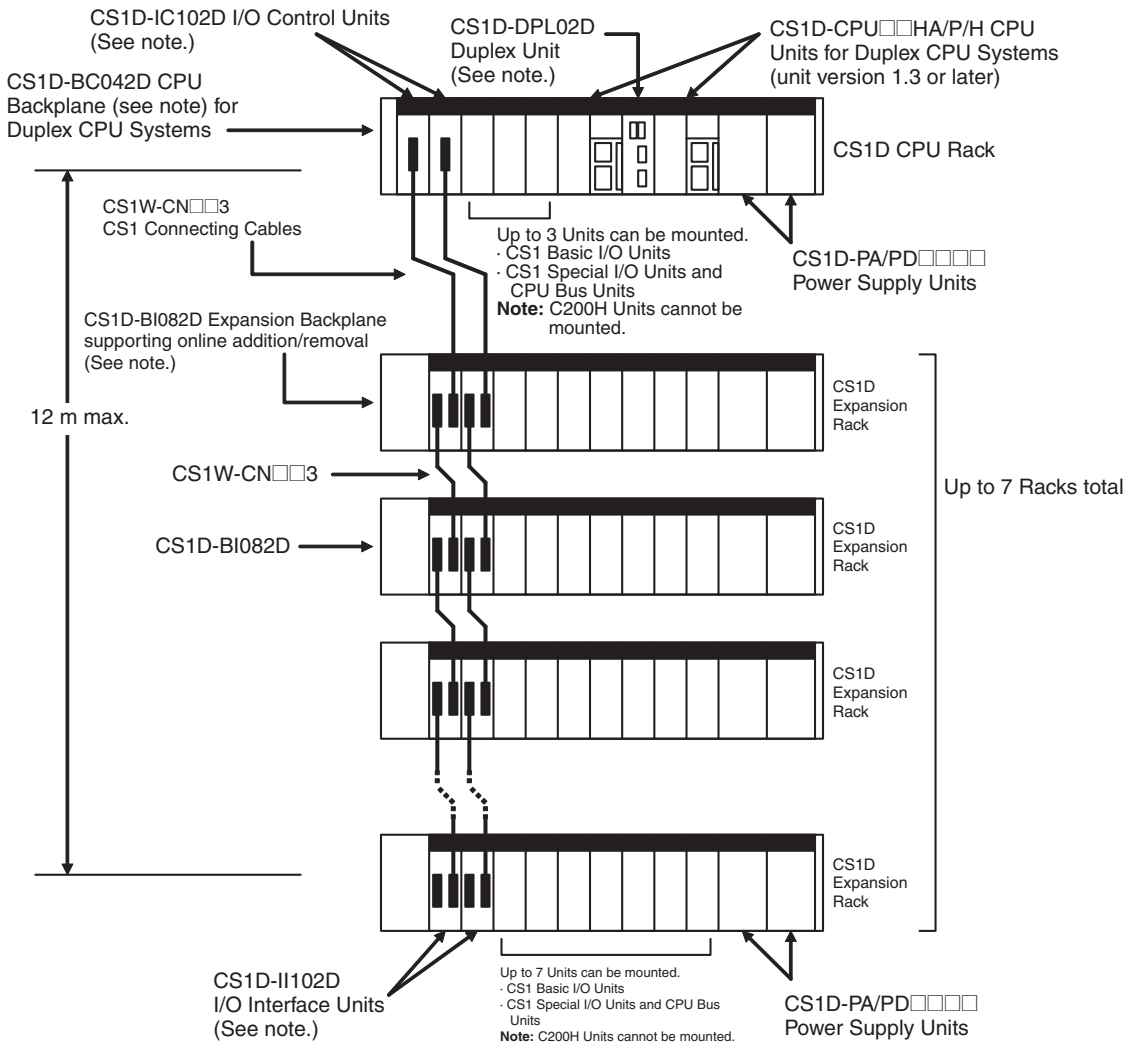


	Name	Model number	Contents
1	CPU Units for Single CPU Systems	CS1D-CPU44SA CS1D-CPU67SA CS1D-CPU42S CS1D-CPU44S CS1D-CPU65S CS1D-CPU67S	These CPU Units are designed especially for a Single CPU System. These CPU Units cannot be used in a Duplex CPU System.
2	CS1D Power Supply Units	CS1D-PA207R CS1D-PD024 CS1D-PD025	CS1D Power Supply Units are designed especially for a CS1D System. Two Power Supply Units are mounted to a CPU Rack, Expansion Rack, or Long-distance Expansion Rack for a duplex power supply configuration. When not configuring a duplex power supply, only one Power Supply Unit is mounted.
3	CPU Backplane for Single CPU Systems	CS1D-BC082S	This CPU Backplane is designed for a Single CPU System and does not support Duplex CPU Units. It does support Duplex Power Supply Units, Duplex Communications Units, and online Unit replacement.

CS1D CPU Rack and CS1D Expansion Racks for a Duplex CPU, Dual I/O Expansion System

The CS1D Expansion Racks in a Duplex CPU, Dual I/O Expansion System are specifically for this system configuration. Use the following Expansion Backplanes and I/O Interface Units, which are specifically for the Duplex CPU, Dual I/O Expansion System.

Name	Model number	Contents
Expansion Backplane Supporting Online Replacement (Especially for a Duplex CPU, Dual I/O Expansion System)	CS1D-BI082D	This Expansion Backplane is used in a Duplex CPU System, Dual I/O Expansion System. It allows the mounting of Duplex Power Supply Units and Duplex Communications Units, as well as online Unit replacement and online addition of Units and Backplanes. This Backplane cannot be used in a Duplex CPU, Single I/O Expansion System or Single CPU System. This Backplane cannot be used for a Long-distance Expansion Rack.
CS1D I/O Interface Unit (Especially for a Duplex CPU, Dual I/O Expansion System)	CS1D-II102D	These Units are required to create a Duplex CPU, Dual I/O Expansion System. The Connecting Cables can be duplexed by using two of these Units. These I/O Control Units cannot be used in a Duplex CPU, Single I/O Expansion System or Single CPU System.

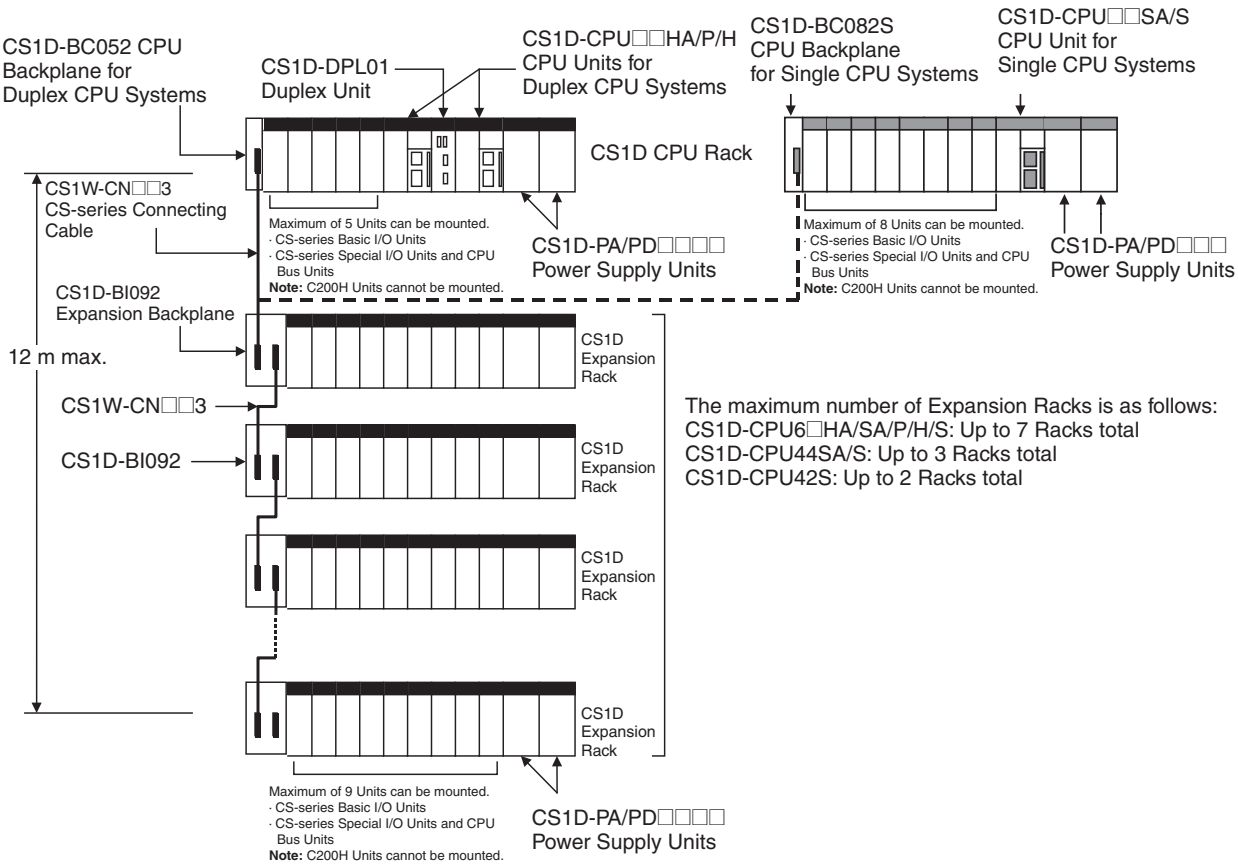


Note These Units are for use in a Duplex CPU, Dual I/O Expansion System only.

CS1D CPU Rack and CS1D Expansion Racks for a Duplex CPU, Single I/O Expansion System

The same kind of CS1D Expansion Rack is used in both the Duplex CPU Single I/O Expansion Systems and Single CPU Systems. Use the following CS1D Expansion Backplane, which is specifically for the CS1D System.

Name	Model number	Contents
CS1D Expansion Backplane (supports online Unit replacement)	CS1D-BI092	This Backplane must be used for any Expansion Racks in a CS1D Duplex System. It enables Duplex Power Supply Units, Duplex Communications Units, and online Unit replacement. It is also used as the Backplane for a Long-distance Expansion Rack. This Backplane cannot be used in a Duplex CPU, Dual I/O Expansion System.



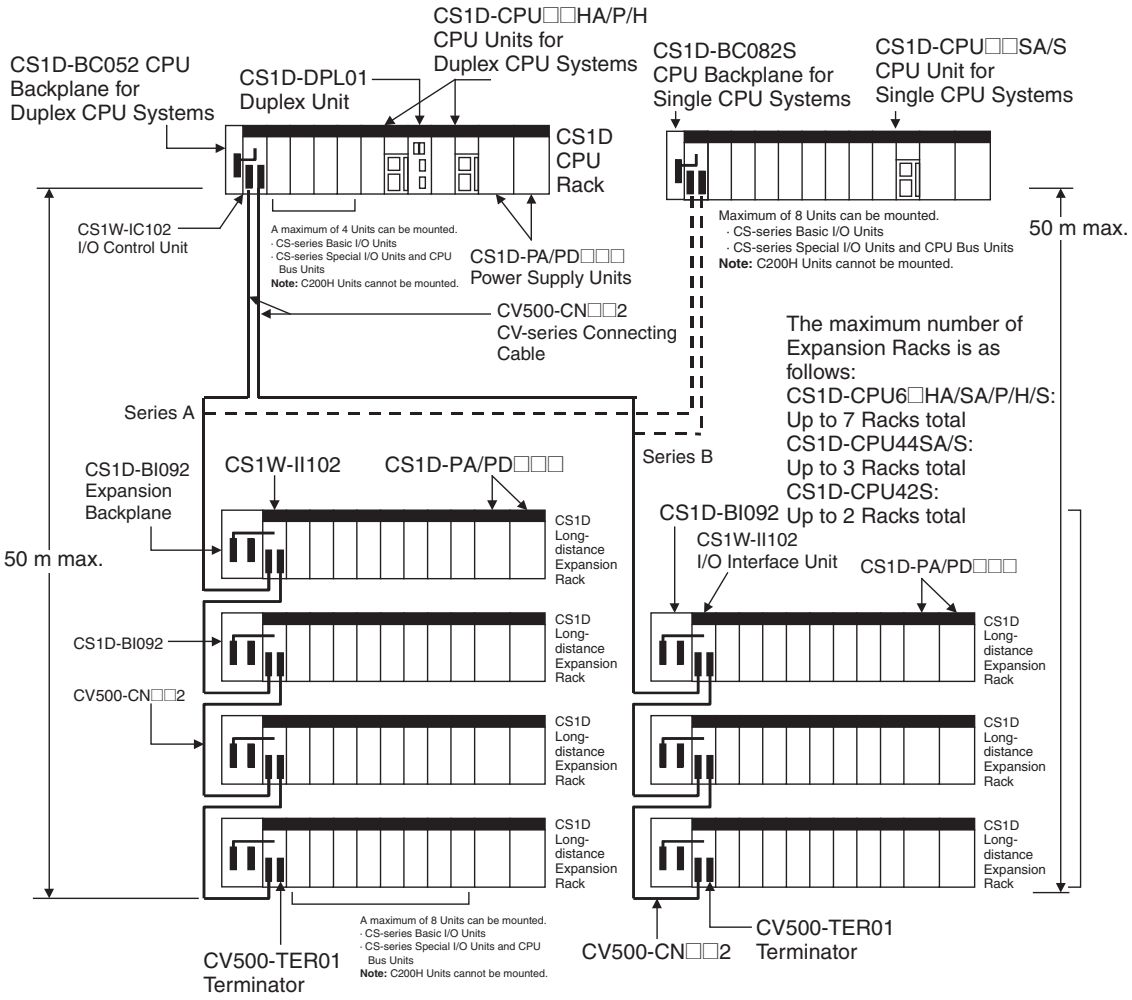
The maximum number of Expansion Racks is as follows:
CS1D-CPU6□HA/SA/P/H/S: Up to 7 Racks total
CS1D-CPU44SA/S: Up to 3 Racks total
CS1D-CPU42S: Up to 2 Racks total

CS1D CPU Rack + CS1D Long-distance Expansion Racks for a Duplex CPU Single I/O Expansion System or Single CPU System

The same Backplanes for Long-distance Expansion Racks are used in both Duplex CPU Single I/O Expansion Systems and Single CPU Systems. Use the following CS1D Expansion Backplane, which is specifically for the CS1D System.

Name	Model Number	Contents
CS1D Expansion Backplane (supports online Unit replacement)	CS1D-BI092	This Backplane must be used for any Long-distance Expansion Racks in a CS1D Duplex System. It enables duplex Power Supply Units, duplex Communications Units, and online Unit replacement.

Note An I/O Control Unit (CS1W-IC102) is mounted only to the CPU Rack.



SECTION 2
Specifications, Nomenclature, and Functions

This section provides the specifications, defines the nomenclature, and describes the functions of CS1D PLCs.

2-1 Specifications

2-1-1 Individual Specifications

CS1D CPU Units

Item	Specifications									
	Duplex CPU Systems				Single CPU Systems					
Model number	CS1D-CPU67HA	CS1D-CPU68HA	CS1D-CPU65H	CS1D-CPU67H	CS1D-CPU44SA	CS1D-CPU67SA	CS1D-CPU42S	CS1D-CPU44S	CS1D-CPU65S	CS1D-CPU67S
Number of I/O points (Number of Expansion Racks)	5,120 points (7 Racks)		5,120 points (7 Racks)		1,280 points (3 Racks)	5,120 points (7 Racks)	960 points (2 Racks)	1,280 points (3 Racks)	5,120 points (7 Racks)	
User program capacity (See note.)	250 Ksteps	400 Ksteps	60 Ksteps	250 Ksteps	30 Ksteps	250 Ksteps	10 Ksteps	30 Ksteps	60 Ksteps	250 Ksteps
Data Memory	32 Kwords		32 Kwords							
Extended Data Memory	32 Kwords x 13 banks E0_00000 to EC_32767	32 Kwords x 25 banks E0_00000 to E18_32767	32 Kwords x 3 banks E0_00000 to E2_32767	32 Kwords x 13 banks E0_00000 to EC_32767	32 Kwords x 1 bank E0_00000 to E0_32767	32 Kwords x 13 banks E0_00000 to EC_32767	32 Kwords x 1 bank E0_00000 to E0_32767		32 Kwords x 3 banks E0_00000 to E2_32767	32 Kwords x 13 banks E0_00000 to EC_32767
Current consumption (provided from CS1D Power Supply Unit)	5 V DC at 0.82 A		5 V DC at 0.82 A		5 V DC at 0.82 A		5 V DC at 0.79 A		5 V DC at 0.82 A	

Note The number of steps in a program is not the same as the number of instructions. Depending on the instruction, anywhere from one to seven steps may be required. For example, LD and OUT require one step each, but MOV(021) requires three steps. The total number of steps must not exceed the program capacity indicated in the above table. Refer to *9-5 Instruction Execution Times and Number of Steps* for the number of steps required for each instruction.

Duplex Unit Required for Duplex CPU System

Item	Specifications	
Model number	CS1D-DPL01 (for a Duplex CPU, Single I/O Expansion System)	CS1D-DPL02D (for a Duplex CPU, Dual I/O Expansion System)
Number mounted	One Duplex Unit.	One Duplex Unit.
Current consumption (provided from CS1D Power Supply Unit)	5 V DC, 0.55 A (with CS1D-BC052 CPU Backplane for Duplex CPU System)	5 V DC, 0.41 A (Duplex Unit only)

2-1-2 Duplex Specifications

System Configuration and Basic Functions

Item	Specifications	Reference
Functional equivalence of existing CS1-H CPU Units	The following CPU Units are equivalent in terms of basic functions (I/O points, program capacity, DM capacity, and instruction execution speed). CS1D-CPU68HA: No equivalent model CS1D-CPU67HA: Equivalent to CS1H-CPU67H. CS1D-CPU67SA: Equivalent to CS1H-CPU67H. CS1D-CPU44SA: Equivalent to CS1G-CPU44H. CS1D-CPU67H: Equivalent to CS1H-CPU67H. CS1D-CPU65H: Equivalent to CS1H-CPU65H. CS1D-CPU42S: Equivalent to CS1G-CPU42H. CS1D-CPU44S: Equivalent to CS1G-CPU44H. CS1D-CPU65S: Equivalent to CS1H-CPU65H. CS1D-CPU67S: Equivalent to CS1H-CPU67H. The instruction processing speed may vary depending on the model/instruction. Refer to *9-5 Instruction Execution Times and Number of Steps* for details.	*3-1-7 Duplex CPU System Restrictions* *Appendix E Precautions in Replacing CS1-H PLCs with CS1D PLCs*
Mountable Inner Boards	Duplex CPU Systems Inner Boards cannot be used in a Duplex CPU System except for in the Process-control CPU Units (CS1D-CPU□□P), which have a built-in CS1D-LCB05D Loop Control Board that cannot be removed. Single CPU Systems CS-series Inner Boards can be mounted in CPU Units for Single CPU Systems, but must be CS1W-LCCB01/05 Loop Control Boards with unit version 1.5 or later.	*1-2-1 CS1D Duplex Systems*
Mountable Units	CS-series Basic I/O Units, CS-series Special I/O Units, CS-series CPU Bus Units C200H Basic I/O Units, C200H Group-2 Multipoint I/O Units, and C200H Special I/O Units cannot be mounted.	*1-2-1 CS1D Duplex Systems*
System configuration	The following system configurations are possible: Duplex CPU, Dual I/O Expansion Systems In a this system, two CS1D CPU Units (CS1D-CPU□□HA/P/H, unit version 1.3 or later), two (or one) CS1D Power Supply Units, and one CS1D-DPL02D Duplex Unit are mounted to a CS1D-BC042D Backplane. Duplex CPU, Single I/O Expansion Systems In a Duplex CPU System, two CS1D CPU Units (CS1D-CPU□□HA/P/H), two (or one) CS1D Power Supply Units, and one CS1D-DPL01 Duplex Unit are mounted to a CS1D-BC052 Backplane. Single CPU Systems In a Single CPU System, one CS1D CPU Unit (C1D-CPU□□SA/S), two (or one) CS1D Power Supply Units, and one Duplex Unit are mounted to a CS1D CS1D-BC082S Backplane.	*1-2 System Configuration*

Item	Specifications			Reference
Duplex CS1D CPU Units (Supported only in Duplex CPU Systems)	Duplex Mode	A Duplex CPU System can be operated in either of the following two modes: Duplex Mode (DPL) The system operates with CS1D CPU Units and CS1D Power Supply Units in duplex status. Simplex Mode (SPL) The system operates with just a single CS1D CPU Unit.		*1-2-1 CS1D Duplex Systems*
	Operation of the two CS1D CPU Units in Duplex Mode	Hot standby method: One of the two CS1D CPU Units actually controls operations, and the other is on standby as a backup. The two CS1D CPU Units have the same I/O memory, and parameters (PLC Setup, I/O tables, etc.), and both run the same user's program. Their operation differ in the following points: The active CPU Unit executes I/O refreshing and all event servicing. The standby CPU Unit handles file accessing (read only) and FINS command execution event servicing (read only).		*3-1-1 Duplex CPU Systems*
	Operation switching errors	Power interruptions (CPU operation setting switch: NO USE), CPU errors, memory errors, program errors, cycle time overrun errors, FALS executions, fatal Inner Board errors	If any of the errors listed on the left occur in the active CPU Unit, stopping operation, the standby CPU Unit automatically switches to active status and takes over control. At the same time, the mode is switched to Simplex Mode. The CPU Unit where the error occurred can be replaced without stopping system operation. **Note** A fatal Inner Board error applies only to Process-control CPU Units.	*3-1-2 Errors Causing Operation to Switch to the Standby CPU Unit*
	Duplex errors	Duplex bus errors Duplex verification errors	If either of the errors listed on the left occurs in Duplex Mode, the active CPU Unit remains the same and operation is switched to Simplex Mode.	*3-1-3 Duplex Errors*
	Automatic recovery to duplex operation	After operation has been switched from Duplex Mode to Simplex Mode as a result of any of the operation switching errors listed above, operation is automatically returned to Duplex Mode when it is determined that the cause of the error has been cleared. Automatic recovery to duplex operation must first be enabled in the PLC Setup. (The recovery can be repeated up to ten times.)		*3-1-4 Automatic Recovery to Duplex Operation by Self-diagnosis*
	Hardware conditions for the two CS1D CPU Units in Duplex Mode	Identical models must be used for the two CS1D CPU Units.		*3-1-1 Duplex CPU Systems*
	Software conditions for the two CS1D CPU Units in Duplex Mode	The same user program areas must be used. The same parameter areas (PLC Setup, etc.) must be used. The same Inner Board data must be used (Process-control CPU Units only). Only the functions that can be executed by both CPU Units can be used (when the unit versions of the CPU Units are not the same).		*3-1-1 Duplex CPU Systems* *3-1-6 Duplex CPU Units with Different Unit Versions*
	CS1D CPU Unit online replacement	The CS1D CPU Unit where the error occurred can be replaced online by turning OFF the power to only that Unit (i.e., setting the CPU operation switch to NO USE).		*11-3 Replacing a CPU Unit*
	Duplex CPU compatible setting (CS1D-CPU67HA only)	The Duplex CPU Compatible Setting on the CS1D-CPU67HA enables the CPU Unit duplexity with the CS1D-CPU65H or CS1D-CPU67H.		*3-1-8 Duplex CPU Compatible Setting*

Item	Specifications		Reference
Duplex CS1D Power Supply Units	Operation with two CS1D Power Supply Units mounted	Power is supplied to the Backplane simultaneously by two CS1D Power Supply Units. (The load for each CS1D Power Supply Unit is approximately one half.)	*3-2 Duplex Power Supply Units*
	Operation when one CS1D Power Supply Unit breaks down	If one CS1D Power Supply Unit breaks down (i.e., if the power supply voltage drops), operation is continued using only the other one.	
Duplex Communications Units	When two Optical-ring Controller Link Units for duplex communications (H-PCF cable: CS1W-CLK12-V1/CLK13; GI cable: CS1W-CLK52-V1/CLK53) are mounted using the same node address and unit number, and a special cable is used to connect them, one of the Units will continue communications even if the other one breaks down (active-standby Units)		*Optical Ring Controller Link Units Operation Manual* (W370)
	Duplex Ethernet Units Two CS1D-ETN21D Ethernet Units are mounted. One is connected to the secondary communications line and the other to the primary communications line, thereby increasing reliability of the network (primary/secondary communications lines).		*3-3 Duplex Communications Units* *CS-series CS1D Ethernet Unit Operation Manual* (W430)
Duplex Connecting Cables	Two Connecting Cables are installed between the CPU Rack and Expansion Racks. If one Connecting Cable is removed or damaged, operation continues using the other cable.		*3-4 Duplex Connecting Cables* *11-6 Replacement of Expansion Units*
Online Unit replacement using a Programming Devices	Using the Programming Console, it is possible to mount or remove CS-series Basic I/O Units, CS-series Special I/O Units, and CS-series CPU Bus Units while the power is ON and the CPU Unit is operating in any mode (PROGRAM, MONITOR, or RUN).		*11-4 Online Replacement of I/O Units, Special I/O Units, and CPU Bus Units*
Unit Removal without a Programming Device	When Unit removal without a Programming Device is enabled in the PLC Setup, a Unit can be removed without using the CX-Programmer or a Programming Console. **Note** Unit removal without Programming Device is possible only in a CS1D Duplex System (Unit Ver. 1.2 or later). After the replacement Unit is mounted, the Online Replacement Completed Bit must be turned ON.		*6-1-3 Tab Pages for Duplex Settings in the PLC Setup* *11-4-5 Online Replacement without a Programming Device*
Removal/ Addition of Units without a Programming Device	If the *Removal/Addition of Units without a Programming Device* function is enabled in advance, Units can be removed and mounted without CX-Programmer or Programming Console operations. **Note** This function is possible only in a Duplex CPU, Dual I/O Expansion System.		*6-1-3 Tab Pages for Duplex Settings in the PLC Setup* *11-4-5 Online Replacement without a Programming Device*
Online Addition of Duplex Unit	If there is a Duplex Unit error, the Duplex Unit can be replaced during operation. The Duplex Unit in which the error occurred can be replaced after turning OFF power to the Unit by setting the DPL USE/NO USE Switch to *NO USE*. **Note** This function is possible only in a Duplex CPU, Dual I/O Expansion System. The PLC operates in simplex mode while the Duplex Unit is being replaced.		*11-7 Replacing the Duplex Unit*
Online Addition of Units and Backplanes	A new Basic I/O Unit, Special I/O Unit, or Expansion Backplane can be added during operation. to an existing Rack. An operating Rack can be expanded without stopping the Rack. **Note** This function is possible only in a Duplex CPU, Dual I/O Expansion System or Duplex CPU, Single I/O Expansion System with CPU Units that have unit version 1.2 or later. Backplanes can be replaced only in a Duplex CPU, Dual I/O Expansion System.		*7-7 Online Addition of Units and Backplanes*
Securing Expansion Rack Cables	Secure cables help prevent Expansion Rack Cables from being disconnected accidentally.		*5-2-6 I/O Connecting Cables*

Specifications with Application Restrictions

Item	Specifications		Reference
Programming Device operating restrictions	CX-Programmer	CX-Programmer Ver. 3.□ or lower: • The Duplex CPU System uses the CS1D-CPU□□H, so select “CS1H-H” as the device type. • Not supported in CS1D-CPU□□HA. • This version does not support Single CPU Systems. CX-Programmer Ver. 4.0 or higher: • The Duplex CPU System uses the CS1D-CPU□□H, so select “CS1D-H” or “CS1H-H” as the device type. • In CS1D-CPU□□HA, select the PLC model: "CS1D-H." **Note** CS1D-CPU□□HA requires CX-Programmer Ver. 9.7 or later. • The Single CPU System uses the CS1D-CPU□□SA/S, so select “CS1D-S” as the device type. Cable connection: Connect to the peripheral port or RS-232C port of the active CPU Unit. **Note** If a CX-Programmer is connected to the standby CPU Unit in a Duplex CPU System, write processing from the CX-Programmer cannot be executed.	*2-6-2 Precautions when Connecting Programming Devices to Duplex CPU Systems*
	Programming Console (Duplex CPU Systems only)	Cable connection: Connect to peripheral port of active CPU Unit. If a Programming Console is connected to the standby CPU Unit, write processing from the Programming Console cannot be executed.	
Applications constantly connected to RS-232C port in Duplex CPU Systems	When a constant monitoring system, such as a PT or personal computer application, is connected to the CPU Unit’s RS-232C port, an RS-232C/RS-422 Adapter can be used to connect to both the active and standby CS1D CPU Units. Set the standby CPU Unit’s RS-232C port setting in the PLC Setup so that it cannot be used independently.		*6-2-11 CPU Duplex Tab Page* *Appendix F Connecting to the RS-232C Port on the CPU Unit*
Restrictions on Memory Card functions (Duplex CPU Systems only)	When writing to a Memory Card, the same data is written to not only the Memory Card mounted in the active CPU Unit, but also to the one mounted in the standby CPU Unit. **Note** In the PLC Setup, duplex operation must be enabled for Memory Cards. **Note** No processing is executed during duplex initialization to match the data on the Memory Cards mounted in the active and standby CPU Units even if the data is not the same. Therefore, before enabling duplex operation for Memory Cards, make sure that the contents are the same for both of the Memory Cards. **Note** When EM File Memory is set for duplex operation, processing is executed to match the contents of EM File Memory in both CPU Units. It is not necessary to enable duplex operation for Memory Cards in the PLC Setup.		*2-5-1 File Memory Functions in Duplex CPU Systems*

Item	Specifications		Reference
Restrictions on interrupts (Duplex CPU Systems only)	The CS1D CPU Units for Duplex CPU Systems do not support any interrupt functions. Power OFF interrupt tasks, scheduled interrupt tasks, I/O interrupt tasks, and external interrupt tasks cannot be used in either Duplex or Simplex Mode. Interrupt control instructions (MSKS, MSKR, and CLI) are executed as NOPs.		*3-1-7 Duplex CPU System Restrictions* *Appendix E Precautions in Replacing CS1-H PLCs with CS1D PLCs*
Restrictions on I/O refresh methods (Duplex CPU Systems only)	No restrictions.	Cyclic refreshing Refreshing by I/O refresh instruction (IORF(097)) Refreshing by CPU Bus Unit immediate refresh instruction (DLINK(226))	
	Cannot be used in Duplex CPU Systems (disabled).	Immediate refresh option "!" Immediate refresh option "!" will be not be used even if it is specified.	
Restrictions on CPU processing modes (Duplex CPU Systems only)	Only Normal Mode can be used in Duplex CPU Systems. Parallel Processing Mode and Peripheral Servicing Priority Mode cannot be used.		
Restrictions on background execution (Duplex CPU Systems only)	Background execution of text string instructions, table data instructions, and data shift instructions cannot be used in Duplex CPU Systems.		
Accuracy of timer instructions in Duplex CPU Systems	± (10 ms + cycle time) If a timer instruction is being executed when operation is switched from duplex to simplex, the error in the timer in the first cycle after switching may exceed the normal time. In this case, the timer accuracy will be as follows: TIM, TIMX, TIMH(015), TIMHX(551), TTIM(087), TTIMX(555), TIML(542), TIMLX(553), MTIM(543), MTIMX(554), TIMW(813), TIMWX(816), TMHW(815), TMHWX(817): ± (10 ms + cycle time) ± 10 ms or less TMHH(540), TMHHX(552): ± (10 ms + cycle time) ± 20 ms or less		
PV refreshing in Duplex CPU Systems during timer instructions in jumped program sections or in stopped block program section (Differences from CS1-H.)	TIM, TIMX, TIMH(015), TIMHX(551), TMHH(540), TMHHX(552), TTIM(087), TTIMX(555): The timer PV is not refreshed when the timer instruction is jumped for JMP, CJMP, or CJPN-JME. The PV will be refreshed for the entire period it was jumped the next time it is executed (i.e., the next time it is not jumped). (With CS1-H CPU Units, the PV for these timers were refreshed even when jumped.)		*3-1-7 Duplex CPU System Restrictions* *Appendix E Precautions in Replacing CS1-H PLCs with CS1D PLCs*
	TIMW(813), TIMWX(816), TMHW(815), TMHWX(817): When the input condition for BPRG is OFF, or when the block program is temporarily stopped by BPPS, the timer PV is not refreshed. (With the CS1-H CPU Units, the PV for these timers were refreshed each cycle.)		
Clock function in Duplex CPU Systems	Synchronized with active CPU Unit.		

2-1-3 Common Specifications other than Duplex Specifications

Item		Specifications	Reference
Control method		Stored program	---
I/O control method		Cyclic scan and immediate processing (by IORF only) are both supported. **Note** Immediate refresh cannot be used in CS1D Duplex-CPU Systems. It can be used in Single CPU Systems.	---
Programming		Ladder diagram Structured text (ST) Sequential function chart (SFC) Instruction list (IL) **Note** ST and SFC can be used in unit version 4.0 or later	---
CPU processing mode		Duplex CPU Systems: Normal Mode only **Note** Parallel Processing Mode and Peripheral Servicing Priority Mode cannot be used. Single CPU Systems: Normal Mode, Parallel Processing with Asynchronous Memory Access Mode, Parallel Processing with Synchronous Memory Access Mode, and Peripheral Servicing Priority Mode can be used.	---
Instruction length		1 to 7 steps per instruction	*9-5 Instruction Execution Times and Number of Steps*
Number of ladder instructions		Duplex CPU Systems: Approx. 440 (3-digit function codes) Single CPU Systems: Approx. 470	---
Instruction execution times	Basic instructions	0.02 μs or more	*9-5 Instruction Execution Times and Number of Steps*
	Special instructions	0.06 μs or more	
Overhead processing time		Duplex CPU Systems: 1.9 ms Single CPU Systems: 0.5 ms (Normal Mode) 0.4 ms (Parallel Processing Mode)	*9-4-2 Cycle Time Overview*
Number of Expansion Racks		7 max. (CS1D Expansion Racks) (C200H Expansion I/O Racks and SYSMAC BUS Remote I/O Slave Racks cannot be connected.)	*2-2-2 Expansion Racks*
Number of Tasks	Duplex CPU Systems	288 (cyclic tasks: 32; extra cyclic tasks: 256) Extra cyclic tasks can be executed each cycle, just like cyclic tasks, making a total of 288 tasks that can be executed each cycle. Cyclic tasks are executed each cycle and are controlled with TKON(820) and TKOF(821) instructions.	*Programming Manual* (W394)
	Single CPU Systems	288 (cyclic tasks: 32; interrupt tasks: 256) Interrupt tasks can be executed each cycle, just like cyclic tasks, making a total of 288 tasks that can be executed each cycle. Cyclic tasks are executed each cycle and are controlled with TKON(820) and TKOF(821) instructions. The following 4 types of interrupt tasks are supported: Power OFF interrupt task (1 max.), scheduled interrupt tasks (2 max.), I/O interrupt tasks (32 max.), and external interrupt tasks (256 max.).	
Function blocks (Supported in unit version 4.0 or later)		Languages in function block definitions: Ladder language, Structured Text	Refer to *CX-Programmer CS/CJ Series Operation Manual: Function Blocks* (No. W338)

<table>
<tr><th colspan="2">Item</th><th>Specifications</th><th colspan="2">Reference</th></tr>
<tr><td colspan="2">Starting subroutines from multiple starts</td><td>Supported (by global subroutines).</td><td colspan="2">Programming Manual (W394)</td></tr>
<tr><td rowspan="5">CIO (Core I/O) Area</td><td>I/O Area</td><td>5,120: CIO 000000 to CIO 031915 (320 words from CIO 0000 to CIO 0319)
The setting of the first word can be changed from the default (CIO 0000) so that CIO 0000 to CIO 0999 can be used.
I/O bits are allocated to Basic I/O Units (CS-series Basic I/O Units).</td><td>Input bits
Output bits
8-3 I/O Area</td><td rowspan="5">The CIO Area can be used as work bits if the bits are not used as shown here.</td></tr>
<tr><td>Data Link Area</td><td>3,200 (200 words): CIO 10000 to CIO 119915 (words CIO 1000 to CIO 1199)
Link bits are used for data links and are allocated to Units in Controller Link Systems.</td><td>8-5 Data Link Area</td></tr>
<tr><td>CPU Bus Unit Area</td><td>6,400 (400 words): CIO 150000 to CIO 189915 (words CIO 1500 to CIO 1899)
CPU Bus Unit bits can be used to store the operating status of CPU Bus Units.
(25 words per Unit, 16 Units max.)</td><td>8-6 CPU Bus Unit Area</td></tr>
<tr><td>Special I/O Unit Area</td><td>15,360 (960 words): CIO 200000 to CIO 295915 (words CIO 2000 to CIO 2959)
Special I/O Unit bits can be allocated to CS-series Special I/O Units.
(10 words per Unit, 96 Units max.)</td><td>8-8 Special I/O Unit Area</td></tr>
<tr><td>Inner Board Area (Process-control CPU Units and Single CPU Systems only)</td><td>1,600 (100 words): CIO 190000 to CIO 199915 (words CIO 1900 to CIO 1999)
Inner Board bits can be allocated to Inner Boards. (100 I/O words max.)</td><td>8-7 Inner Board Area</td></tr>
<tr><td>CIO (Core I/O) Area, continued</td><td>CS-series DeviceNet Area</td><td>9,600 (600 words): CIO 320000 to CIO 379915 (words CIO 3200 to CIO 3799)
CS-series DeviceNet Area bits are allocated to Slaves according to CS1W-DRM21(-V1) DeviceNet Unit remote I/O communications.
<table><tr><td>Fixed Allocations 1</td><td>Output: 3200 to 3263
Input: 3300 to 3363</td></tr><tr><td>Fixed Allocations 2</td><td>Output: 3400 to 3463
Input: 3500 to 3563</td></tr><tr><td>Fixed Allocations 3</td><td>Output: 3600 to 3663
Input: 3700 to 3763</td></tr></table>The following words are allocated in the Master even when fixed allocations are used for the remote I/O communications Slave functions of a CS-series DeviceNet Unit (CS1W-DRM21(-V1)).
<table><tr><th>Item</th><th>To Slave</th><th>To Master</th></tr><tr><td>Fixed Allocations 1</td><td>Output: 3370</td><td>Input: 3270</td></tr><tr><td>Fixed Allocations 2</td><td>Output: 3570</td><td>Input: 3470</td></tr><tr><td>Fixed Allocations 3</td><td>Output: 3770</td><td>Input: 3670</td></tr></table></td><td>8-4 CS-series DeviceNet Area</td><td></td></tr>
</table>

Item		Specifications	Reference
CIO (Core I/O) Area, Work Areas	Internal I/O Area	4,800 (300 words): CIO 120000 to CIO 149915 (words CIO 1200 to CIO 1499) 37,504 (2,344 words): CIO 380000 to CIO 614315 (words CIO 3800 to CIO 6143) These bits in the CIO Area are used as work bits in programming to control program execution. They cannot be used for external I/O.	*8-3 I/O Area*
	Work Area	8,192 bits (512 words): W00000 to W51115 (W000 to W511) These bits are used to control the programs only. (I/O from external I/O is not possible.) When using work bits in programming, use the bits in the Work Area first before using bits from other areas.	*8-9 Work Area*
Holding Area		8,192 bits (512 words): H00000 to H51115 (H000 to H511) Holding bits are used to control the execution of the program, and maintain their ON/OFF status when the PLC is turned OFF or the operating mode is changed. 16,384 bits (1024 CH): H51200 to 153515 (H512 to H1535 CH) Supported in unit version 4.0 or later. These are Function Block Holding Area words. They can be set only in the FB instance area (internally-assigned range of variables).	*8-10 Holding Area*
Auxiliary Area		Read only: 7,168 bits (448 words): A00000 to A44715 (words A000 to A447) Read/write: 8,192 bits (512 words): A44800 to A95915 (words A448 to A959) Auxiliary bits are allocated for specific functions.	Functions: *8-11 Auxiliary Area* Addresses: *Appendix B Auxiliary Area Allocations*
Temporary Relay (TR) Area		16 bits (TR0 to TR15) Temporary bits are used to temporarily store the ON/OFF execution conditions at program branches.	*8-12 TR (Temporary Relay) Area*
Timer Area		4,096: T0000 to T4095 (used for timers only)	*8-13 Timer Area*
Counter Area		4,096: C0000 to C4095 (used for counters only)	*8-14 Counter Area*
Data Memory (DM) Area		32 Kwords: D00000 to D32767 Used as a general-purpose data area for reading and writing data in word units (16 bits). Words in the DM Area maintain their status when the PLC is turned OFF or the operating mode is changed. Special I/O Unit DM Area: D20000 to D29599 (100 words × 96 Units) Used to set parameters for Special I/O Units. CPU Bus Unit DM Area: D30000 to D31599 (100 words × 16 Units) Used to set parameters for CPU Bus Units. Inner Board DM Area: D32000 to D32099 Used to set parameters for Inner Boards (Single CPU Systems or Process-control CPU Units only).	*8-15 Data Memory (DM) Area*

Item	Specifications	Reference
Extended Data Memory (EM) Area	32 Kwords per bank, 25 banks max.: E0_00000 to E18_32767 max. (Not available on some CPU Units.) Used as a general-purpose data area for reading and writing data in word units (16 bits). Words in the EM Area maintain their status when the PLC is turned OFF or the operating mode is changed. The EM Area is divided into banks, and the addresses can be set by either of the following methods. Changing the current bank using the EMBC(281) instruction and setting addresses for the current bank. Setting bank numbers and addresses directly. EM data can be stored in files by specifying the number of the first bank.	*8-16 Extended Data Memory (E18) Area*
Index Registers	IR0 to IR15 Store PLC memory addresses for indirect addressing. One register is 32 bits (2 words). Index registers can be set to be shared by all tasks or to be used independently by each task.	*8-17 Index Registers*
Data Registers	DR0 to DR15 Used to offset the PLC memory addresses in Index Registers when addressing words indirectly. Data registers can be set to be shared by all tasks or to be used independently by each task.	*8-18 Data Registers*
Task Flags	32 (TK0000 to TK0031) Task Flags are read-only flags that are ON when the corresponding cyclic task is executable and OFF when the corresponding task is not executable or in standby status.	*8-19 Task Flags*
Trace Memory	4,000 words (trace data: 31 bits, 6 words)	*Programming Manual* (W394)
File Memory	Memory Cards: Compact flash memory cards can be used (MS-DOS format). EM file memory: The EM Area can be converted to file memory (MS-DOS format).	*Programming Manual* (W394)

Functions

Function	Specifications	Reference
Constant cycle time	1 to 32,000 ms (Unit: 1 ms) **Note** When Parallel Processing Mode is used in a Single CPU System, the cycle time for executing instructions is constant.	Cycle time: *9-4 Computing the Cycle Time* Constant cycle time: *Programming Manual* (W394)
Cycle time monitoring	Possible (Unit stops operating if the cycle is too long): 10 to 40,000 ms (Unit: 10 ms) **Note** When Parallel Processing Mode is used in a Single CPU System, the cycle time for executing instructions is monitored. CPU Unit operation will stop if the peripheral servicing cycle time exceeds 2 s (fixed).	Cycle time: *9-4 Computing the Cycle Time* Constant cycle time: *Programming Manual* (W394)
I/O refreshing	Duplex CPU Systems: Cyclic refreshing, refreshing by IORF (097). Single CPU Systems: Cyclic refreshing, refreshing by IORF (097), immediate refreshing IORF(097) refreshes I/O bits allocated to Basic I/O Units and Special I/O Units. The CPU BUS UNIT I/O REFRESH (DLNK(226)) instruction can be used to execute cyclic refreshing of bits allocated to CPU Bus Units.	I/O refreshing: *9-4 Computing the Cycle Time* I/O refreshing method: *Programming Manual* (W394)

Function	Specifications		Reference
Timing of special refreshing for CPU Bus Units	Data links for Controller Link Units and SYSMAC LINK Units, remote I/O for DeviceNet Units, and other special refreshing for CPU Bus Units is performed at the I/O refresh period and when the CPU BUS UNIT I/O REFRESH (DLNK(226)) instruction is executed.		*9-1-3 I/O Refreshing and Peripheral Servicing*
I/O memory holding when changing operating modes	Depends on the ON/OFF status of the IOM Hold Bit in the Auxiliary Area.		I/O memory: *SECTION 8 Memory Areas* Holding memory areas when changing operating modes: *Programming Manual* (W394) Holding I/O memory: *8-2-3 Data Area Properties*
Load OFF	All outputs on Output Units can be turned OFF when the CPU Unit is operating in RUN, MONITOR, or PROGRAM mode.		*Programming Manual* (W394)
Input response time setting	Time constants can be set for inputs from Basic I/O Units. The time constant can be increased to reduce the influence of noise and chattering or it can be decreased to detect shorter pulses on the inputs.		Input response time: *9-4-8 I/O Response Time* Input response settings: *Programming Manual* (W394)
Startup mode setting	Supported The CPU Unit will start in RUN mode if the PLC Setup is set to use the Programming Console mode (default) and a Programming Console is not connected.		*Programming Manual* (W394) *6-1 Overview of PLC Setup*
Flash memory	The user program and Parameter Area data (e.g., PLC Setup) are always backed up automatically in flash memory.		---
Memory Card functions (Accessed only for Memory Card mounted in active CPU Unit of Duplex CPU System.)	Automatically reading programs (autoboot) from the Memory Card when the power is turned ON.	Supported.	*2-5 File Memory* *Programming Manual* (W394)
	Program replacement during PLC operation.	Supported.	*Programming Manual* (W394)
	Format in which data is stored in Memory Card	User program: Program file format PLC Setup and other parameters: Data file format I/O memory: Data file format (binary format), text format, or CSV format (except preversion-1 CS1 CPU Units)	*Programming Manual* (W394)
	Functions for which Memory Card read/write is supported	User program instructions, Programming Devices (including Programming Consoles), Host Link computers, AR Area control bits, simple backup operation	*Programming Manual* (W394)
Filing	Memory Card data and the EM (Extended Data Memory) Area can be handled as files.		*Programming Manual* (W394)
Debugging	Control set/reset, differential monitoring, data tracing (scheduled, each cycle, or when instruction is executed), storing location generating error when a program error occurs		*Programming Manual* (W394)
Online editing	User programs can be overwritten in program-block units when the CPU Unit is in MONITOR or PROGRAM mode. This function is not available for block programming areas. With the CX-Programmer, more than one program block can be edited at the same time.		*Programming Manual* (W394)
Program protection	Overwrite protection: Set using DIP switch. Copy protection: Password set using Programming Device.		*Programming Manual* (W394)

Function	Specifications	Reference
Error check	User-defined errors (i.e., user can define fatal errors and non-fatal errors) The FPD(269) instruction can be used to check the execution time and logic of each programming block. FAL and FALS instructions can be used with the CS1-H CPU Units to simulate errors.	Failure diagnosis: *Programming Manual* (W394) Fatal and nonfatal errors: *SECTION 10 Troubleshooting* User-defined errors: *Programming Manual* (W394)
Error log	Up to 20 errors are stored in the error log. Information includes the error code, error details, and the time the error occurred. The CPU Unit can be set so that user-defined FAL errors are not stored in the error log.	*Programming Manual* (W394)
Serial communications	Built-in peripheral port: Programming Device (including Programming Console) connections, Host Links, NT Links Built-in RS-232C port: Programming Device (excluding Programming Console) connections, Host Links, no-protocol communications, NT Links	*2-6 Programming Devices* *Programming Manual* (W394)
	Serial Communications Board (sold separately): Protocol macros, Host Links, NT Links	
Clock	Provided on all models. Accuracy: CS1D-CPU□□H/P/S: Monthly difference ± 180 seconds (Ambient temperature 55 °C) Monthly difference ± 30 seconds (Ambient temperature 25 °C) Monthly difference ± 70 seconds (Ambient temperature 0 °C) CS1D-CPU□□HA/SA: Monthly difference -3.0 minutes to 0.5 minutes (Ambient temperature 55°C) ± 1.5 minutes (Ambient temperature: 25°C) -3 minutes to +1 minute (Ambient temperature 0°C) **Note a)** The accuracy varies with the temperature. **b)** Used to store the time when power is turned ON and when errors occur.	*Programming Manual* (W394)
Power OFF detection time	10 to 25 ms (AC power supply) 2 to 5 ms (DC power supply)	*9-3 Power OFF Operation*
Power OFF detection delay time	0 to 10 ms (user-defined, default: 0 ms)	*Programming Manual* (W394)
Memory protection	Held Areas: Holding bits, contents of Data Memory and Extended Data Memory, and status of the counter Completion Flags and present values. **Note** If the IOM Hold Bit in the Auxiliary Area is turned ON, and the PLC Setup is set to maintain the IOM Hold Bit status when power to the PLC is turned ON, the contents of the CIO Area, the Work Area, part of the Auxiliary Area, timer Completion Flags and PVs, Index Registers, and the Data Registers will be saved.	*8-2-3 Data Area Properties*
Sending commands to a Host Link computer	FINS commands can be sent to a computer connected via the Host Link System by executing Network Communications Instructions from the PLC.	---
Remote programming and monitoring	Host Link communications can be used for remote programming and remote monitoring through a Controller Link System or Ethernet network.	*Programming Manual* (W394)

Function	Specifications	Reference
Multiple-level communications	Duplex CPU Systems: 3 levels Single CPU Systems: 8 levels **Note** Communications are possible across up to eight levels only for the Controller Link and Ethernet networks (and the CX-Integrator or CX-Net in CX-Programmer version 4.0 or higher is required to set the routing tables). Communications are possible across only up to three communications levels for the SYSMAC LINK, DeviceNet, and FL-net networks.	---
Storing comments in CPU Unit	I/O comments can be stored in the Memory Card or EM file memory, or in the comment memory in the CPU Unit flash memory (unit version 4.0 or later).	I/O comments: *CX-Programmer User Manual* Storing comments in CPU Units: *Programming Manual* (W394)
Program check	Program checks are performed at the beginning of operation for items such as no END instruction and instruction errors. CX-Programmer can also be used to check programs.	*Programming Manual* (W394)
Control output signals	RUN output: An internal contact turns ON when the CPU Unit is operating in RUN or MONITOR mode. These terminals are provided only on CS1D-PA207R Power Supply Units.	*Programming Manual* (W394)
Battery service life	Battery Set: CS1W-BAT01	*11-2-1 Battery Replacement*
Self-diagnostics	CPU errors (watchdog timer), I/O verification errors, I/O bus errors, memory errors, and battery errors	*10-2-4 Errors and Troubleshooting*
Other functions	Storage of number of times power has been interrupted. (Stored in A514.)	*9-3 Power OFF Operation*

2-1-4 General Specifications

Item	Specifications		
CS1D Power Supply Unit	CS1D-PA207R	CS1D-PD024	CS1D-PD025
Power supply voltage	100 to 120 V AC/200 to 240 V, 50/60 Hz	24 V DC	24 V DC
Operating voltage range	85 to 132 V AC/170 to 264 V	19.2 to 28.8 V DC	19.2 to 28.8 V DC
Power consumption	150 VA max.	40 W max.	60 W max.
Inrush current	100 to 120 V AC: 30 A max. (cold start at normal temperatures); 8 ms max. 200 to 240 V AC: 40 A max. (cold start at normal temperatures); 8 ms max. (See note 1.)	30 A max.	30 A max.
Power supply output capacity	5 V DC, 7 A (including the CPU Unit power supply)	5 V DC, 4.3 A (including the CPU Unit power supply)	5 V DC, 5.3 A (including the CPU Unit power supply)
	26 V DC, 1.3 A	26 V DC, 0.56 A	26 V DC, 1.3 A
	Total: 35 W max.	Total: 28 W max.	Total: 40 W max.
Power supply output terminal	Not provided.	Not provided.	Not provided.

Item		Specifications		
CS1D Power Supply Unit		CS1D-PA207R	CS1D-PD024	CS1D-PD025
RUN output (See note 3.)	Contact configuration	SPST-NO	Not provided.	Not provided.
	Switch capacity	240 V AC, 2A (resistive load) 120 V AC, 0.5 A (induction load) 24 V DC, 2A (resistive load) 24 V DC, 2 A (induction load)		
Insulation resistance		20 MΩ min. (at 500 V DC) between AC external and GR terminals (See note 2.)	20 MΩ min. (at 500 V DC) between DC external and GR terminals (See note 2.)	20 MΩ min. (at 500 V DC) between DC external and GR terminals (See note 2.)
Dielectric strength		2,300 V AC 50/60 Hz for 1 min between AC external and GR terminals (See note 2.) Leakage current: 10 mA max.	1,000 V AC 50/60 Hz for 1 min between DC external and GR terminals (See note 2.) Leakage current: 10 mA max.	1,000 V AC 50/60 Hz for 1 min between DC external and GR terminals (See note 2.) Leakage current: 10 mA max.
		1,000 V AC 50/60 Hz for 1 min between AC external and GR terminals (See note 2.) Leakage current: 10 mA max.		
Noise immunity		2 kV on power supply line (conforming to IEC61000-4-4)		
Vibration resistance		10 to 57 Hz, 0.075-mm amplitude, 57 to 150 Hz, acceleration: 9.8 m/s^2 in X, Y, and Z directions for 80 minutes (Time coefficient: 8 minutes × coefficient factor 10 = total time 80 min.)		
Shock resistance		147 m/s^2 3 times each in X, Y, and Z directions (according to JIS 0041)		
Ambient operating temperature		0 to 55°C		
Ambient operating humidity		10% to 90% (with no condensation)		
Atmosphere		Must be free from corrosive gases.		
Ambient storage temperature		–20 to 75°C (excluding battery)		
Grounding		Less than 100 Ω		
Enclosure		Mounted in a panel.		
Weight		Refer to *SECTION 2 Specifications, Nomenclature, and Functions*.		
CPU Rack dimensions		5 slots (CS1D-BC052): 505 × 130 × 153 mm (W x H x D) (See note 4.)		
Expansion Rack dimensions		9 slots (CS1D-BI092): 505 × 130 × 153 mm (W x H x D) (See note 4.)		
Safety standards		Conforms to cULus, NK, Lloyd's, and EU Directives.		

Note

1. The above inrush current value is for a cold start at normal temperatures. The inrush current circuit for this power supply includes a thermistor element (for current suppression at low temperatures). If the ambient temperature is too high, the thermistor element will not be cool enough, so the above inrush current value may be exceeded (by as much as double the value shown). Provide a sufficient margin by taking this into consideration along with breaking or detection characteristics when selecting fuses and breakers for external circuits.
2. Disconnect the CS1D Power Supply Unit's LG terminal from the GR terminal when testing insulation and dielectric strength. Testing the insulation and dielectric strength with the LG terminal and the GR terminals connected will damage internal circuits in the CPU Unit.
3. Supported when mounted to a Backplane.

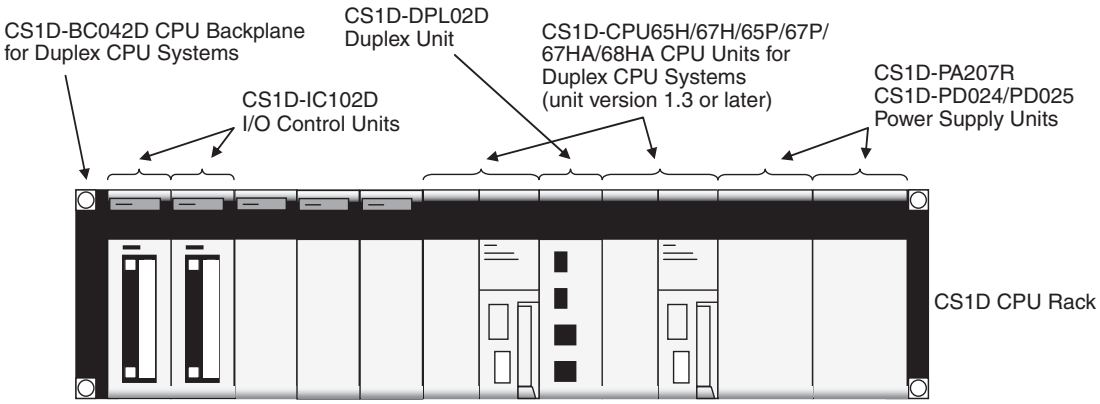
4. The depth (D) is 123 mm for the CS1D-PD024.

2-2 Configuration Devices

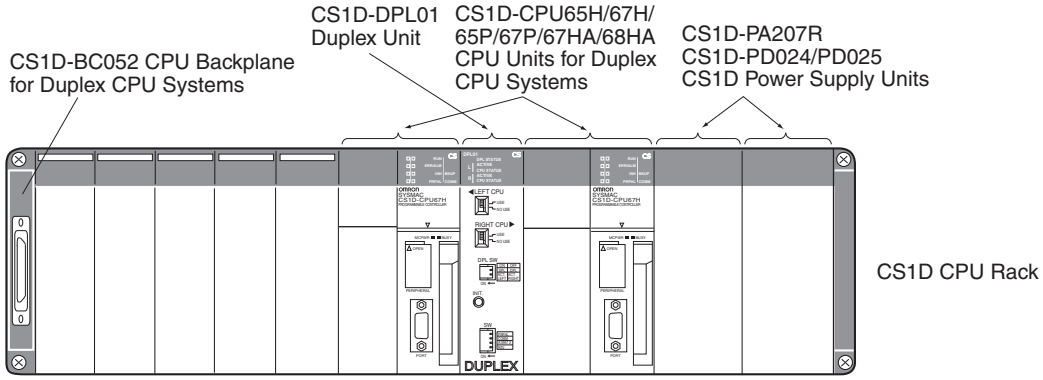
2-2-1 CPU Rack

Expansion Patterns

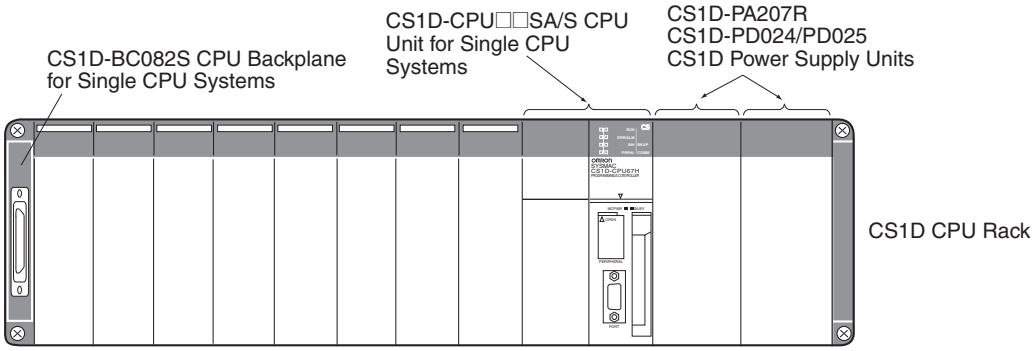
Duplex CPU, Dual I/O Expansion Systems



Duplex CPU, Single I/O Expansion Systems



Single CPU Systems



Rack Configurations

Rack name	Devices	Remarks
CPU Rack for Duplex CPU, Dual I/O Expansion Systems	CPU Units for Duplex CPU Systems (unit version 1.3 or later) (See note 1.)	Two Units (or one) are required.
	CS1D Power Supply Units	Two Units (or one) are required.
	CPU Backplane for Duplex CPU Systems (See note 2.)	One Unit is required.
	Duplex Unit (See note 2.)	One Unit is required.
	CS1D I/O Control Units (See note 2.)	Two Units (or one) are required for expansion.
	Memory Card	Install a Memory Card in the active CPU Unit as required.
CPU Rack for Duplex CPU, Single I/O Expansion Systems	CPU Units for Duplex CPU Systems (See note 1.)	Two Units (or one) are required.
	CS1D Power Supply Units	Two Units (or one) are required.
	CPU Backplane for Duplex CPU Systems (See note 3.)	One Unit is required.
	Duplex Unit (See note 3.)	One Unit is required.
	Memory Card	Install a Memory Card in the active CPU Unit as required.
CPU Rack for Single CPU Systems	CPU Unit for Single CPU Systems (See note 4.)	One Unit is required.
	CS1D Power Supply Units	Two Units (or one) are required.
	CPU Backplane for Single CPU Systems (See note 4.)	One Unit is required.
	Duplex Inner Boards	Install an Inner Board as required.
	Memory Card	Install a Memory Card as required.

Note

1. The CPU Units for Duplex CPU Systems are specially designed for use in Duplex CPU Systems and cannot be used in Single CPU Systems or mounted in a CS-series CPU Rack.
2. The CS1D-BC042D CPU Backplane, CS1D-DPL02D Duplex Unit, and CS1D I/O Control Unit are specially designed for use in Duplex CPU Dual I/O Expansion Systems. These components cannot be used in Duplex CPU Single I/O Expansion Systems, Single CPU Systems, or a CS-series CPU Rack.
3. The CS1D-BC052 CPU Backplane and CS1D-DPL01 Duplex Unit are specially designed for use in Duplex CPU Single I/O Expansion Systems. These components cannot be used in Duplex CPU Dual I/O Expansion Systems, Single CPU Systems, or a CS-series CPU Rack.
4. CPU Units for Single CPU Systems and CPU Backplanes for Single CPU Systems are specially designed for use in Single CPU Systems and cannot be used in Duplex CPU Systems or for a CS-series CPU Rack.

Devices

CPU Units

Two CS1D CPU Units of the same model are required when using Duplex CPU Units in a Duplex CPU System.

Name	Model	Specifications
CPU Units for Duplex CPU System	CS1D-CPU67HA	I/O bits: 5,120; program capacity: 250 Ksteps; Data memory: 448 Kwords (DM: 32 Kwords; EM: 32 Kwords x 13 banks)
	CS1D-CPU68HA	I/O bits: 5,120; program capacity: 400 Ksteps; Data memory: 832 Kwords (DM: 32 Kwords; EM: 32 Kwords x 25 banks)
	CS1D-CPU65H	I/O bits: 5,120; program capacity: 60 Ksteps; Data Memory: 128 Kwords (DM: 32 Kwords; EM: 32 Kwords x 3 banks)
	CS1D-CPU67H	I/O bits: 5,120; program capacity: 250 Ksteps; Data Memory: 448 Kwords (DM: 32 Kwords; EM: 32 Kwords x 13 banks)
CPU Units for Single CPU System	CS1D-CPU44SA	I/O bits: 1,280; program capacity: 30 Ksteps; Data memory: 64 Kwords (DM: 32 Kwords; EM: 32 Kwords x 1 banks)
	CS1D-CPU67SA	I/O bits: 5,120; program capacity: 250 Ksteps; Data Memory: 448 Kwords (DM: 32 Kwords; EM: 32 Kwords x 13 banks)
	CS1D-CPU42S	I/O bits: 960; program capacity: 10 Ksteps; Data Memory: 64 Kwords (DM: 32 Kwords; EM: 32 Kwords x 1 bank)
	CS1D-CPU44S	I/O bits: 1,280; program capacity: 30 Ksteps; Data Memory: 64 Kwords (DM: 32 Kwords; EM: 32 Kwords x 1 bank)
	CS1D-CPU65S	I/O bits: 5,120; program capacity: 60 Ksteps; Data Memory: 128 Kwords (DM: 32 Kwords; EM: 32 Kwords x 3 banks)
	CS1D-CPU67S	I/O bits: 5,120; program capacity: 250 Ksteps; Data Memory: 448 Kwords (DM: 32 Kwords; EM: 32 Kwords x 13 banks)

CPU Backplanes

Name	Model	Specifications
CPU Backplane for Duplex CPU Systems (Especially for a Duplex CPU, Dual I/O Expansion System)	CS1D-BC042D	Duplex Connecting Cable:3 slots Single Connecting Cable:4 slots No Expansion:5 slots
CPU Backplane for Duplex CPU Systems (Especially for a Duplex CPU, Single I/O Expansion System)	CS1D-BC052	5 slots
CPU Backplane for Single CPU System	CS1D-BC082S	8 slots

Power Supply Units

Two CS1D Power Supply Units are required for a duplex power supply configuration.

Name	Model	Specifications
CS1D Power Supply Units	CS1D-PA207R	100 to 120 V AC; 200 to 240 V AC (RUN output) Output capacity: 5 V DC at 7 A; 26 V DC at 1.3 A
	CS1D-PD024	24 V DC Output capacity: 5 V DC at 4.3 A; 26 V DC at 0.56 A
	CS1D-PD025	24 V DC Output capacity: 5 V DC at 5.3 A; 26 V DC at 1.3 A

Duplex Unit

One Duplex Unit is required on the CPU Rack.

Name	Model	Specifications
Duplex Unit (Especially for a Duplex CPU, Dual I/O Expansion System)	CS1D-DPL02D	Required in a Duplex CPU System. Can be replaced online.
Duplex Unit (Especially for a Duplex CPU, Single I/O Expansion System)	CS1D-DPL01	Required in a Duplex CPU System.

I/O Control Unit

Name	Model	Specifications
CS1D I/O Control Unit (Especially for a Duplex CPU, Dual I/O Expansion System)	CS1D-IC102D	Two Units (or one) are required to expand a Duplex CPU, Dual I/O Expansion System.

Other Devices

Name	Model	Specifications
Memory Cards	HMC-EF183	Flash memory, 128 MB
	HMC-EF283	Flash memory, 256 MB
	HMC-EF583	Flash memory, 512 MB
	HMC-AP001	Memory Card Adapter
Programming Consoles	C200H-PRO27-E	An English Keyboard Sheet (CS1W-KS001-E) is required.
Programming Console Key Sheet	CS1W-KS001	For C200H-PRO27-E
Programming Console Connecting Cables	CS1W-CN224	Connects the CQM1-PRO27-E Programming Console. (Length: 2.0 m)
	CS1W-CN624	Connects the CQM1-PRO27-E Programming Console. (Length: 6.0 m)
Programming Device Connecting Cables (for peripheral port)	CS1W-CN118	Connects IBM PC/AT or compatible computers. D-Sub 9-pin receptacle (For converting between RS-232C cable and peripherals) (Length: 0.1 m)
	CS1W-CN226	Connects IBM PC/AT or compatible computers. D-Sub 9-pin (Length: 2.0 m)
	CS1W-CN626	Connects IBM PC/AT or compatible computers. D-Sub 9-pin (Length: 6.0 m)

Name	Model	Specifications
Programming Device Connecting Cables (for RS-232C port)	XW2Z-200S-CV	Connects IBM PC/AT or compatible computers. D-Sub 9-pin (Length: 2.0 m), Static-resistant connector used.
	XW2Z-500S-CV	Connects IBM PC/AT or compatible computers. D-Sub 9-pin (Length: 5.0 m), Static-resistant connector used.
	XW2X-200S-V	Connects IBM PC/AT or compatible computers. D-Sub 9-pin (Length: 2.0 m (See note 2.)
	XW2X-500S-V	Connects IBM PC/AT or compatible computers. D-Sub 9-pin (Length: 5.0 m) (See note 2.)
Battery Set	CS1W-BAT01	For CS Series only.
Space Units	CS1W-SP001	Mount to an unused I/O slot.
	CS1D-SP001	Mount to an unused Power Supply Unit slot (same shape as PA207R).
	CS1D-SP002	Mount to an unused Power Supply Unit slot (same shape as PD024).
Expansion Rack Cable Mounting Bracket	CS1D-ATT02	Mounting Bracket to prevent accidental disconnection of the Expansion Rack's cable (for a Duplex CPU, Dual I/O Expansion System)
	CS1D-ATT01	Mounting Bracket to prevent accidental disconnection of the Expansion Rack's cable (for a Duplex CPU, Single I/O Expansion System)

Note

1. A Host Link (SYSWAY) connection is not possible when connecting a CX-Programmer via Peripheral Bus Connecting Cable for the peripheral port. Use a peripheral bus connection.
2. A peripheral bus connection is not possible when connecting a CX-Programmer via RS-232C Connecting Cable.
3. For precautions regarding the use of Memory Cards, refer to *5-1 File Memory* in the *SYSMAC CS/CJ/NSJ Series Programmable Controllers Programming Manual* (W394).

2-2-2 Expansion Racks

It is possible to connect Expansion Racks in order to mount Units outside of the CS1D CPU Rack.

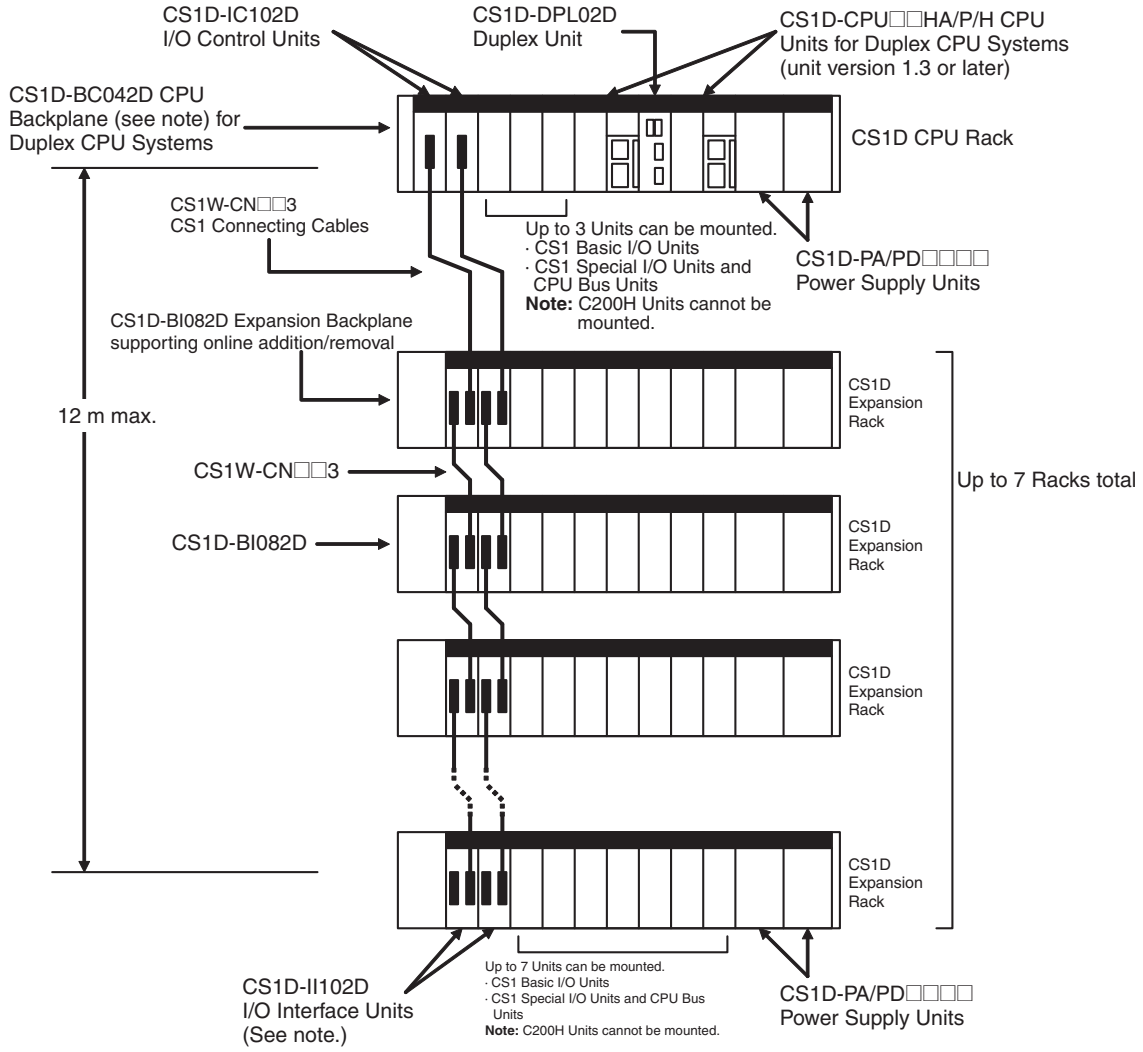
There are two types of Expansion Racks that can be connected: CS1D Expansion Racks and CS1D Long-distance Expansion Racks. Both Racks can be connected to Duplex CPU Systems and Simple-CPU Systems, but the appropriate CS1D Backplane must be used for either type of Rack.

Note Neither CS-series Expansion Racks nor C200H Expansion I/O Racks can be connected to a CS1D CPU Rack.

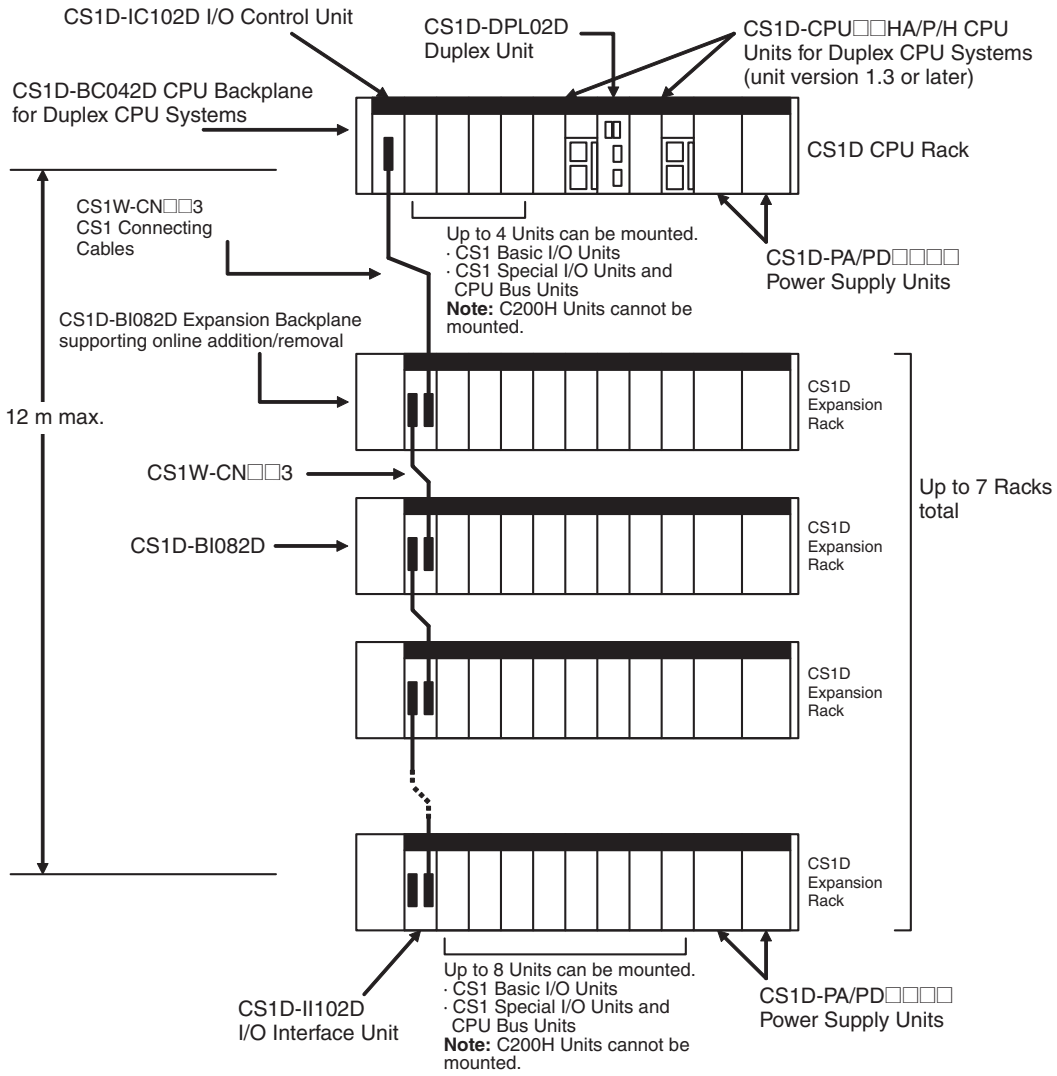
Expansion Patterns

CS1D CPU Rack + CS1D Expansion Racks (Duplex CPU, Dual I/O Expansion System)

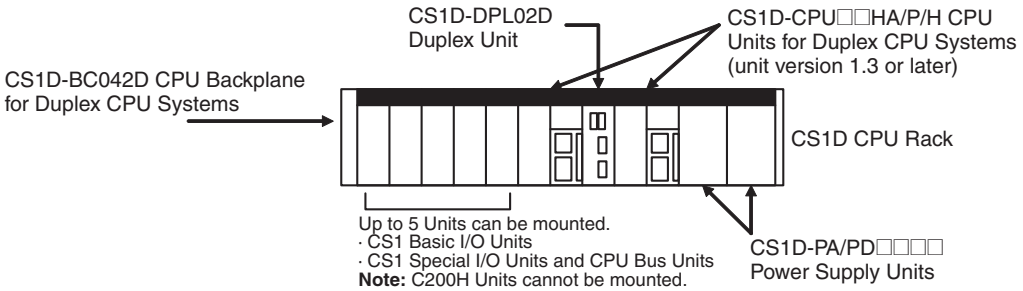
■ **Configuration with Duplex Connecting Cables**



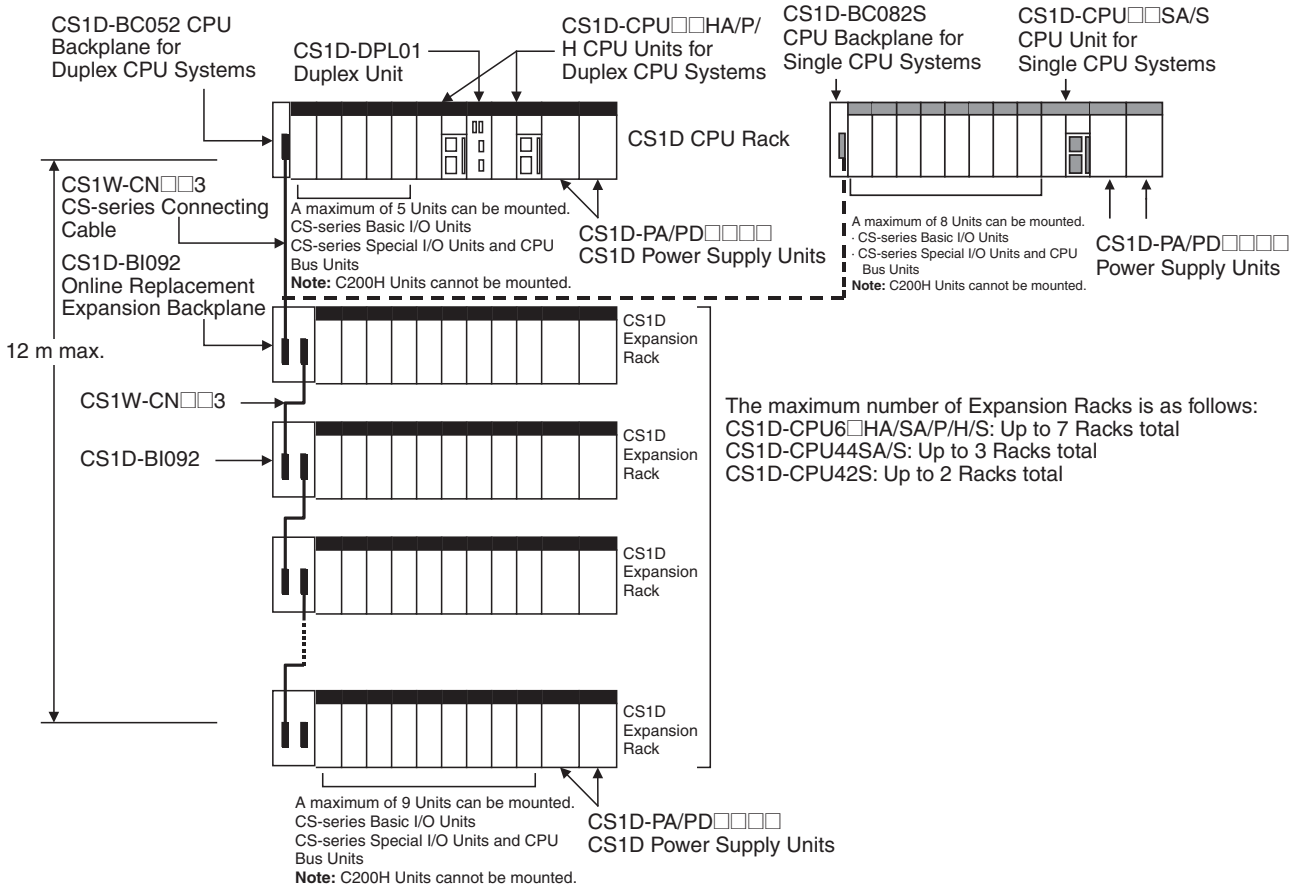
■ Configuration with Single Connecting Cable



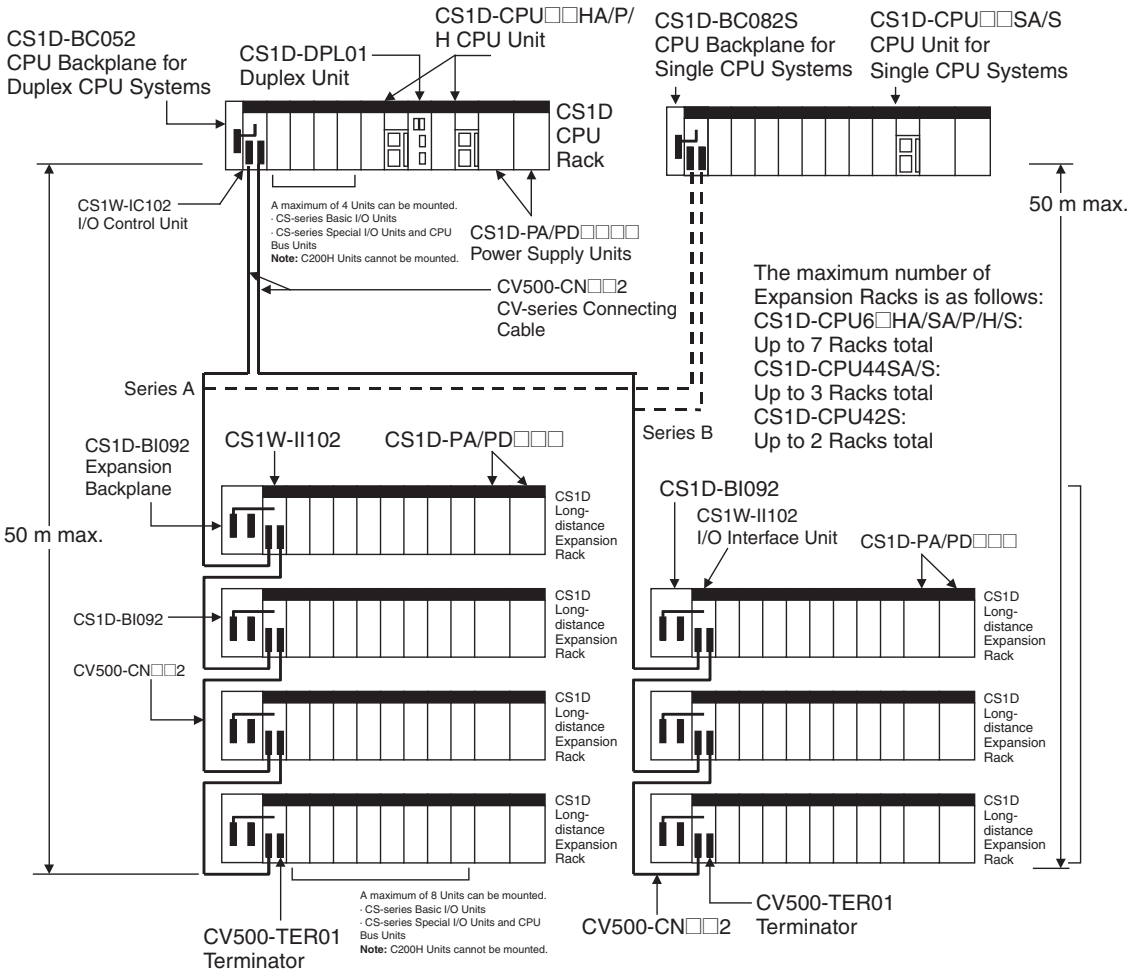
■ Configuration without Expansion Racks



CS1D CPU Rack + CS1D Expansion Racks (Duplex CPU, Single I/O Expansion System)



CS1D CPU Rack + CS1D Long-distance Expansion Racks (Duplex CPU, Single I/O Expansion System)



Maximum Expansion Racks

Expansion pattern	Rack	Maximum No. of Racks (See note.)	Remarks
CS1D CPU Rack + CS1D Expansion Racks	CS1D Expansion Rack	7 Racks	The total cable length must be 12 m or less.
CS1D CPU Rack + CS1D Long-distance Expansion Racks	CS1D Long-distance Expansion Rack	7 Racks	The total cable length must be 50 m or less each for up to two series of Long-distance Expansion Racks (100 m max. total).

Note The maximum number of Racks depends on the CPU Unit being used.

Model	Number of Expansion Racks
CS1D-CPU67HA	7
CS1D-CPU68HA	7
CS1D-CPU65H	7
CS1D-CPU67H	7
CS1D-CPU44SA	3
CS1D-CPU67SA	7

Model	Number of Expansion Racks
CS1D-CPU42S	2
CS1D-CPU44S	3
CS1D-CPU65S	7
CS1D-CPU67S	7

Rack Configurations

Name	Configuration	Remarks
CS1D Expansion Racks	CS1D Online Replacement Expansion Backplane	One Backplane is required.
	CS1D Power Supply Units	Two Units (or one) are required.
	Duplex CPU, Dual I/O Expansion System • Mount a CS1D-IC102D I/O Control Unit to the CS1D CPU Rack. • Mount CS1D-II102D I/O Interface Units to the CS1D Expansion Racks. • A terminator is not required.	One (or two) CS1D I/O Control Units or I/O Interface Units are required.
	CS-series Connecting Cable (When CS1D CPU Rack + CS1D Expansion Racks are connected)	It is not possible to connect to either a CS-series Expansion Rack or a C200H Expansion I/O Rack from a CS1D Expansion Rack.
CS1D Long-distance Expansion Racks	Mount an I/O Control Unit (CS1W-IC102) to the CS1D CPU Rack. Mount an I/O Interface Unit (CS1W-II102) to each Long-distance Expansion Rack. Attach a Terminator (CV500-TER01) to the last Long-distance Expansion Rack in each series. Two Terminators are provided with the I/O Control Unit.	Each I/O Control Unit and I/O Interface Unit requires one slot. These Units are not allocated I/O words. Use CV-series I/O Connecting Cables. A CS1D Long-distance Expansion Rack cannot be connected to another Long-distance Expansion Rack using CS-series I/O Connecting Cable.

Configuration Device List

CS1D Online Replacement Expansion Backplane

Name	Model	Specifications
Expansion Backplane supporting online replacement (for a Duplex CPU, Dual I/O Expansion System)	CS1D-BI082D	Duplex Connecting Cables: 7 slots Single Connecting Cable: 8 slots
CS1D Online Replacement Expansion Backplane (for a Duplex CPU Single I/O Expansion System or Single CPU System)	CS1D-BI092	9 slots Used for both CS1D Expansion Racks and CS1D Long-distance Expansion Racks.

CS1D Power Supply Units

Two CS1D Power Supply Units are required for a duplex configuration.

Name	Model	Specifications
CS1D Power Supply Units	CS1D-PA207R	100 to 120 V AC or 200 to 240 V AC (RUN output) Output capacity: 5 V DC, 7 A; 26 V DC, 1.3 A
	CS1D-PD024	24 V DC Output capacity: 5 V DC at 4.3 A; 26 V DC at 0.56 A
	CS1D-PD025	24 V DC Output capacity: 5 V DC at 5.3 A; 26 V DC at 1.3 A

CS1D I/O Interface Unit

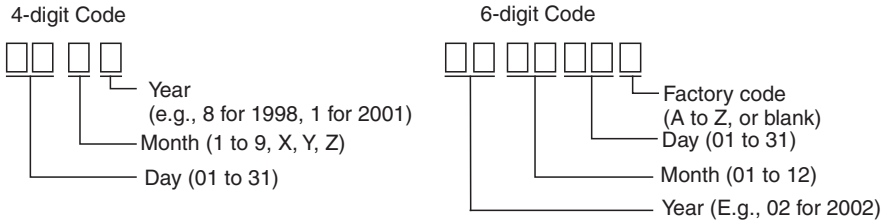
Name	Model	Specifications
CS1D I/O Interface Unit (for a Duplex CPU, Dual I/O Expansion System)	CS1D-II102D	One or two Units are required for a Duplex CPU, Dual I/O Expansion System.

CS-series Connecting Cables

Name	Model	Specifications	Remarks
CS-series Connecting Cables	CS1W-CN313 (See note.)	Connects between CS1D CPU Racks or CS1D Expansion Racks.	0.3 m
	CS1W-CN713 (See note.)		0.7 m
	CS1W-CN223		2 m
	CS1W-CN323		3 m
	CS1W-CN523		5 m
	CS1W-CN133		10 m
	CS1W-CN133B2		12 m

Note When using a CS1W-CN313 or CS1W-CN713 CS-series I/O Expansion Cable for a CS1D System, always use a Cable manufactured on or after September 20, 2001. The manufacturing date is indicated on the connector as a 4-digit code or a 6-digit code. Cables that were manufactured before this date, or that do not indicate a manufacturing date cannot be used.

Manufacturing Date Codes



Devices for Long-distance Expansion Racks

Name	Model	Specifications	Remarks
I/O Control Unit	CS1W-IC102	Mounts to the leftmost slot on the CS1D CPU Rack to enable connecting CS1D Long-distance Expansion Racks.	---
I/O Interface Unit	CS1W-II102	Mounts to the leftmost slot on a Long-distance Expansion Rack.	
CV-series I/O Connecting Cables	CV500-CN312	Connects CS1D Long-distance Expansion Racks.	0.3 m
	CV500-CN612		0.6 m
	CV500-CN122		1 m
	CV500-CN222		2 m
	CV500-CN322		3 m
	CV500-CN522		5 m
	CV500-CN132		10 m
	CV500-CN232		20 m
	CV500-CN332		30 m
	CV500-CN432		40 m
	CV500-CN532		50 m

Connectable Units

The following table shows the Units that can be connected to CS1D CPU Racks and CS1D Expansion Racks.

Rack	Unit					
	Basic I/O Units (See note 1.)			Special I/O Units		CPU Bus Units
	CS-series Basic I/O Units	C200H Basic I/O Units	C200H Group 2 Multi-point I/O Units	CS-series Special I/O Units	C200H Special I/O Units	CPU Bus Units
CS1D CPU Racks	Yes	No	No	Yes	No	Yes
CS1D Expansion Racks	Yes	No	No	Yes	No	Yes
CS1D Long-distance Expansion Racks	Yes	No	No	Yes	No	Yes (See note 2.)

Note

1. Interrupt Input Units can be used only as ordinary Input Units.
2. Although CPU Bus Units can be mounted, it is not recommended because of delays in cycle time.

Maximum Number of Connectable Units

The maximum number of expansion slots depends upon the system configuration, as shown in the following table. The total number of each type of Unit is not limited by the mounting location.

Note Up to 16 CPU Bus Units can be mounted.

System		Max. number of slots
Duplex CPU, Dual I/O Expansion System	Duplex Connecting Cables	52 slots
	Single Connecting Cable	60 slots
Duplex CPU, Single I/O Expansion System		68 slots
Single CPU System		71 slots

CS1D Configuration Devices

The following table shows the Units, Programming Devices, and Support Software that can be used to configure a CS1D Duplex System.

Note Always use the specified CS1D Units for the CPU Units, Power Supply Units, CPU Backplanes, and Expansion Backplanes. CS-series Units cannot be used.

Name		Model	Support			Remarks
			Duplex CPU, Dual I/O Expansion System	Duplex CPU, Single I/O Expansion System	Single CPU System	
CPU Units	CPU Units for Duplex CPU Systems	CS1D-CPU□□HA/H CS1D-CPU□□P	Yes (Unit version 1.3 or later)	Yes	No	Use specified CS1D Units only. CS-series Units cannot be used.
	CPU Units for Single CPU Systems	CS1D-CPU□□SA/S	No	No	Yes	
	CS-series CPU Units	CS1G/H-CPU□□-V1 CS1G/H-CPU□□H	No	No	No	
Duplex Unit	Duplex CPU, Dual I/O Expansion System	CS1D-DPL02D	Yes	No	No	---
	Duplex CPU, Single I/O Expansion System	CS1D-DPL01	No	Yes	No	---
Power Supply Units	CS1D Power Supply Units	CS1D-PA207R CS1D-PD024 CS1D-PD025	Yes	Yes	Yes	Use specified CS1D Units only. C200H and CS-series Units cannot be used.
	C200H and CS-series Power Supply Units	C200HW-P□□□□□	No	No	No	
CPU Backplanes	CPU Backplane for Duplex CPU Systems	CS1D-BC042D (for a Duplex CPU, Dual I/O Expansion System)	Yes	No	No	Use specified CS1D Units only. CS-series Units cannot be used. **Note** When securing the Expansion Rack's cable, the Backplane must have a production date of July 2005 or later.
		CS1D-BC052 (See note.) (for a Duplex CPU, Single I/O Expansion System)	No	Yes	No	
	CPU Backplane for Single CPU Systems	CS1D-BC082S	No	No	Yes	
	CS-series CPU Backplanes	CS1W-BC□□□	No	No	No	

Name		Model	Support			Remarks
			Duplex CPU, Dual I/O Expansion System	Duplex CPU, Single I/O Expansion System	Single CPU System	
Expansion Backplanes	Online Replacement Expansion Backplane	CS1D-BI082D (for a Duplex CPU, Dual I/O Expansion System)	Yes	No	No	Use specified CS1D Units only. CS-series Units cannot be used. CS1D Expansion Racks and CS1D Long-distance Expansion Racks can both be used. The Connecting Cable is the same as that used for the CS Series. **Note** When securing the Expansion Rack's cable, the Backplane must have a production date of July 2005 or later.
		CS1D-BI092 (for a Duplex CPU, Single I/O Expansion System or Single CPU System)	No	Yes	Yes	
	CS-series Expansion Backplanes	CS1W-BI□□□	No	No	No	
	C200H Expansion Backplanes	C200HW-BI□□□-V1	No	No	No	
CS1D I/O Control Unit		CS1D-IC102D	Yes	No	No	Use with a Duplex CPU, Dual I/O Expansion System. (Mount in the CPU Rack. Cannot be mounted in an Expansion Rack.)
CS1D I/O Interface Unit		CS1D-II102D	Yes	No	No	Use with a Duplex CPU, Dual I/O Expansion System. (Mount in the Expansion Racks. Cannot be mounted in the CPU Rack.)
I/O Control Unit		CS1W-IC102	No	Yes	Yes	Use with a Long-distance Expansion Rack (Mount to the CPU Backplane. Cannot be mounted to an Expansion Backplane.)
I/O Interface Unit		CS1W-II102	No	Yes	Yes	Use with the Long-distance Expansion Rack. (Cannot be mounted to an Expansion Rack.)
Terminator		CV500-TER01	No	Yes	Yes	Use for terminating resistance on the Long-distance Expansion Rack.
Expansion Rack Cable Mounting Bracket		CS1D-ATT01	No	Yes	No	Secures the Connecting Cable in a Duplex CPU, Dual I/O Expansion System.
		CS1D-ATT02	Yes	No	No	Secures the Connecting Cable in a Duplex CPU, Single I/O Expansion System.

Name		Model	Support		Remarks
			Duplex CPU System	Single CPU System	
Basic I/O Units		CS-series Basic I/O Units	Yes	Yes	---
		CS1W-INT01 CS-series Interrupt Input Units	Restricted	Yes	Can be used only as Standard I/O Units in Duplex CPU Systems.
		C200H Basic I/O Units	No	No	C200H I/O Units cannot be used.
Special I/O Units		CS-series Special I/O Units	Yes	Yes	---
		C200H Special I/O Units	No	No	C200H Special I/O Units cannot be used.
CPU Bus Units		CS-series CPU Bus Units (including Communications Units that support duplex operation)	Yes	Yes	---
Inner Boards		CS1W-SBC21 CS1W-SCB21-V1 CS1W-SCB41 CS1W-SCB41-V1 CS1W-LCB01/05 (See note.) and other models	No	Yes	Inner Boards cannot be used in Duplex CPU Systems unless built into a Process-control CPU Unit. **Note** Loop Control Board unit version 1.5 or later must be used.
Memory Cards		HMC-EF□□□	Yes	Yes	---
Battery Set		CS1W-BAT01	Yes	Yes	---
Connector Covers		C500-COV01	Yes	Yes	Use to protect the power supply connector on the Backplane.
		CV500-COV01	Yes	Yes	Use to protect the I/O slot connector on the Backplane.
Space Units		CS1W-SP001	Yes	Yes	Mount to an unused I/O slot.
		CS1D-SP001	Yes	Yes	Mount to an unused Power Supply Unit slot (same shape as PA207R).
		CS1D-SP002	Yes	Yes	Mount to an unused Power Supply Unit slot (same shape as PD024).
Programming Devices and Support Software	Software for personal computer	CX-Programmer Ver. 4.0 or higher	Yes	Yes	CS1D-CPU□□HA requires CX-Programmer Ver. 9.7 or later.
		CX-Programmer Ver. 3.0 or higher	Yes	No	Use Ver. 3.1 or higher for online Unit replacement functions. CS1D-CPU□□HA cannot be used.
		CX-Programmer Ver. 2.1 or higher	No	No	---
		CX-Protocol	Yes	Yes	---
		SYSMAC-CPT	No	No	---
		SYSMAC Support Software (SSS)	No	No	---
	Programming Console	CQM1-PRO01	Yes	Yes	The Key Sheet and Connecting Cable are the same as those used for the CS1/CS1-H System.
		CQM1H-PRO01	Yes	Yes	---
		C200H-PRO27	Yes	Yes	---

Name		Model	Support		Remarks
			Duplex CPU System	Single CPU System	
CS-series Connecting Cables	0.3 m	CS1W-CN313	Yes	Yes	Use to connect between Expansion Racks or between Expansion Rack and CPU Rack.
	0.7 m	CS1W-CN713	Yes	Yes	
	2 m	CS1W-CN223	Yes	Yes	
	3 m	CS1W-CN323	Yes	Yes	
	5 m	CS1W-CN523	Yes	Yes	
	10 m	CS1W-CN133	Yes	Yes	
	12 m	CS1W-CN133-B2	Yes	Yes	
Long-distance Expansion Cables	0.3 m	CV500-CN312	Yes	Yes	Use to connect Long-distance Expansion Racks.
	0.6 m	CV500-CN612	Yes	Yes	
	1 m	CV500-CN122	Yes	Yes	
	2 m	CV500-CN222	Yes	Yes	
	3 m	CV500-CN322	Yes	Yes	
	5 m	CV500-CN522	Yes	Yes	
	10 m	CV500-CN132	Yes	Yes	
	20 m	CV500-CN232	Yes	Yes	
	30 m	CV500-CN332	Yes	Yes	
	40 m	CV500-CN432	Yes	Yes	
	50 m	CV500-CN532	Yes	Yes	

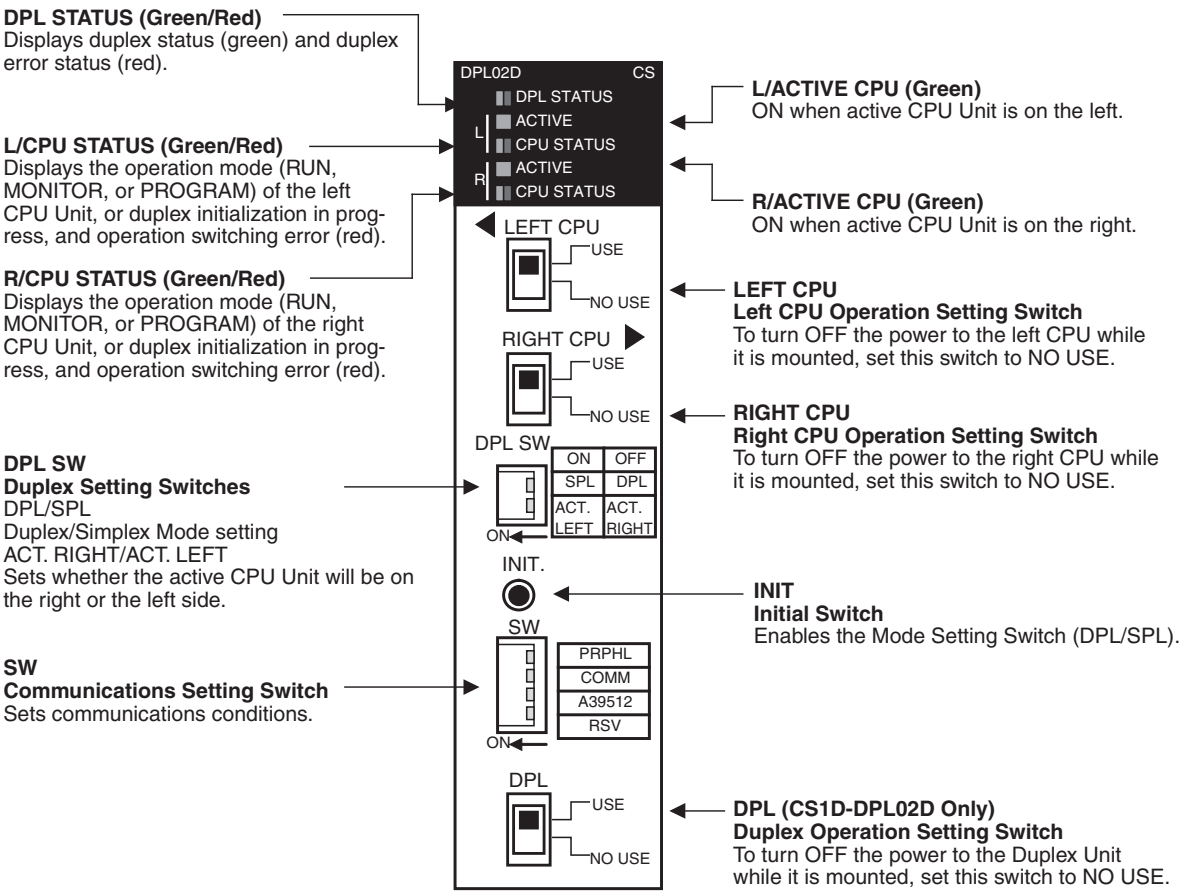
2-3 Duplex Unit

2-3-1 Duplex Unit Model

Item	Specifications
Model number	CS1D-DPL02D (for a Duplex CPU, Dual I/O Expansion System) CS1D-DPL01 (for a Duplex CPU, Single I/O Expansion System)
Number mounted	One Duplex Unit is required for a Duplex CPU System.
Weight	200 g max.

One Duplex Unit is required for a Duplex CPU System. It is not required for a Single CPU System.

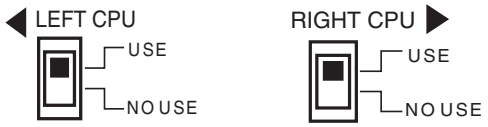
2-3-2 Nomenclature



Duplex Unit Switches

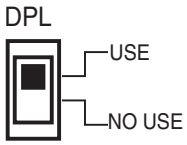
⚠ **Caution** Before touching the Duplex Unit, be sure to first touch grounded metal to discharge static electricity.

CPU Operating Switches



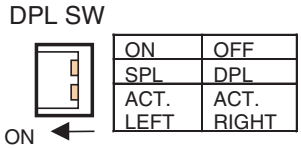
Setting		Contents	Application
USE	Turns ON power to CPU Unit.	Turns ON or OFF the power supply to the respective CPU Units.	Set to NO USE when replacing a CPU Unit while leaving the power ON, or when not using a CPU Unit.
NO USE	Turns OFF power to CPU Unit.		

Duplex Unit Operating Switch



Setting		Contents	Application
USE	Turns ON power to the Duplex Unit.	Turns ON or OFF the power supply to the Duplex Unit.	Set to NO USE when replacing a Duplex Unit. while leaving the power ON. The Duplex CPU System will operate in Simplex Mode during replacement.
NO USE	Turns OFF power to the Duplex Unit.		

Duplex Setting Switches



(1) Mode Setting Switch (DPL/SPL)

Switch	Setting			Meaning	Application
DPL/SPL	OFF	DPL	Duplex Mode	Sets whether the System will operate in Duplex Mode or Simplex Mode. This switch is enabled in the following situations: 1) When the power is turned ON. 2) When the CPU Operation Setting Switch is switched from NO USE to USE. 3) When the Initial Switch is pressed. **Note:** Switching is disabled during operation. This switch is also disabled in a Simplex System.	Set to OFF (DPL) for Duplex Mode, and to ON (SPL) for Simplex Mode.
	ON	SPL	Simplex Mode		

Note Duplex Mode and Simplex Mode can also be determined by the status of bit 08 of word A328.

(2) Active Setting Switch (ACT. RIGHT/ACT. LEFT)

Switch	Setting			Contents	Application
ACT RIGHT/ ACT LEFT	OFF	ACT RIGHT	Sets the right CS1D CPU Unit as the active Unit.	Sets whether the right or left CS1D CPU Unit is to be the active Unit. This switch is enabled only when the power is turned ON, so, after changing the setting, turn the power OFF and then back ON again. Changing the setting is disabled during operation. This switch is also disabled in Simplex Mode.	To set the right CS1D CPU Unit as the active Unit, set the switch to OFF (ACT RIGHT). To set the left CS1D CPU Unit as the active Unit, set the switch to ON (ACT LEFT).
	ON	ACT LEFT	Sets the left CS1D CPU Unit as the active Unit.		

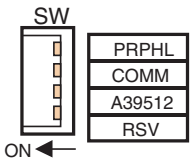
Initial Switch

Press the Initial Switch to toggle between Duplex Mode and Simplex Mode after a CS1D CPU Unit has been replaced.

Setting	Contents	Application
The Mode Setting Switch is enabled when this switch is pressed.	Reflects the status (Duplex/Simplex Mode) of the Mode Setting Switch while the power is ON.	Press to return to Duplex Mode after a CS1D CPU Unit has been replaced. If there is no change in the Mode Setting Switch, then the mode (Duplex/Simplex) will not be changed even if the Initial Switch is pressed.

Note If the Initial Switch is pressed immediately after the power supply is turned ON, it may not have any effect.

Communications Setting Switch



In place of pins 4, 5, and 6 of the DIP switches on the right and left CPU Units, set the PRPHL and COMM pins and bit A39512 as shown in the following table.

Turn OFF pins 4, 5, and 6 on both the right and left CPU Units.

Pin	Contents		Setting	Applications
PRPHL	Peripheral port communications (In place of pin 4 of the DIP switches.)	ON	According to the peripheral port baud rate setting in the PLC Setup. (See note 3.)	Leave OFF when peripheral port is to be used by a Programming Console or CX-Programmer (with peripheral bus setting). Turn ON when peripheral port is to be used by other than a Programming Console or CX-Programmer (peripheral bus).
		OFF (default)	Connect a Programming Console or CX-Programmer at the baud rate for Programming Devices. (The communications conditions are automatically detected.) (See note 1.)	
COMM	RS-232C communications conditions (In place of pin 5 of the DIP switches.)	ON	Connect a CX-Programmer at the baud rate for Programming Consoles. (The baud rate is automatically detected.) (See note 2.)	Leave OFF when RS-232C port is to be used by other than a CX-Programmer (peripheral bus), such as a PT or host computer. Turn ON when RS-232C port is to be used by a CX-Programmer (peripheral bus).
		OFF (default)	According to the RS-232C port communications conditions settings in the PLC Setup.	
A39512	User-customized DIP switch pin (In place of pin 6 of the DIP switches.)	ON	A39512 ON	The status of this DIP switch pin is reflected in the User DIP Switch Pin Flag (A39512) in the Auxiliary Area.
		OFF (default)	A39512 OFF	
RSV		Disabled	Set to OFF.	

Note

1. The order of automatic detection looks for a Programming Console first and then it will attempt to detect a peripheral bus connect at the following speeds: 9,600 bps, 19,200 bps, 38,400 bps, and then 115,200 bps. If the Programming Device is in a mode other than peripheral bus, or if it is set

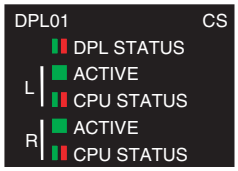
by peripheral bus to a baud rate other than those that are automatically detected, the auto-detection function will not work.

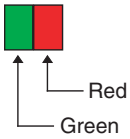
2. The order of automatic detection is as follows: 9,600 bps, 19,200 bps, 38,400 bps, and then 115,200 bps. If the Programming Device is in a mode other than peripheral bus, or if it is set by peripheral bus to a baud rate other than those that are automatically detected, the auto-detection function will not work.
3. For details on the PLC Setup, refer to *SECTION 6 PLC Setup*.
4. When connecting a CX-Programmer to the peripheral port or RS-232C port, set the CX-Programmer's network classification and either the PRPHL pin or the COMM pin on the DIP switch as shown in the following table.

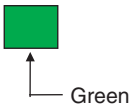
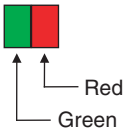
CX-Programmer's network setting	Connecting to peripheral port	Connecting to RS-232C port	PLC Setup
Peripheral bus	Set the PRPHL pin to OFF.	Set the COMM pin to ON.	---
SYSWAY (Host Link)	Set the PRPHL pin to ON.	Set the COMM pin to OFF.	Set to "Host Link."

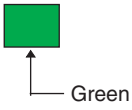
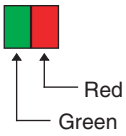
5. Be sure to set the RSV (reserve) pin to OFF.

Duplex Unit Indicators



Indicator	Status	Contents	Description
DPL STATUS 	Green (ON)	The System is operating normally in Duplex Mode.	The active and standby CPU Units are operating normally in synchronization in Duplex Mode.
	Green (flashing)	The System is being initialized for duplex operation.	The active and standby CPU Units are being initialized for duplex operation (transferring or verifying data).
	Red (ON)	A duplex bus error has occurred in the System.	A duplex bus error has occurred in Duplex Mode. (An error has occurred in the duplex bus, and A31601 has turned ON.) **Note** At this time, the mode is switched from Duplex Mode to Simplex Mode, and operation is continued by the active CPU Unit alone.
	Red (flashing)	A duplex verification error has occurred in the System.	A duplex verification error has occurred in Duplex Mode. (One of the following items does not match for the active and standby CPU Units, and A31600 has turned ON.) CPU Unit model numbers Parameter Areas User program areas Inner Board data is not the same (Process-control CPU Units only). A function not supported by the standby CPU Unit was performed by the active CPU Unit (unit version 1.1 or later). The cause of the duplex verification error is stored in Auxiliary Area word A317. **Note** 1. At this time, the mode is switched from Duplex Mode to Simplex Mode, and operation is continued by the active CPU Unit alone. 2. Verification is not performed for the mounting, model number, or data contents of Memory Cards, or for front-panel DIP switch settings. Operation will continue in Duplex Mode even if these do not match for the active and standby CPU Units.
	OFF	The System is operating normally in Simplex Mode.	Either operation is normal in Simplex Mode, or an error has occurred in Duplex Mode and the System is now operating normally in Simplex Mode.

Indicator		Status	Contents		Description
L	ACTIVE 	Green (ON)	The left CPU Unit is active (ACT).		The left CPU Unit is the active (i.e., controlling) CPU Unit.
		OFF	The left CPU Unit is on standby (STB).		Either the left CPU Unit is on standby or the CPU Unit has stopped.
	CPU STATUS 	Green (ON)	The left CPU Unit is in RUN or MONITOR Mode.		The left CPU Unit is operating (i.e., in RUN or MONITOR Mode).
		Green (flashing)	The left CPU Unit is being initialized for duplex operation, or the CPU Unit is waiting.		Either the left CPU Unit is being initialized for duplex operation (transferring or verifying duplex data) or the CPU Unit is waiting. While this indicator is flashing, neither of the CPU Units will begin operation. **Note** 1. If "Run Under Duplex Initial" in the PLC Setup is set to "Start running during initialization" only the active CPU Unit will start running during duplex initialization. 2. This indicator will flash even if a duplex bus error or a duplex verification error occurs when the power is turned ON.
		Red (ON)	Operation switching error at the left CPU Unit	CPU error	A CPU error has occurred at the left CPU Unit.
		Red (flashing)		Other than CPU error	One of the following operation switching errors has occurred at the left CPU Unit. Memory error Program error Cycle time overrun error FALS instruction executed Fatal Inner Board error (Process-control CPU Units only)
		OFF	The left CPU Unit is in PROGRAM Mode.		The left CPU Unit is in PROGRAM Mode, or a fatal error other than those indicated by a lit or flashing red indicator has occurred.

Indicator		Status	Contents		Description
R	ACTIVE 	Green (ON)	The right CPU Unit is active (ACT).		The right CPU Unit is the active (i.e., controlling) CPU Unit.
		OFF	The right CPU Unit is on standby (STB).		Either the right CPU Unit is on standby or the CPU Unit is stopped.
	CPU STATUS 	Green (ON)	The right CPU Unit is in RUN or MONITOR Mode.		The right CPU Unit is operating (i.e., in RUN or MONITOR Mode).
		Green (flashing)	The right CPU Unit is being initialized for duplex operation, or the CPU is waiting.		Either the right CPU Unit is being initialized for duplex operation (transferring or verifying duplex data) or the CPU is waiting. While this indicator is flashing, neither of the CPU Units will begin operation. **Note** 1. If "Run Under Duplex Initial" in the PLC Setup is set to "Start running during initialization" only the active CPU Unit will start running during duplex initialization. 2. This indicator will flash even if a duplex bus error or a duplex verification error occurs when the power is turned ON.
		Red (ON)	Operation switching error at the right CPU Unit	CPU error	A CPU error has occurred at the right CPU Unit.
		Red (flashing)		Other than CPU error	One of the following operation switching errors has occurred at the right CPU Unit. Memory error Program error Cycle time overrun error FALS instruction executed Fatal Inner Board error (Process-control CPU Units only)
		OFF	The right CPU Unit is in PROGRAM Mode.		The right CPU Unit is in PROGRAM Mode, or a fatal error other than those indicated by a lit or flashing red indicator has occurred.

Indicator Status when Power Is Turned ON

The following table shows the status of Duplex Unit indicators when the power supply is turned ON. In this example, the left (L) CPU Unit is set as the active one (ACT.LEFT).

Duplex Unit indicators		Status at startup			
		Being initialized (transferring data, e.g., user program immediately after startup)	**In PROGRAM Mode**	**Operating in Duplex Mode**	**Operating in Simplex Mode**
DPL STATUS		**Green (flashing)**	Green (ON)	**Green (ON)**	**OFF**
L (Active)	ACTIVE	Green (ON)	Green (ON)	Green (ON)	Green (ON)
	CPU STATUS	**Green (flashing)**	**OFF**	**Green (ON)**	**Green (ON)**
R (Non-active)	ACTIVE	OFF	OFF	OFF	OFF
	CPU STATUS	**Green (flashing)**	**OFF**	**Green (ON)**	OFF

Note The items set in bold text in the table are the main ones to indicate the status.

Indicator Status when Errors Occur

The following table shows the status of Duplex Unit indicators when errors occur during Duplex Mode operation (i.e., in either RUN Mode or MONITOR Mode). In this example, the left (L) CPU Unit is set as the active one (ACT.LEFT).

Duplex Unit indicators		Error status						
		Operation switching error at active CPU Unit		Fatal error at active CPU Unit (e.g., too many I/O points)	Duplex error		Non-fatal error at active CPU Unit	CPU waiting
		Non-CPU error	CPU error		Duplex verification error	Duplex bus error		
DPL STATUS		**OFF**		Green (ON)	**Red (flashing)**	**Red (ON)**	Green (ON)	Green (flashing)
L (When set to active)	ACTIVE	OFF		Green (ON)	Green (ON)		Green (ON)	Green (ON)
	CPU STATUS	**Red (flashing)**	**Red (ON)**	**OFF**	Green (flashing) (See note 2.)		**Green (ON)**	**Green (flashing)**
R (When set to standby)	ACTIVE	Green (ON)		OFF	OFF		OFF	OFF
	CPU STATUS	Green (ON) (See note 1.)		OFF	OFF		**Green (ON)**	**Green (flashing)**
System operation		Continues.		Stops.	Continues.		Continues.	Waits.

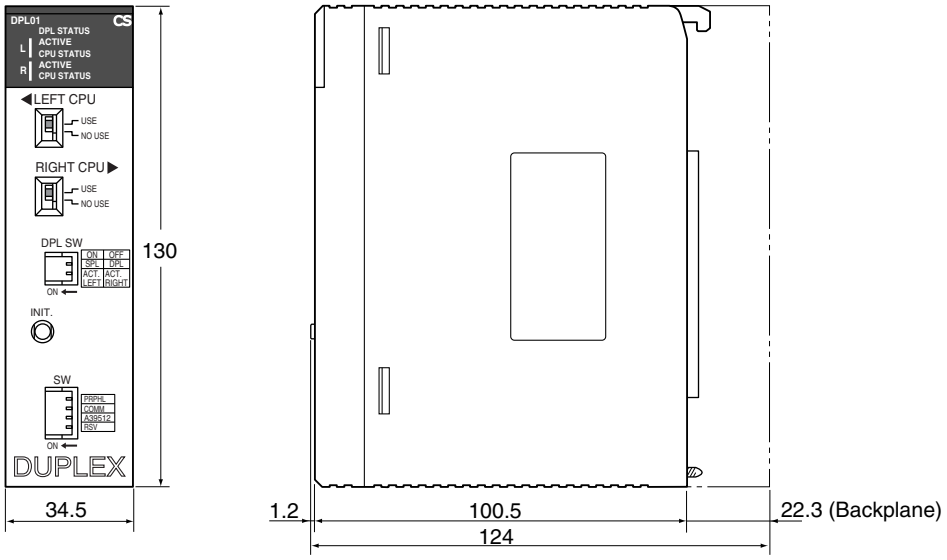
Note

1. If operation is switched to the standby CPU Unit (i.e., in this example, from the left CPU Unit to the right), and then an error occurs at the newly active CPU Unit, the CPU STATUS indicator will flash red for a non-CPU error and stay lit red for a CPU error.
2. This indicator will light green if a duplex error occurs during operation.
3. The items set in bold text in the table are the main ones to indicate the status.

Indicator Status when Replacing the Duplex Unit Online (CS1D-DPLO2D Only)

When the Duplex Unit Operating Switch (DPL USE/NO USE) is set to NO USE to replace the Duplex Unit online, all of the Duplex Unit indicators will be OFF (not lit). During online replacement, only the active CPU Unit will continue operating.

2-3-3 External Dimensions



2-4 CPU Units

2-4-1 Models

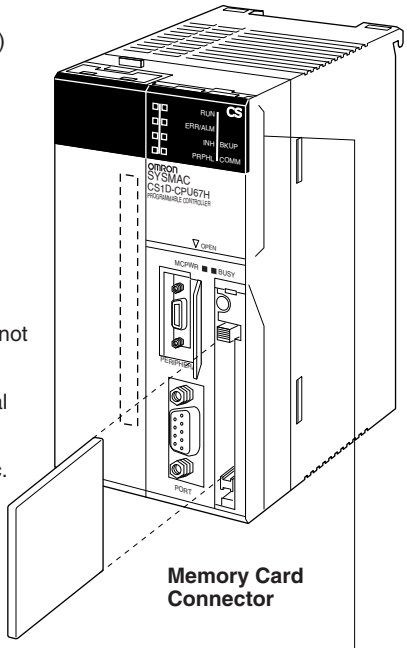
	Number of I/O points (Number of Expansion Racks)	Programming	Data Memory (DM + EM)	Model	Weight
CPU Units for Duplex CPU Systems	5,120 points (7 Racks)	250 Ksteps	448 Kwords	CS1D-CPU67HA	350 g max.
		400 Ksteps	832 Kwords	CS1D-CPU68HA	
		60 Ksteps	128 Kwords	CS1D-CPU65H	
		250 Ksteps	448 Kwords	CS1D-CPU67H	
	1,280 points (3 Racks)	30 Ksteps	64 Kwords	CS1D-CPU44SA	
	5,120 points (7 Racks)	250 Ksteps	448 Kwords	CS1D-CPU67SA	
CPU Units for Single CPU Systems	960 points (2 Racks)	10 Ksteps	64 Kwords	CS1D-CPU42S	
	1,280 points (3 Racks)	30 Ksteps	64 Kwords	CS1D-CPU44S	
	5,120 points (7 Racks)	60 Ksteps	128 Kwords	CS1D-CPU65S	
	5,120 points (7 Racks)	250 Ksteps	448 Kwords	CS1D-CPU67S	

2-4-2 Components

Inner Board Connector
Install an Inner Board. (See note.)

Peripheral Port
Connects Programming Device (including Programming Console) host computer, etc. Refer to 2-6.

RS-232C Port
Connects CX-Programmer (but not Programming Console), host computer, external devices, Programmable Terminal (PT), etc. Refer to 2-6.



Memory Card Connector

Memory Card
Install into the active CPU Unit.

Memory Card
Powered/Accessed Indicators
MCPWR (ON: green)
Power provided to Memory Card.
BUSY (ON: Yellow)
Memory Card being accessed.

Memory Card Power Supply Button
Press this button to turn OFF the power supply before removing the Memory Card or when performing the simple backup operation.

Memory Card Eject Button
Press to remove the Memory Card.

RUN
Lit green when the CPU Unit is operating normally in MONITOR or RUN mode.

ERR/ALM
Lit read when a fatal error was discovered in self-diagnosis or a hardware error has occurred. The CPU Unit will stop operating and all outputs will be turned OFF.
Flashing red when a non-fatal error was discovered in self-diagnosis. The CPU Unit will continue operating.

INH
Lit yellow when the Output OFF Bit (A50015) has been turned ON. The outputs from all Output Units will turn OFF.

BKUP
Lit yellow when data is being transferred between RAM and flash memory.
Do not turn OFF the power supply to the PLC while this indicator is lit.

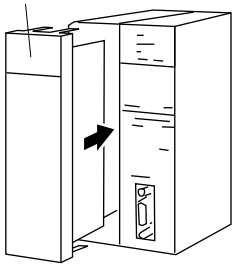
PRPHL
Flashes yellow when the CPU Unit is communicating (sending or receiving) via the peripheral port.

COMM
Flashes yellow when the CPU Unit is communicating (sending or receiving) via the RS-232C port.

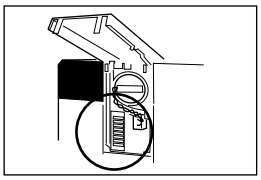
MCPWR
Lit green when power is being supplied to the Memory Card.

BUSY
Flashes yellow when the Memory Card is being accessed.

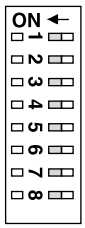
Note: An Inner Board can be mounted in a Single CPU System.



View with battery housing opened.



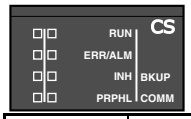
DIP Switch



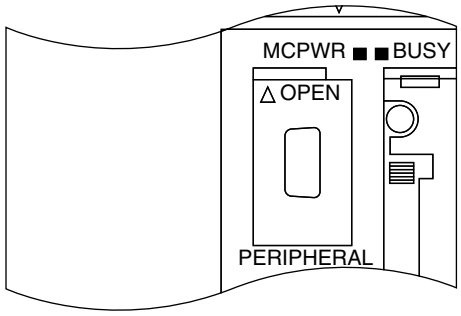
Pin 1: User program memory write (enable: OFF; disable: ON)
Pin 2: Automatic user program transfer at startup (not transferred: OFF; transferred: ON)
Pin 3: Always OFF.
Pin 4: } Refer to *DIP Switch Settings.*
Pin 5: }
Pin 6: }
Pin 7: } Easy backup (read/write from Memory Card) with pin 7 ON and pin 8 OFF.
Easy backup (verification with Memory Card) with pin 7 OFF and pin 8 OFF.
Pin 8: Always OFF.

Note In a Duplex CPU System, the DIP switch on the front panel of the active CPU Unit is enabled (and the one on the standby CPU Unit is disabled). The DIP switch settings on the active and standby CPU Units do not necessarily have to match. Even if they do not match, operation in Duplex Mode is still possible.

Indicators (LED)



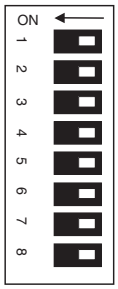
Indicator	Color	Status	Meaning
RUN	Green	ON	CPU Unit is operating normally in MONITOR or RUN mode.
		Flashing	DIP switch settings error.
		OFF	PLC has stopped operating while in PROGRAM mode, or has stopped operating due to a fatal error.
ERR/ALM	Red	ON	A fatal error has occurred (including FALS instruction execution), or a hardware error (CPU error) has occurred. The CPU Unit will stop operating, and the outputs will turn OFF.
		Flashing	A non-fatal error has occurred (including FAL instruction execution). The CPU Unit will continue operating.
		OFF	CPU Unit is operating normally.
INH	Yellow	ON	Output OFF Bit (A50015) has been turned ON. The outputs from all Output Units will turn OFF.
		OFF	Output OFF Bit (A50015) has been turned OFF.
BKUP	Yellow	ON	User program and Parameter Area data is being backed up to flash memory in the CPU Unit or being restored from flash memory. Do not turn OFF the power supply to the PLC while this indicator is lit.
		OFF	Data is not being written to flash memory.
PRPHL	Yellow	Flashing	CPU Unit is communicating (sending or receiving) via the peripheral port.
		OFF	CPU Unit is not communicating via the peripheral port.
COMM	Yellow	Flashing	CPU Unit is communicating (sending or receiving) via the RS-232C port.
		OFF	CPU Unit is not communicating via the RS-232C port.



Indicator	Color	Status	Meaning
MCPWR	Green	ON	Power is being supplied to the Memory Card.
		Flashing	Flashes once: Simple backup write, read, or verify normal. Flashes five times: Simple backup read error. Flashes three times: Simple backup read warning. Flashes continuously: Simple backup write or verify error.
		OFF	Power is not being supplied to the Memory Card.
BUSY	Yellow	Flashing	Memory Card is being accessed.
		OFF	Memory Card is not being accessed.

DIP Switch Settings

A Duplex CPU System, the DIP switch on the front panel of the active CPU Unit is enabled (and the one on the standby CPU Unit is disabled). The DIP switch settings on the active and standby CPU Units do not necessarily have to match. (A duplex verification error will not be generated.) Even if they do not match, operation in Duplex Mode is still possible.



Pin No.	Setting	Function	Application	Default
1	ON	Writing prohibited for user program memory. (See note 1.)	Used to prevent programs from being accidentally overwritten from Programming Devices (including Programming Console).	OFF
	OFF	Writing enabled for user program memory.		
2	ON	The user program is automatically transferred from the Memory Card when power is turned ON. (See note 2.)	Used to store the programs in the Memory Card for switching operations, or to automatically transfer programs at startup (Memory Card ROM operation). **Note** When pin 7 is ON and pin 8 is OFF, simple backup reading from the Memory Card is given priority, so even if pin 2 is ON, the user program is not automatically transferred from the Memory Card when power is turned ON.	OFF
	OFF	The user program is not automatically transferred from the Memory Card when power is turned ON.		
3	Always OFF.	Use with this pin set to OFF.	---	OFF

Pin No.	Setting	Function	Application	Default
4 to 6	See below.		---	
7		Simple backup type	Used to determine the simple backup type. (See note 3.) Normally turn this pin OFF.	OFF
8	Always OFF.	Keep set to Always OFF.	**Note** If the power is turned on with Pin 7 and Pin 8 both ON, a DIP Switch setting error will occur and the peripheral tool cannot be connected.	OFF

DIP Switch Pins 4 to 6 Set these pins as described below. Settings are different for Duplex CPU and Single CPU Systems.

■ Duplex CPU Systems (other than CS1D-CPU67HA)

Pin No.	Setting	Function	Application	Default
4	Always OFF.	Use with this pin set to OFF.	Do not set these switches. Instead, use the PRPHL and COMM switches on the Duplex Unit and A39512 in the Auxiliary Area.	OFF
5	Always OFF.	Use with this pin set to OFF.		OFF
6	Always OFF.	Use with this pin set to OFF.		OFF

■ Duplex CPU Systems (CS1D-CPU67HA)

Pin No.	Function	Application	Default
4	See table below.	Used in Duplex of the CS1D-CPU67HA with the CS1D-CPU67H or the CPU65H. **Note** The CPU Unit will not operate if it is turned ON while "Cannot be used" has been set (Cannot be connected to the Programming Device as well).	OFF
5			OFF
6			OFF

Duplex CPU compatible setting	No.		
	SW4	SW5	SW6
CS1D-CPU67HA (no setting)	OFF	OFF	OFF
CPU67H mode	ON	OFF	ON
CPU65H mode	ON	ON	OFF
(Use prohibited)	Other than above		

■ Single CPU Systems

Pin No.	Setting	Function	Application	Default
4	ON	Peripheral port communications parameters set in the PLC Setup are used.	Turn ON to use the peripheral port for a device other than Programming Console or CX-Programmer (Peripheral bus only).	OFF
	OFF	Peripheral port communications parameters set using Programming Console or CX-Programmer (Peripheral bus only) are used.		
5	ON	RS-232C port communications parameters set using a CX-Programmer (Peripheral bus only) are used.	Turn ON to use the RS-232C port for a Programming Device.	OFF
	OFF	RS-232C port communications parameters set in the PLC Setup are used.		
6	ON	User-defined pin. Turns OFF the User DIP Switch Pin Flag (A39512).	Set pin 6 to ON or OFF and use A39512 in the program to create a user-defined condition without using an I/O Unit.	OFF
	OFF	User-defined pin. Turns ON the User DIP Switch Pin Flag (A39512).		

⚠ **Caution** Always touch a grounded metal object to discharge static electricity from your body before changing the settings on the DIP switch during operation.

Note

1. When pin 1 is set to ON, writing is prohibited for the user program and all parameter data (PLC Setup, I/O table registration, etc.). Moreover, it is not possible to clear the user program or parameters even by executing a memory clear operation from a Programming Device.
2. In a Duplex CPU System, automatic transfer at startup can be executed only from the active CPU Unit. Duplex initialization is performed between the two CPU Units after the automatic transfer, and the user program, parameters, and I/O memory are matched. If pin 2 it set to ON, I/O memory (AUTOEXEC.IOM, ATEXEC□□.IOM) will also be transferred automatically. (Refer to the *Programming Manual*.) The program (AUTOEXEC.OBJ) and Parameter Area (AUTOEXEC.STD) must both be on the Memory Card, but the I/O memory (AUTOEXEC.IOM, ATEXEC□□.IOM, AUTOEM□□.IOM) does not need to be.
3. Simple Backup Operations
   In Duplex Mode, the simple backup function can be executed only from the active CPU Unit. Duplex initialization is not executed between the two CPU Units after simple backup is performed. Therefore, after the data has been read to the CPU Unit, turn the power OFF and back ON and then press the Initial Switch on the Duplex Unit. If DIP switch pin 7 on the active CPU Unit is ON, a duplex verification error will occur.

Pin 7 of DIP switch on CPU Unit	Simple backup operation	Procedure
ON	Writing from active CPU Unit to Memory Card	Hold down the Memory Card Power Supply Switch for three seconds.
	Reading from Memory Card to active CPU Unit	Turn PLC power OFF and then back ON. This setting is given priority over automatic transfer at startup (pin 2 ON).
OFF (default)	Comparison of Memory Card and CPU Unit	Hold down the Memory Card Power Supply Switch for three seconds.

Note After the simple backup operation has been used to read data from the Memory Card to the CPU Unit, the operating mode will remain in PROGRAM mode and cannot be changed to MONITOR or RUN mode until the PLC power is turned OFF.

After reading the data to the PLC with the simple backup operation, turn OFF the power, turn OFF DIP switch pin 7, and then turn the power back ON.

2-4-3 CPU Unit Memory Map

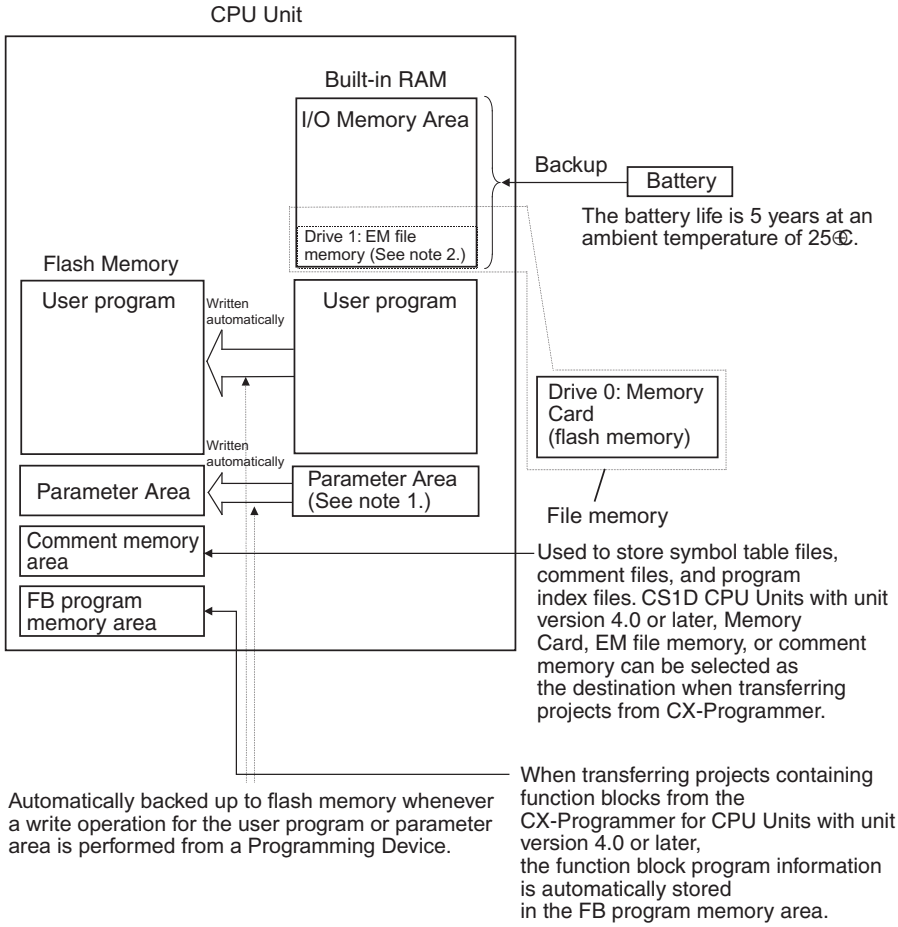
The memory of CS1D CPU Units is configured in the following blocks.

- I/O Memory: The data areas accessible from the user program
- User Memory: The user program and Parameter Area (See note 1.)

The above memory is backed up using a CS1W-BAT01 Battery. If the battery voltage is low, the data in these areas will not be stable.

The CPU Unit has a built-in flash memory, however, to which the user program and Parameter Area data is backed up whenever the user memory is written to, including data transfers and online editing from a Programming Device (CX-Programmer or Programming Console, data transfers from a

Memory Card, etc.). The user program and the Parameter Area data will thus not be lost even if battery voltage drops.



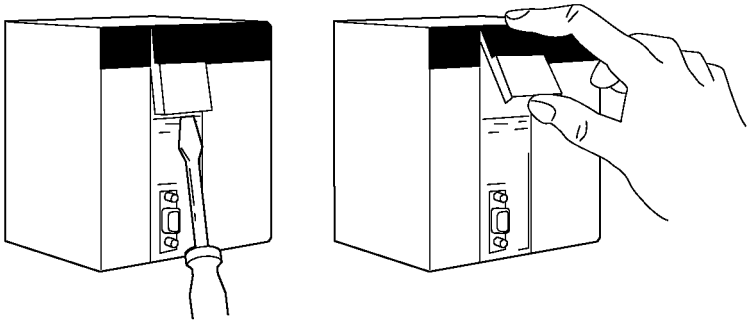
Note

1. The Parameter Area stores system information for the CPU Unit, such as the PLC Setup.
2. Part of the EM (Extended Data Memory) Area can be converted to file memory to handle data files and program files in RAM memory format, which has the same format as Memory Cards. File memory in the EM Area is backed up by a battery.

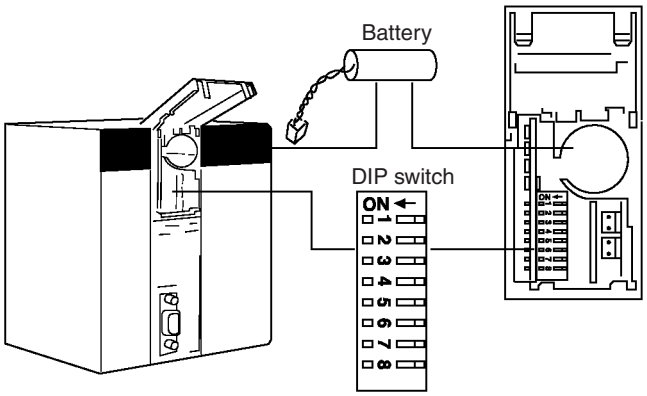
2-4-4 Battery Compartment and Peripheral Port Covers

Opening the Battery Compartment Cover

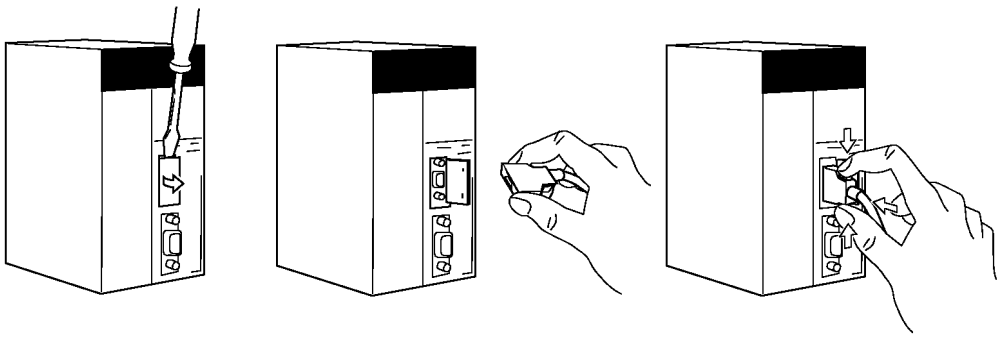
Insert a small flat-blade screwdriver into the opening at the bottom of the battery compartment cover and lift open the cover.



Insert a small flat-blade screwdriver into the opening at the bottom of the battery compartment cover and lift open the cover.



Opening the Peripheral Port Cover and Connecting Cables

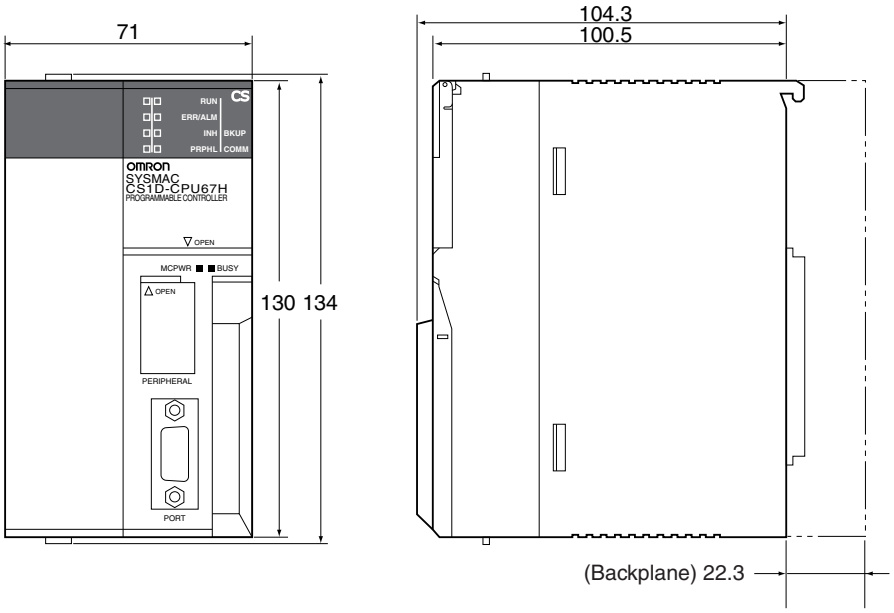


Insert a small flat-blade screwdriver into the opening at the top of the port cover and pull open.

Make sure the connector is in facing the correct direction.

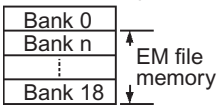
Hold the grips on the side of the connector and push into the port.

2-4-5 Dimensions



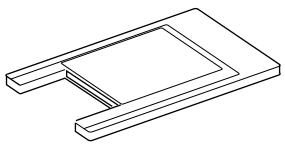
2-5 File Memory

For CS1D CPU Units, the Memory Card and a specified part of the EM Area can be used to store files. All user programs, the I/O Memory Area, and the Parameter Area can be stored as files.

File memory	Memory type	Memory capacity	Model
Memory Card (See note 3.) 	Flash memory	128 Mbytes	HMC-EF183
		256 Mbytes	HMC-EF283
		512 Mbytes	HMC-EF583
EM file memory 	RAM	The maximum capacity of the CPU Unit's EM Area CPU68HA: 1600 KB CPU67HA/SA/H/S: 832 KB CPU65H/S: 192 KB CPU44SA/S: 64 KB CPU42S: 64 KB	The specified bank (set in the PLC Setup) to the last bank of the EM Area in the I/O Memory.

Note

1. A Memory Card can be written up to approximately 100,000 times. (Each write operation to the Memory Card must be counted regardless of the size of the write.) Be particularly careful not to exceed the service life of the Memory Card when writing to it from the ladder program.
2. The HMC-AP001 Memory Card Adapter is shown below.



3. For precautions regarding the use of Memory Cards, refer to *5-1 File Memory* in the *SYSMAC CS/CJ/NSJ Series Programmable Controllers Programming Manual* (W394).

2-5-1 File Memory Functions in Duplex CPU Systems

Only the Memory Card in the active CPU Unit is accessed, whereas EM file memory is accessed for both the active and standby CPU Units.

Using Memory Cards

Operation in a Duplex CPU System

Memory Card functions can be executed in duplex only when the doing so is enabled in the PLC Setup. In Duplex Mode, the same data that is written to the Memory Card mounted in the active CPU Unit will also be written to the Memory Card in the standby CPU Unit. No processing, however, is executed during duplex initialization to match the data on the Memory Cards mounted in the active and standby CPU Units. Therefore, before enabling duplex operation for Memory Cards, make sure that the contents are the same for both of the Memory Cards.

Data read from the Memory Card mounted in the active CPU Unit is used by both the active and standby CPU Units, so this ensures that the data for the two CPU Units will match.

Memory Card Functions The following table shows the operations of the various Memory Card-related functions.

Function	Memory Card location		Data unification processing method	Notes
	Installed in active CPU Unit	Installed in standby CPU Unit		
Writing to Memory Card using the FWRIT instruction	Accessed.	Accessed. (Same data written as for active CPU Unit.)	Data is written to the Memory Cards mounted in both CPU Units.	When referencing file memory-related status, use the status for the active CPU Unit (word A343).
Reading from Memory Card using the FREAD instruction		Not accessed.	Data read from the Memory Card in the active CPU Unit is used by both CPU Units.	
Automatic transfer when power is turned ON			After the automatic transfer at startup, duplex initialization is executed between the two CPU Units, and the user program, parameters, and I/O memory are matched.	There is no need to mount a Memory Card or to set the DIP switch at the standby CPU Unit.
Replacement of the Entire Program During Operation			Simultaneously with program replacement during operation, duplex operation is initialized between the two CPU Units, and the user programs are matched.	
Simple backup			Duplex operation is not initialized between the CPU Units after reading to the CPU Units.	After data is read from the Memory Card by the simple backup operation, the CPU Unit will be in PROGRAM mode. (CS-series specifications) To begin the operation: 1. Turn OFF the power and set DIP switch pins 7 and 8 on the CPU Units. Then turn the power back ON. 2. Press the Initial Switch on the Duplex Unit. **Note** If pin 7 on the active CPU Unit is turned ON, a duplex verification error will be generated.

Note For details, refer to the *CS/CJ-series Programming Manual*.

Using EM File Memory

Operation in a Duplex CPU System When a file is written to the EM file memory in the active CPU Unit in a Duplex System, the same file is simultaneously written to the EM file memory in the standby CPU Unit.

Note If EM file memory is specified for the active CPU Unit's EM Area with the PLC Setup, the same banks will be specified for the standby CPU Unit's EM Area by means of duplex initialization.

EM File Memory-related Functions

The following table shows the operations of the EM file memory-related functions.

Function	EM file memory		Data matching method	Note
	In active CPU Unit	In standby CPU Unit		
Writing to EM file memory by FWRIT instruction	Accessed.	Accessed	When a file is written to the active CPU Unit's EM file memory, the file is simultaneously written to the standby CPU Unit's EM file memory. FWRIT instruction execution is synchronized for the active and standby CPU Units.	When referencing file memory-related status, use the status for the active CPU Unit (word A343).
Reading from EM file memory by FREAD instruction		Not accessed.	The FREAD instruction is executed for both CPU Units, and the data read from the active CPU Unit's EM file memory is used by both CPU Units.	

2-5-2 Files Handled by CPU Unit

Files are ordered and stored in the Memory Card or EM file memory according to the file name and the extension attached to it. File names handled by the CPU Unit (i.e., file names that can be read) are set as shown in the following tables.

General-use Files

File type	Contents		File name	Extension
Data files	Specified range in I/O memory	Binary	********	.IOM
		Text		.TXT
		CSV		.CSV
Program files	All user programs		********	.OBJ
Parameter files	PLC Setup, registered I/O tables, routing tables, CPU Bus Unit settings, SYSMAC LINK link tables, and Controller Link link tables		********	.STD

Files Transferred Automatically at Startup

File type	Contents		File name
Data files	DM Area data (stores data for specified number of words starting from D20000)	AUTOEXEC	.IOM
	DM Area data (stores data for specified number of words starting from D00000)	ATEXECDM	.IOM
	EM area for bank No. □ (stores data for specified number of words starting from E□_00000)	ATEXECE□ (EM bank No.0 to C(Hex))	.IOM
	EM area for bank No. □ (stores data for specified number of words starting from E□_00000) **Note** CS1D-CPU68HA only	AUTOEM□□ (□□: EM bank No.0D to 18(Hex))	.IOM
Program files	All user programs	AUTOEXEC	.OBJ
Parameter files	PLC Setup, registered I/O tables, routing tables, CPU Bus Unit settings, SYSMAC LINK link tables, and Controller Link link tables	AUTOEXEC	.STD

Simple Backup Files

File type	Contents		File name
Data files	Words allocated to Special I/O Units, CPU Bus Units, and Inner Boards in the DM Area	BACKUP	.IOM
	CIO area	BACKUPIO	.IOR
	DM Area	BACKUPDM	.IOM
	EM area	BACKUPE□ (□: EM bank No.0 to C(Hex))	.IOM
	EM area **Note** CS1D-CPU68HA only	BKUPEM□□ (□□: EM bank No.0D to 18(Hex))	.IOM
Program files	All user programs	BACKUP	.OBJ
Parameter files	PLC Setup, registered I/O tables, routing tables, CPU Bus Unit settings, SYSMAC LINK link tables, and Controller Link link tables		.STD
Unit/Board backup files	Data from specific Units or Boards	BACKUP□□ (□□: Unit address)	.PRM

Note
1. Specify up to eight ASCII characters.
2. Always specify the name of files to be transferred automatically at startup as AUTOEXEC or ATEXEC□□.
3. The Units and Boards use the following file names.

Unit/Board	□□	Unit No.
CPU Bus Units	I0 to IF	0 to F
Special I/O Units	20 to 6F	0 to 79
Inner Boards	E1	---

2-5-3 Initializing File Memory

File memory	Initializing procedure	Data capacity after initialization
Memory Card	1. Install Memory Card into CPU Unit. 2. Initialize the Memory Card using a Programming Device (including Programming Console).	Essentially the specific capacity of the Memory Card
EM file memory	1. Convert the part of the EM Area from the specified bank No. to the last bank No. to file memory in the PLC Setup. 2. Initialize the EM file memory using a Programming Device (excluding Programming Console).	1 bank: Approx. 61 KB 13 banks: Approx. 825 KB

Note To delete all of the contents of a Memory Card, or to format the Memory Card, use either a CX-Programmer or Programming Console with the CPU Unit. Do not use a personal computer for this purpose.

2-5-4 Using File Memory

Note For details on using file memory, refer to the CS/CJ-series *Programming Manual.*

Memory Cards

Reading/Writing Files Using Programming Device

File	File name and extension	Data transfer direction
Program files	********.OBJ	Between CPU Unit and Memory Card,
I/O memory files	********.IOM	
Parameter files	********.STD	

1,2,3... 1. Install the Memory Card into the CPU Unit.
2. Initialize the Memory Card if necessary.
3. Name the file containing the data in the CPU Unit and save the contents in the Memory Card.
4. Read the file that is saved in the Memory Card to the CPU Unit.

Automatically Transferring Memory Card Files to the CPU Unit at Startup

File	File name and extension	Data transfer direction
Program files	AUTOEXEC.OBJ	From Memory Card to CPU Unit
I/O memory files	AUTOEXEC.IOM ATEXECDM.IOM ATEXECE□.IOM (□: EM bank No.0 to C(Hex)) AUTOEM□□.IOM (□□: EM bank No.0D to 18(Hex))	
Parameter files	AUTOEXEC.STD	

1,2,3... 1. Install the Memory Card into the CPU Unit.
2. Set pin 2 of the DIP switch to ON.
3. The files are read automatically when the power is turned ON.

Reading/Writing I/O Memory Files inside the Memory Card Using (FREAD(700), FWRIT(701), and TWRIT(704)) Instruction for File Memory

File	File name and extension	Data transfer direction
I/O memory files	********.IOM ********.TXT ********.CSV	Between CPU Unit and Memory Card

1,2,3... 1. Install the Memory Card into the CPU Unit.
2. Initialize the Memory Card using a Programming Device.
3. Using the FWRIT(701) instruction, name the file of the specified I/O memory area, and save to the Memory Card.
4. Using the FREAD(700) instruction, read the I/O memory files from the Memory Card to the I/O memory in the CPU Unit.

Note When using spreadsheet software to read data that has been written to the Memory Card in CSV or text format, it is now possible to read the data using Windows applications by mounting a Memory Card in the personal computer card slot using a HMC-AP001 Memory Card Adapter.

Reading and Replacing Program Files during Operation

File	File name and extension	Data transfer direction
Program files	********.OBJ	Memory Card to CPU Unit

1,2,3... 1. Install a Memory Card into the CPU Unit.
2. Set the following information: Program File Name (A654 to A657) and Program Password (A651).
3. Next, from the program, turn ON the Replacement Start Bit (A65015).

Backing Up or Restoring CPU Unit Data or Data for Specific Units and Boards

File	File name and extension	Data transfer direction
Program files	BACKUP.OBJ	CPU Unit to Memory Card (when backing up) Memory Card to CPU Unit (when restoring)
Data files	BACKUP.IOM	
	BACKUPIO.IOR	
	BACKUPDM.IOM	
	BACKUPE□.IOM	
	BKUPEM□□.IOM (□: EM bank No.)	
Parameter files	BACKUP.STD	
Unit/Board backup files	BACKUP□□.PRM (□□: unit No.)	

1,2,3... 1. Install a Memory Card into the CPU Unit.
2. Turn ON pin 7 and turn OFF pin 8 on the DIP switch.
3. To back up data, press and hold the Memory Card Power Supply Switch for three seconds. To restore data, turn ON the PLC power.

Note The following files can be transferred between the Memory Card and the CX-Programmer.

File	File name and extension	Data transfer direction
Symbols file	SYMBOLS.SYM	Between CX-Programmer and Memory Card
Comment file	COMMENTS.CMT	

1,2,3... 1. Insert a formatted Memory Card into the CPU Unit.
2. Place the CX-Programmer online and use the file transfer operations to transfer the above files from the personal computer to the PLC or from the PLC to the personal computer.

EM File Memory

Reading/Writing EM File Memory Files Using Programming Device

File	File name and extension	Data transfer direction
Program files	********.OBJ	Between CPU Unit and EM file memory
I/O memory files	********.IOM	
Parameter files	********.STD	

1,2,3... 1. Convert the part of the EM Area specified by the first bank number into file memory in the PLC Setup.
2. Initialize the EM file memory using a Programming Device.
3. Name the data in the CPU Unit and save in the EM file memory using the Programming Device.
4. Read the EM file memory files to the CPU Unit using the Programming Device.

Reading/Writing I/O Memory Files inside the EM File Memory Using (FREAD(700), FWRIT(701), and TWRIT(704)) Instruction for File Memory

File	File name and extension	Data transfer direction
I/O memory files	********.IOM	Between CPU Unit and EM file memory

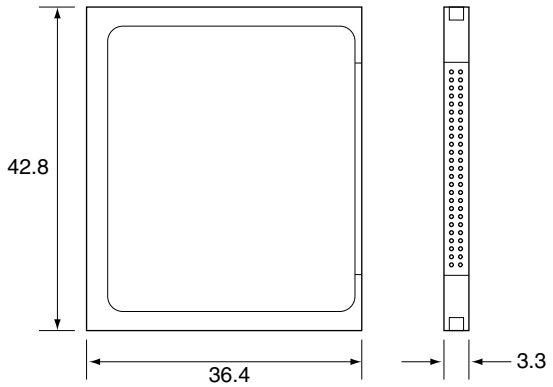
1,2,3... 1. Convert the part of the EM Area specified by the first bank number into file memory in the PLC Setup.
2. Initialize the EM file memory using a Programming Device.
3. Using the FWRIT(701) instruction, name the specified area in I/O memory with a file name and save in the EM file memory.
4. Using the FREAD(700) instruction, read the I/O memory files from the EM file memory to the I/O memory in the CPU Unit.

Note The following files can be transferred between EM file memory and the CX-Programmer.

File	File name and extension	Data transfer direction
Symbols file	SYMBOLS.SYM	Between CX-Programmer and EM file memory
Comment file	COMMENTS.CMT	

1,2,3... 1. Format the EM Area in the CPU Units as file memory.
2. Place the CX-Programmer online and use the file transfer operations to transfer the above files from the personal computer to the PLC or from the PLC to the personal computer.

2-5-5 Memory Card Dimensions

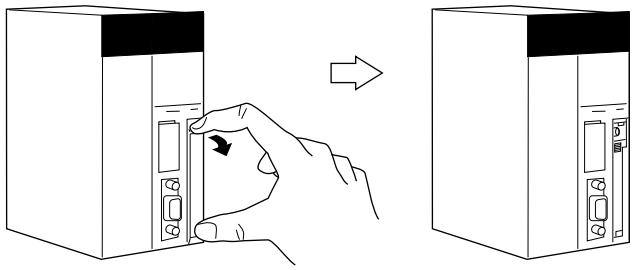


2-5-6 Installing and Removing the Memory Card

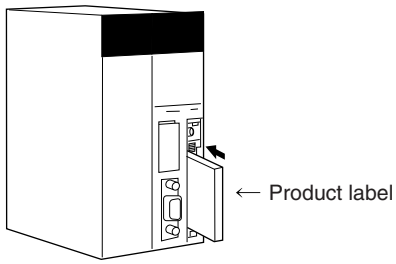
Installing the Memory Card

Note In a Duplex CPU System, install the Memory Card into the active CPU Unit. Even if Memory Cards are mounted in both CPU Units, there will be no duplex initialization to match the data on the two Memory Cards. Therefore there is no guarantee that operation will continue after an operation switching error.

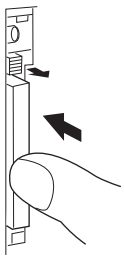
1,2,3... 1. Pull the top end of the Memory Card cover forward and remove from the Unit.



2. Insert the Memory Card with the label facing to the right. (Insert with the Δ on the Memory Card label and the ◁ on the CPU Unit facing each other.)

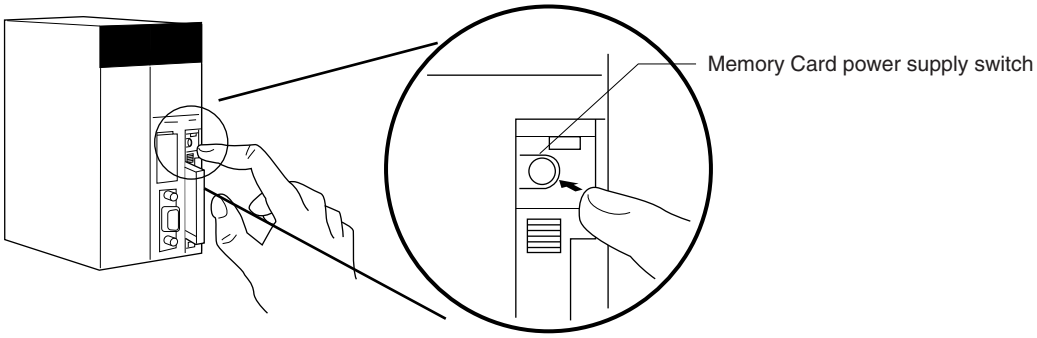


3. Push the Memory Card securely into the compartment. If the Memory Card is inserted correctly, the Memory Card eject button will be pushed out.

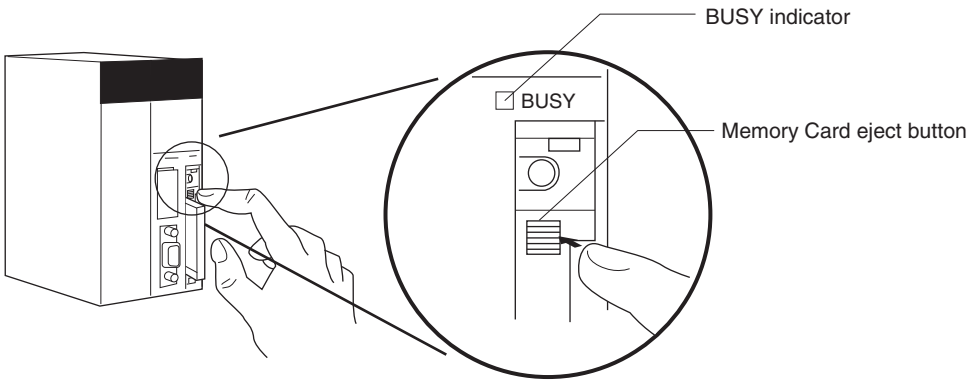


Removing the Memory Card

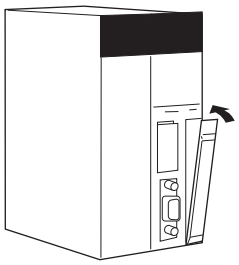
1,2,3... 1. Press the Memory Card Power Supply Switch.



2. Press the Memory Card eject button after the BUSY indicator is no longer lit.

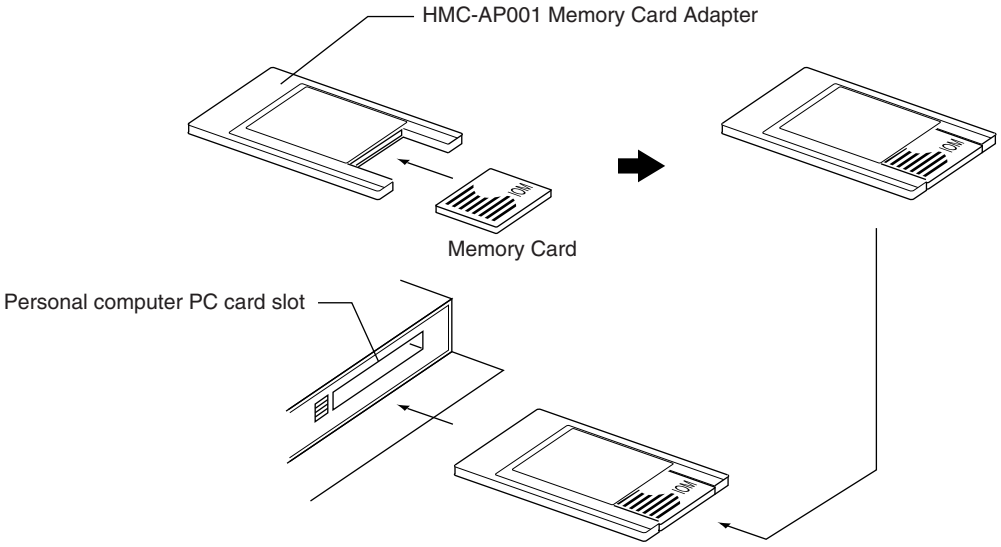


3. The Memory Card will eject from the compartment.
4. Remove the Memory Card cover when a Memory Card is not being used.



Note
1. Never turn OFF the PLC while the CPU is accessing the Memory Card.
2. Never remove the Memory Card while the CPU is accessing the Memory Card. Press the Memory Card Power Supply Switch and wait for the BUSY indicator to go OFF before removing the Memory Card. In the worst case, the Memory Card may become unusable if the PLC is turned OFF or the Memory Card is removed while the Card is being accessed by the CPU.
3. Never insert the Memory Card facing the wrong way. If the Memory Card is inserted forcibly, it may become unusable.

Installing the Memory Card into a Personal Computer



Note When a Memory Card is inserted into a computer using a Memory Card Adapter, it can be used as a standard storage device, like a floppy disk or hard disk.

2-6 Programming Devices

2-6-1 Overview

There are two types of Programming Devices that can be used: the Hand-held Programming Consoles or the CX-Programmer, which is operated on a Windows computer. The CX-Programmer is usually used to write the programs, and a Programming Console is then used to change the operating modes, edit the programs, and monitor a limited number of points.

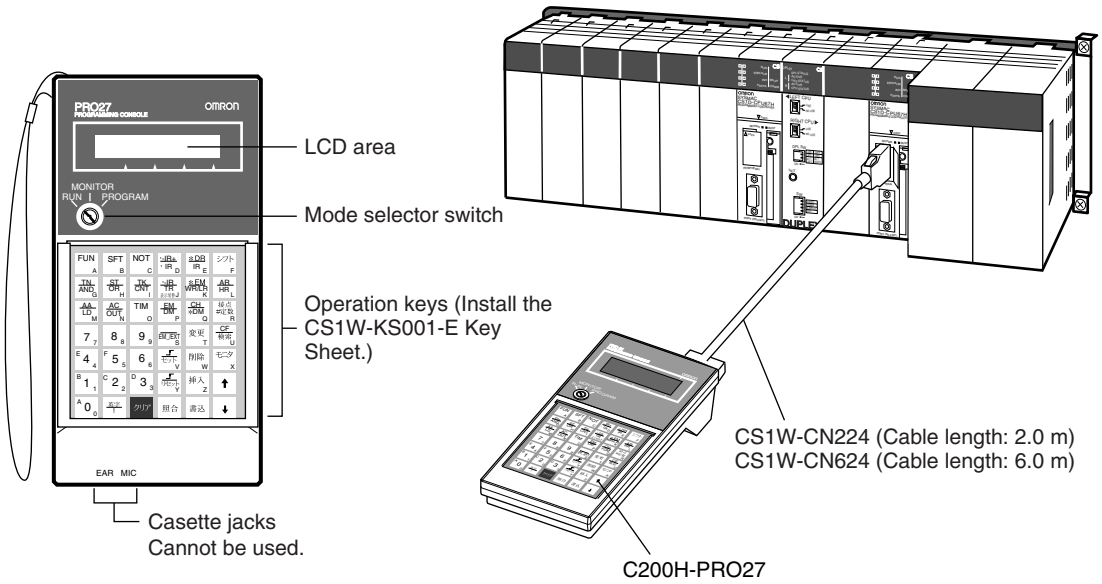
Use one of the following methods to connect the Programming Devices to a CS1D CPU Unit.

- Programming Console:
  Connect to the peripheral port of the CPU Unit. Online replacement is possible for Units mounted to a CS1D CPU Rack or CS1D Expansion Rack.
- CX-Programmer:
  Connect to the peripheral port or RS-232C port.

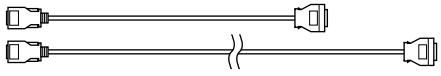
Note In a Duplex CPU System, the Programming Device must be connected to the active CPU Unit.

Programming Consoles

C200H-PRO27-E Programming Console



Connect the CPU Unit to the Programming Console with the following cables.
CS1W-CN224 (Cable length: 2.0 m)
CS1W-CN624 (Cable length: 6.0 m)



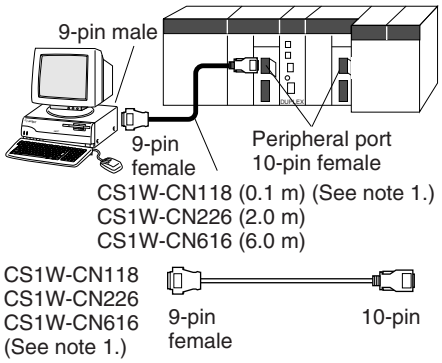
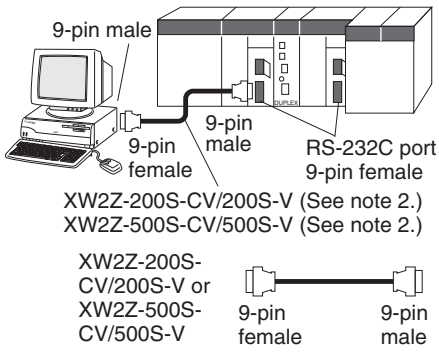
CX-Programmer

There are differences in functions depending on the version of CX-Programmer connected to the CS1D PLC. These are listed in the following table.

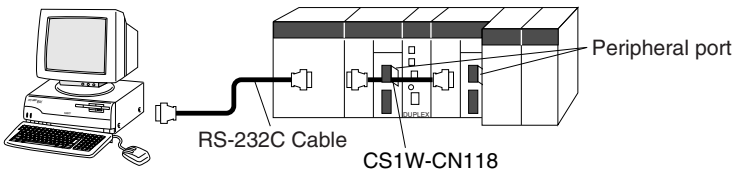
CX-Programmer	Duplex CPU Systems	Single CPU Systems	Remarks
Version 2.□ or lower	Not supported.	Not supported.	This version cannot be used for CS1D PLCs.
Version 3.□	Supported.	Not supported.	Online Unit replacement is supported for version 3.1 or higher. Select “CS1H-H” as the device type. When using duplex functions, select ***Duplex Settings*** from the Option Menu in the PLC Setup. Not supported in CS1D-CPU□□HA. Single CPU Systems are not supported.
Version 4.□ or higher	Supported.	Supported.	Select “CS1D-S” as the device type when using a Single CPU System. In CS1D-CPU□□H, select the PLC model "CS1D-H." The “CS1H-H” can also be selected as the device type, but if it is, then ***Duplex Settings*** must be selected from the Option Menu in the PLC Setup. Supported if the PLC model: "CS1D-H" is selected in CS1D-CPU□□HA. **Note** CS1D-CPU□□HA requires Ver. 9.7 or later.

For the main specifications of CX-Programmer, refer to the manual of your CX-Programmer.

Connections

Personal computer	Peripheral port connection	RS-232C port connection
IBM PC/AT or compatible		

Note 1. The CS1W-CN118 Cable is used with one of the RS-232C Cables shown on the right (XW2Z-□□□S-□□) to connect to the peripheral port on the CPU Unit.



2. If cables with model numbers ending in -V instead of -CV are used to connect the computer running the CX-Programmer to the RS-232C port (including when using a CS1W-CN118 Cable), a peripheral bus connection cannot be used. Use a Host Link (SYSWAY) connection. To connect to the port using a peripheral bus connection, prepare an RS-232C cable as described in *Connection Methods* on page 81.

CX-Programmer Connecting Cables

Unit	Unit port	Computer	Computer port	Serial communications mode	Model	Length	Cable notes
CPU Units	Peripheral port	IBM PC/AT or compatible	D-Sub, 9-pin, male	Peripheral bus or Host Link	CS1W-CN226	2.0 m	---
					CS1W-CN626	6.0 m	
	Built-in RS-232C port D-Sub, 9-pin, female	IBM PC/AT or compatible	D-Sub, 9-pin, male	Peripheral bus or Host Link	XW2Z-200S-CV	2 m	Use a static-resistant connector.
					XW2Z-500S-CV	5 m	
Serial Communications Boards/Units (See note 1.)	RS-232C Port D-Sub, 9-pin, female	IBM PC/AT or compatible	D-Sub, 9-pin, male	Host Link	XW2Z-200S-CV	2 m	Use a static-resistant connector.
					XW2Z-500S-CV	5 m	

Note

1. Serial Communications Boards are supported only for Single CPU Systems.
2. Before connecting a connector from the above table to a PLC RS-232C port, touch a grounded metal object to discharge static electricity from your body. The XW2Z-□□□S-CV Cables have been strengthened against static because they use a static-resistant connector hood (XM2S-0911-E). Even so, always discharge static electricity before touching the connectors.
3. Do not use commercially available RS-232C personal computer cables. Always use the special cables listed in this manual or make cables according to manual specifications. Using commercially available cables may damage the external devices or CPU Unit.

RS-232C Cables for a Peripheral Port

Unit	Unit port	Computer	Computer port	Serial communications mode	Model	Length	Cable notes
CPU Units	Built-in peripheral port	IBM PC/AT or compatible	D-Sub, 9-pin, male	Peripheral bus or Host Link	CS1W-CN118 + XW2Z-200S-CV/500S-CV	0.1 m+ (2 m or 5 m)	XW2Z-□□□S-CV models use a static - resistant connector.

Using a CQM1-CIF01/02 Cable for a Peripheral Port

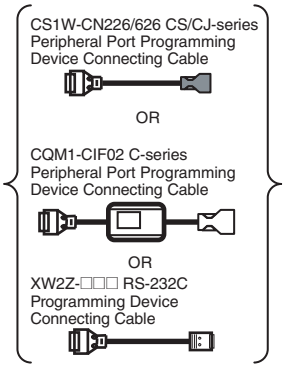
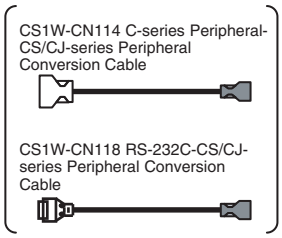
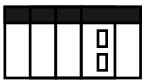
Unit	Unit port	Computer	Computer port	Serial communications mode	Model	Length	Cable notes
CPU Units	Built-in peripheral port	IBM PC/AT or compatible	D-Sub, 9-pin, male	Host Link	CS1W-CN114 + CQM1-CIF02	0.05 m + 3.3 m	---

Using an RS-232C Cable for an IBM PC/AT or Compatible

Unit	Unit port	Computer	Computer port	Serial communications mode	Model	Length	Cable notes
CPU Units	Built-in RS-232C port D-Sub, 9-pin, female	IBM PC/AT or compatible	D-Sub, 9-pin, male	Host Link	XW2Z-200S-V	2 m	---
					XW2Z-500S-V	5 m	
Serial Communications Boards/Units (See note.)	RS-232C port D-Sub, 9-pin, female	IBM PC/AT or compatible	D-Sub, 9-pin, male	Host Link	XW2Z-200S-V	2 m	
					XW2Z-500S-V	5 m	

Note Serial Communications Boards are supported only for Single CPU Systems.

Connection Method for USB-Serial Conversion Cable

Computer	CS1W-CIF31		Cable 1		Cable 2	PLC
		+		+		

CX-Programmer Connecting Cables

Cables Connecting to CPU Units

USB Connecting Cable Model	Cable 1			Cable 2			Unit port	Serial communications mode (network)
	Connector	Cable model	Connector	Connector	Cable model	Connector		
CS1W-CIF31	D-sub, 9-pin female	CS1W-CN226/626 (length: 2 m/6 m)	CS/CJ-series peripheral	Not required.			CS/CJ-series peripheral	Peripheral Bus (Toolbus) or Host Link (SYSWAY)
		CQM1-CIF02 (length: 3.3 m)	C-series peripheral	C-series peripheral	CS1W-CN114 (length: 5 cm)	CS/CJ-series peripheral		Host Link (SYSWAY)
		XW2Z-200S-V/500S-V (length: 2 m/5 m)	D-sub, 9-pin male	D-sub, 9-pin female	CS1W-CN118 (length: 0.1 m)	CS/CJ-series peripheral		Peripheral Bus (Toolbus) or Host Link (SYSWAY)
		XW2Z-200S-V/500S-V (length: 2 m/5 m	D-sub, 9-pin male	D-sub, 9-pin female	CS1W-CN118 (length: 0.1 m)	CS/CJ-series peripheral		Host Link (SYSWAY)
		XW2Z-200S-CV/500S-CV (length: 2 m/5 m)	RS-232C D-sub, 9-pin male	Not required.			RS-232C D-sub, 9-pin female	Peripheral Bus (Toolbus) or Host Link (SYSWAY)
		XW2Z-200S-V/500S-V (length: 2 m/5 m)	RS-232C D-sub, 9-pin male	Not required.				Host Link (SYSWAY)

Peripheral Port Specifications

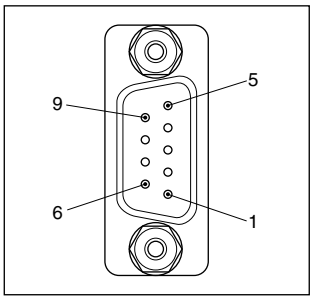
Protocol PLC Setup and Duplex Unit DIP Switch Settings

PRPHL	Peripheral port settings (in PLC Setup)			
	Default value: 0 hex	NT Link: 2 hex	Peripheral bus: 4 hex	Host Link: 5 hex
OFF	Programming Console or CX-Programmer through peripheral bus (automatically detects the Programming Device's communications parameters)			
ON	Host computer or CX-Programmer (Host Link)	PT (NT Link)	CX-Programmer (peripheral bus)	Host computer or CX-Programmer (Host Link)

RS-232C Port Specifications

Connector Pin Arrangement

Pin No.	Signal	Name	Direction
1	FG	Protection earth	---
2	SD (TXD)	Send data	Output
3	RD (RXD)	Receive data	Input
4	RS (RTS)	Request to send	Output
5	CS (CTS)	Clear to send	Input
6	5 V	Power supply	---
7	DR (DSR)	Data set ready	Input
8	ER (DTR)	Data terminal ready	Output
9	SG (0 V)	Signal ground	---
Connector hood	FG	Protection earth	---

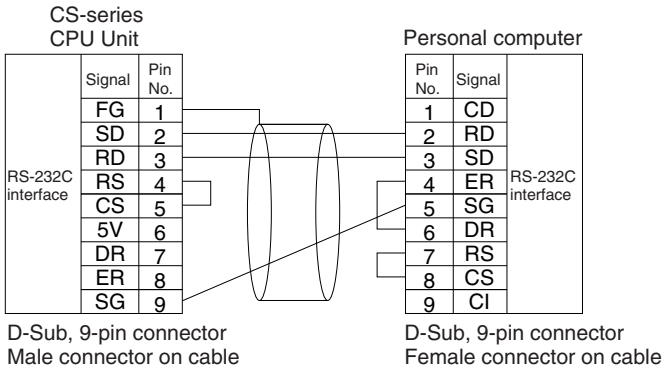


Note Do not use the 5-V power from pin 6 of the RS-232C port for anything but an NT-AL001 Link Adapter, CJ1W-CIF11 Conversion Adapter, or NV3W-M□20L Programmable Terminal. Using this power supply for any other external device may damage the CPU Unit or external devices.

Connection Methods

Connection between CPU Unit and Personal Computer

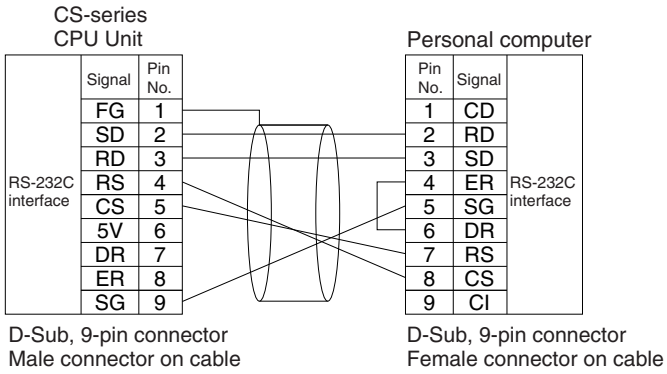
The following connections are in Host Link serial communications mode.



Note

1. Refer to *Connection Examples* under *Appendix F Connecting to the RS-232C Port on the CPU Unit* when converting between RS-232C and RS-422A/485 for 1:N connections.
2. Refer to *Recommended Wiring Methods* under *Appendix F Connecting to the RS-232C Port on the CPU Unit* when making your own RS-232C cable.

The following connections are in peripheral bus serial communications mode.



Use the following connectors and cables when creating RS-232C cable for connecting to the RS-232C port.

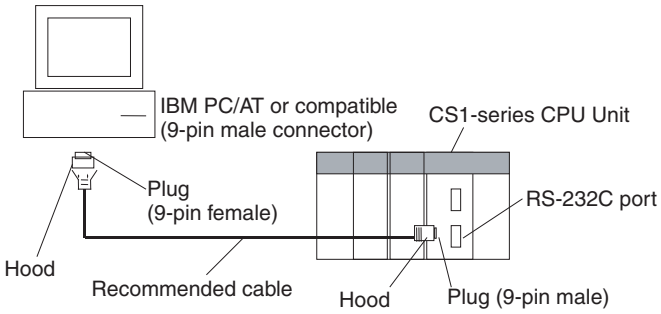
Applicable Connectors

CPU Unit Connector

Item	Model	Specifications	
Plug	XM3A-0921 or equivalent	9-pin male	Used together
Hood	XM2S-0911-E or equivalent	9-pin, millimeter screws	

Personal Computer Connector

Item	Model	Specifications	
Plug	XM3D-0921 or equivalent	9-pin female	Used together
Hood	XM2S-0913 or equivalent	9-pin, inch screws	



Note Use the special cables provided from OMRON for all connections whenever possible. If cables are produced in-house, be sure they are wired correctly. External devices and the CPU Unit may be damaged if general purpose (e.g., computer to modem) cables are used or if wiring is not correct.

Recommended Cables

Fujikura Ltd.:UL2464 AWG28 × 5P IFS-RVV-SB (UL product)
AWG 28 × 5P IFVV-SB (non-UL product)

Hitachi Cable, Ltd.: UL2464-SB(MA) 5P × 28AWG (7/0.127) (UL product)
CO-MA-VV-SB 5P × 28AWG (7/0.127) (non-UL product)

RS-232C Port Specifications

Item	Specification
Communications method	Half duplex
Synchronization	Start-stop
Baud rate	0.3/0.6/1.2/2.4/4.8/9.6/19.2/38.4/57.6/115.2 kbps (See note.)
Transmission distance	15 m max.
Interface	EIA RS-232C
Protocol	Host Link, NT Link, 1:N, No-protocol, or peripheral bus

Note Baud rates for the RS-232C are specified only up to 19.2 kbps. The CS Series supports serial communications from 38.4 kbps to 115.2 kbps, but some computers cannot support these speeds. Lower the baud rate if necessary.

Protocol PLC Setup and Duplex Unit DIP Switch Settings

COMM	RS-232C port settings (in PLC Setup)				
	Default value: 0 hex	NT Link: 2 hex	No protocol: 3 hex	Peripheral bus: 4 hex	Host Link: 5 hex
OFF	Host computer or CX-Programmer (Host Link)	PT (NT Link)	General-purpose external devices (No protocol)	CX-Programmer (peripheral bus)	Host computer or CX-Programmer (Host Link)
ON	CX-Programmer (not a Programming Console) connected through the peripheral bus. (The Programming Device's communications parameters are detected automatically.)				

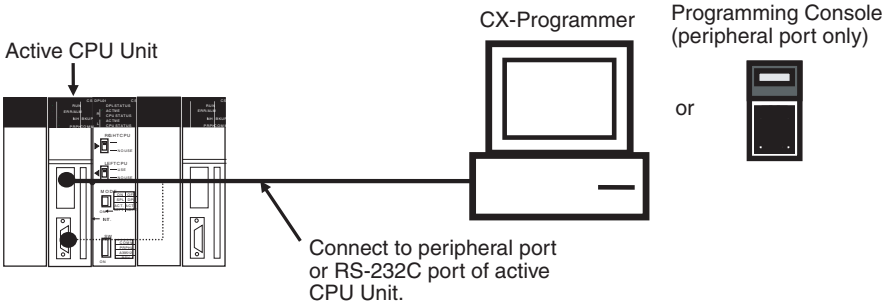
Note The location of the setting depends on the system.
Duplex CPU Systems: COMM switch on the front of the Duplex Unit.
Single CPU Systems: Pin 5 on the DIP switch on the front of the CPU Unit.

2-6-2 Precautions when Connecting Programming Devices to Duplex CPU Systems

This section describes factors that must be taken into account when connecting a CX-Programmer or a Programming Console to a CS1D Duplex System.

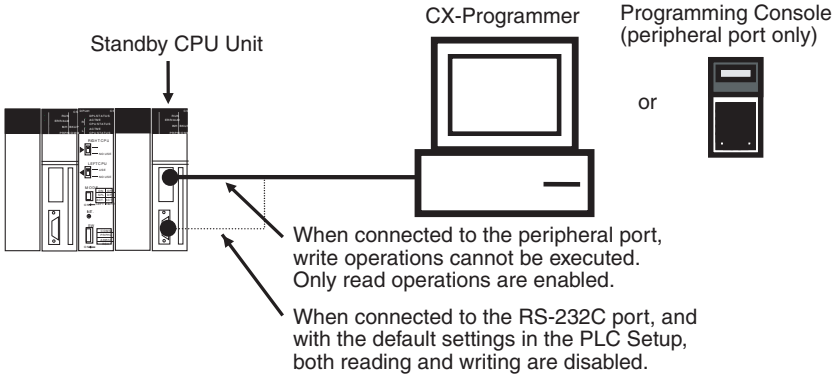
Connecting a Programming Device

With a Duplex CPU System, Programming Devices must be connected to a serial communications port (peripheral port or RS-232C port) of the active CPU Unit.



Note 1. If connected to the peripheral port of the standby CPU Unit, no writing can be executed from either the CX-Programmer or the Programming Console. Only reading is enabled. (The CX-Programmer cannot be used for operations such as changing operating modes, transferring user programs, transferring PLC Setup settings, changing I/O memory, creating and transferring I/O tables, performing online editing, and changing timer/counter settings.)

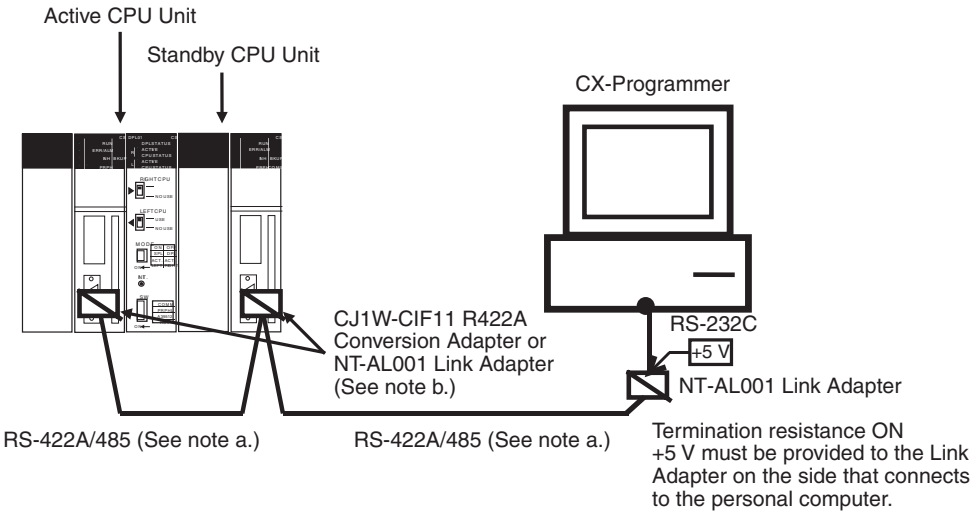
2. If connected to the RS-232C port of the standby CPU Unit, neither reading nor writing can be executed from the CX-Programmer. Reading only, however, can be enabled by means of the Standby CPU Unit RS-232C Port Setting in the PLC Setup.



Leaving CX-Programmer Connected Constantly to RS-232C Port

With a Duplex CPU Systems, communications will become possible if the CX-Programmer is left connected constantly only to the active CPU Unit, and an operation switching error occurs causing the active CPU Unit to become the standby CPU Unit.

For that reason, if the CX-Programmer is to be left connected, or if it is preferable to not have to reconnect the cable to the other CPU Unit when a switching error occurs, it is recommended that the following connection be used. For this, it is required that the Standby CPU Unit RS-232C Port Setting in the PLC Setup be set so that independent communications are disabled (i.e., the default setting).



Note a) Use shielded twisted-pair cable for the RS422A/RS-485 cable.

Model	Manufacturer
CO-HC-ESV-3P×7/0.2	Hirakawa Hewtech Corp.

b) The CJ1W-CIF11 does not provide isolation. The total length of the transmission path must therefore be 50 m or less. If the transmission distance is greater than 50 m, use the NT-AL001, which provides isolation, and do not include the CJ1W-CIF11 in the

transmission path. When only the NT-AL001 is used, the total length of the transmission path can be a maximum of 500 m.

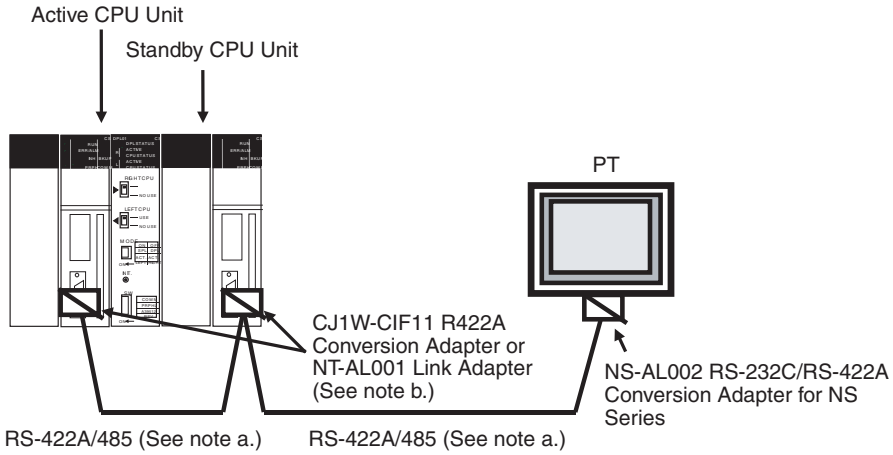
Leaving a PT or Host Computer Connected Constantly to RS-232C Port

If a PT (Programmable Terminal) or host computer (running SCADA software) is left connected constantly for monitoring a Duplex CPU System, and if the connection is only to the active CPU Unit, then writing will become impossible when an operation switching error occurs and the active CPU Unit becomes the standby CPU Unit.

For that reason, it is recommended that the following connection be used. For this, it is required that the Standby CPU Unit RS-232C Port Setting in the PLC Setup be set so that independent communications are disabled (i.e., the default setting).

PT Connection Example

In this example, communications between the CPU Unit and the PT are continued even after an operation switching error occurs.



Note a) Use shielded twisted-pair cable for the RS422A/RS-485 cable.

Model	Manufacturer
CO-HC-ESV-3P×7/0.2	Hirakawa Hewtech Corp.

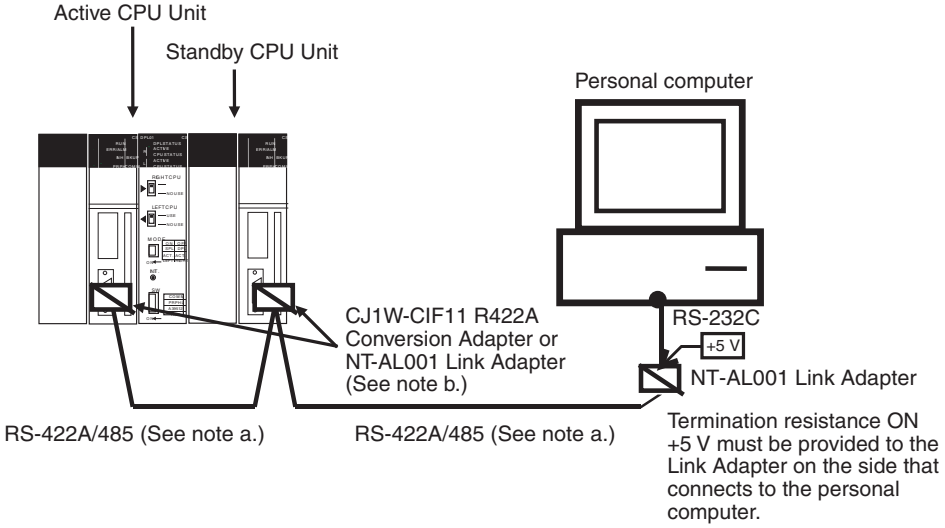
b) The CJ1W-CIF11 does not provide isolation. The total length of the transmission path must therefore be 50 m or less. If the transmission distance is greater than 50 m, use the NT-AL001, which provides isolation, and do not include the CJ1W-CIF11 in the transmission path. When only the NT-AL001 is used, the total length of the transmission path can be a maximum of 500 m.

Note

1. The above Conversion Adapter is not required for the RS-422A/RS-485 port at the PT.
2. When the CPU Units are switched, communications may be momentarily interrupted, so enable communications retries in the PT communications settings.

Personal Computer Connection Example

In this example, communications between the CPU Unit and the personal computer are continued even after an operation switching error occurs.



Note a) Use shielded twisted-pair cable for the RS422A/RS-485 cable.

Model	Manufacturer
CO-HC-ESV-3P×7/0.2	Hirakawa Hewtech Corp.

b) The CJ1W-CIF11 does not provide isolation. The total length of the transmission path must therefore be 50 m or less. If the transmission distance is greater than 50 m, use the NT-AL001, which provides isolation, and do not include the CJ1W-CIF11 in the transmission path. When only the NT-AL001 is used, the total length of the transmission path can be a maximum of 500 m.

Note When the CPU Units are switched, communications may be momentarily interrupted, so enable communications retries in the personal computer (SCADA software, etc.) communications settings.

2-7 Power Supply Units

2-7-1 Duplex Power Supply Units

In a CS1D Duplex System, a duplex power supply can be configured by mounting a pair of CS1D Power Supply Units on the CPU Rack, an Expansion Rack, or Long-distance Expansion Rack.

With a duplex power supply, the Backplane's 5-V DC/26-V DC power supply is provided from the two CS1D Power Supply Units. Therefore the load per CS1D Power Supply Unit is approximately 50%.

If there is a breakdown at one of the CS1D Power Supply Units, operation is continued by using only the other one. In that event, the load at the one remaining CS1D Power Supply Unit will increase to 100%. (See note 1.) At the same time, A31602 (duplex power supply error) will turn ON.

Errors at Power Supply Units mounted on any Rack can be checked by means of A31900 to A31915 (for 5-V/26-V output errors) or A32000 to A32015 (for primary-side input voltage errors).

Note Even if duplex Power Supply Units are to be used, take into account the effects if an error occurs at one of the Power Supply Units and calculate the

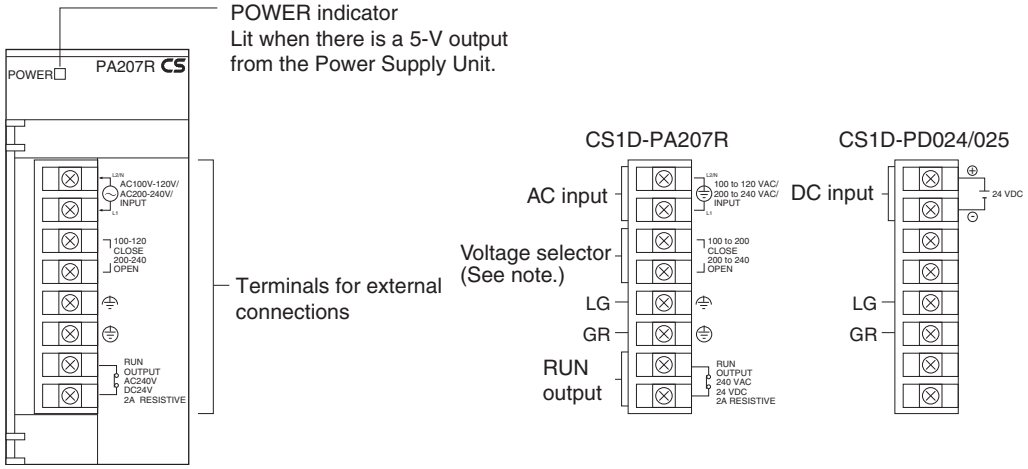
current consumption under the condition of one Power Supply Unit. If two different kinds of Power Supply Units are to be used, calculate the current consumption using the output of the smaller-capacity Power Supply Unit.

2-7-2 CS1D Power Supply Unit Models

Power supply voltage	Power supply output capacity	Power supply output terminals	RUN output	Model	Weight
100 to 120 V AC, or 200 to 240 V AC (Switched with short bar for voltage switching terminals.)	5 V DC, 7 A 26 V DC, 1.3 A Total: 35 W	No	Yes	CS1D-PA207R	1,000 g max.
24 V DC	5 V DC, 4.3 A 26 V DC, 0.56 A Total: 28 W	No	No	CS1D-PD024	550 g max.
24 V DC	5 V DC, 5.3 A 26 V DC, 1.3 A Total: 40 W	No	No	CS1D-PD025	630 g max.

Note Use the above Duplex Power Supply Units in a CS1D System. The C200HW-P□□□□ is for the CS Series and C200H, and cannot be used with the CS1D.

2-7-3 Components and Switch Settings



Note For 100 to 120 V AC: Close (short circuit)
For 200 to 240 V AC: Open
Always remove the metal jumper before applying a voltage of 200 to 240 V AC. Not doing so will damage the Unit.

AC Input

Either a power supply of 100 to 120 V AC (50/60 Hz) or 200 to 240 V AC (50/60 Hz) can be selected.

Voltage Selector

Before applying a voltage of 100 to 120 V AC, close the circuit using the metal jumper.

⚠ Caution Always remove the metal jumper before applying a voltage of 200 to 240 V AC. Otherwise, the Unit will be damaged.

LG

Ground to a resistance of 100 Ω or less to increase noise resistance and avoid electric shock.

GR Ground to a resistance of 100 Ω or less to avoid electric shock.

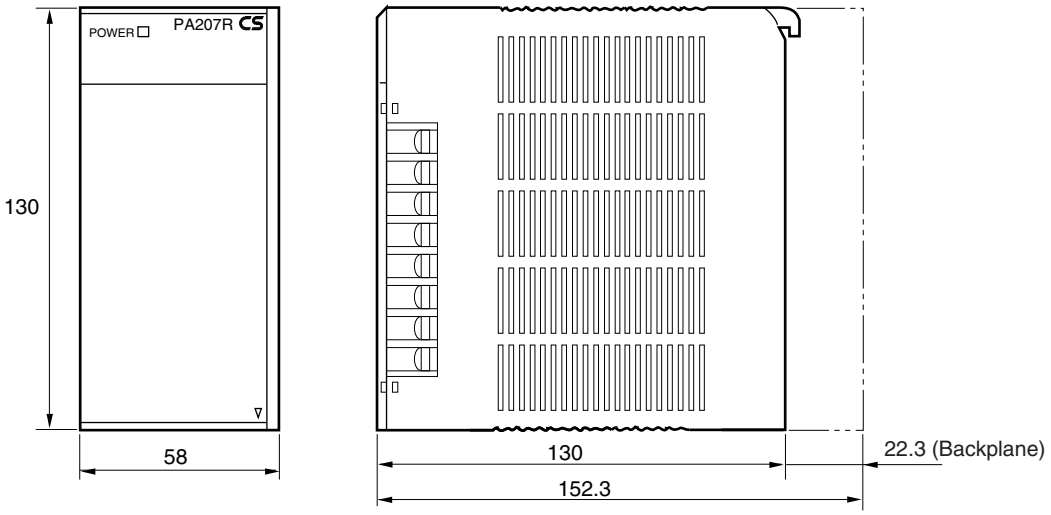
RUN Output An internal contact turns ON when the CPU Unit is operating in RUN or MONITOR mode. Any of the RUN outputs at the CPU Rack, an Expansion Rack, or a Long-distance Rack can be used. When Power Supply Units are used in duplex operation, the RUN output turns ON for both Power Supply Units together.

Contact configuration	SPST-NO
Switching capacity	240 V AC, 2 A (resistive load) 120 V AC, 0.5 A (induction load) 24 V DC, 2 A (resistive load) 24 V DC, 2 A (induction load)

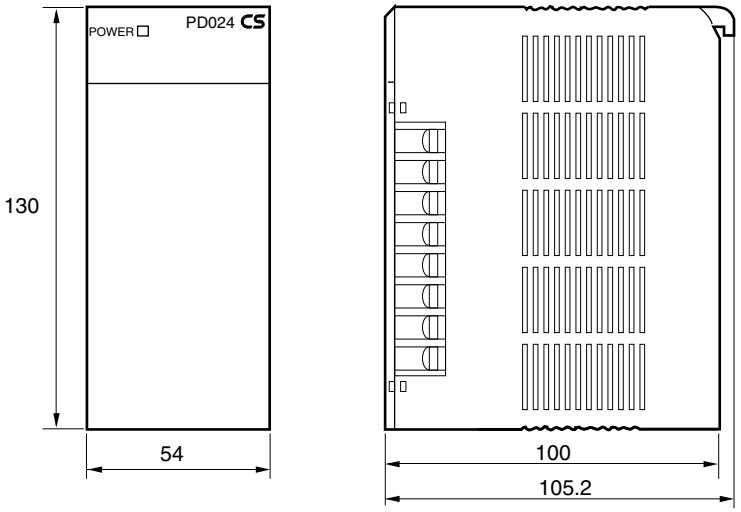
DC Input DC input power (24 V DC) is supplied.

2-7-4 Dimensions

CS1D-PA207R
CS1D-PD025



CS1D-PD024



2-8 Backplanes

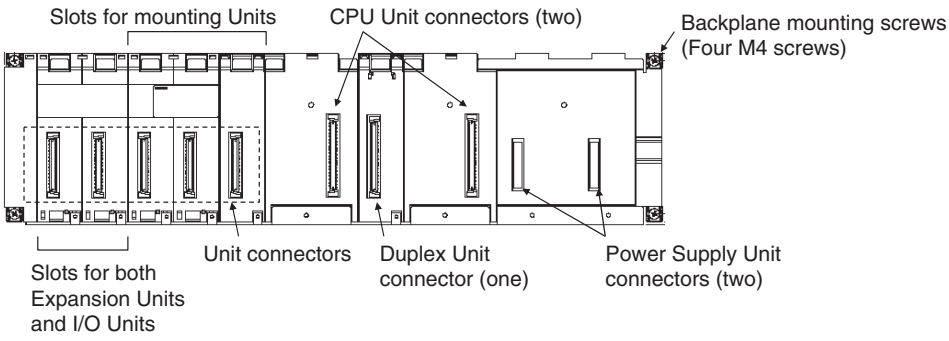
2-8-1 CPU Backplanes

Model

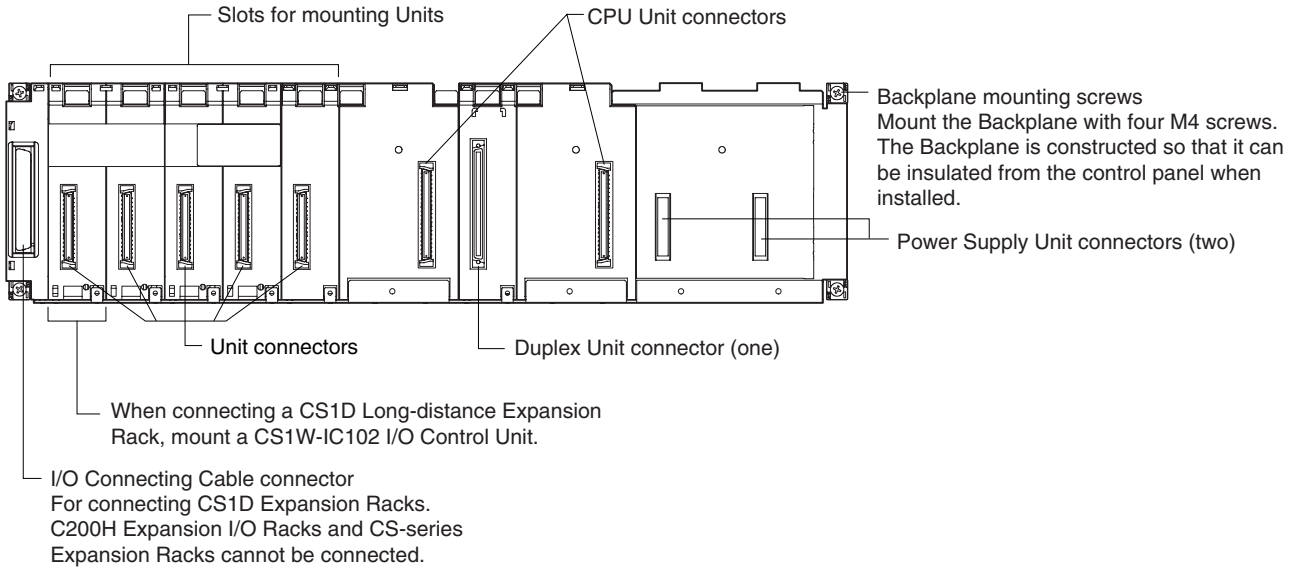
Model	Number of slots	Application	Weight
CS1D-BC042D	3 to 5	Duplex CPU, Dual I/O Expansion Systems	1,600 g max.
CS1D-BC052	5	Duplex CPU, Single I/O Expansion Systems	1,600 g max.
CS1D-BC082S	8	Single CPU Systems	1,600 g max.

Nomenclature and Functions

CPU Backplane for Duplex CPU, Dual I/O Expansion Systems: CS1D-BC042D

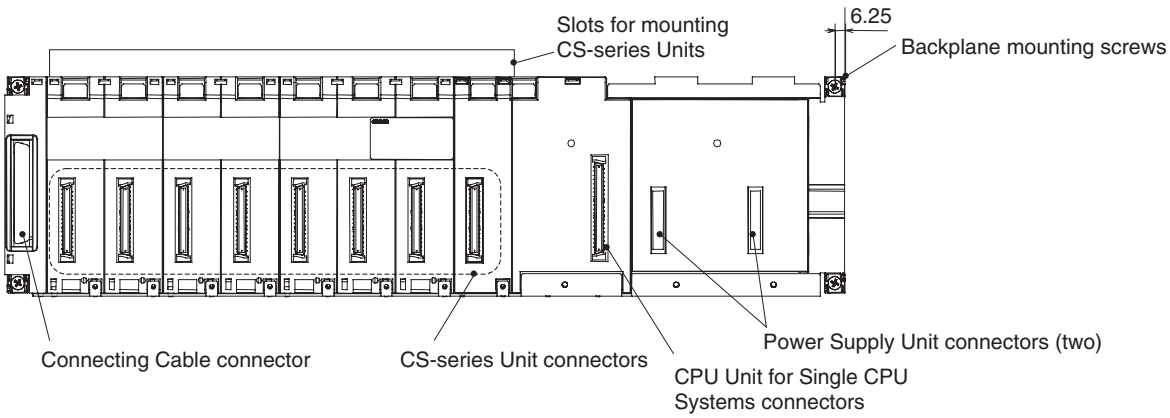


CPU Backplane for Duplex CPU, Single I/O Expansion Systems: CS1D-BC052



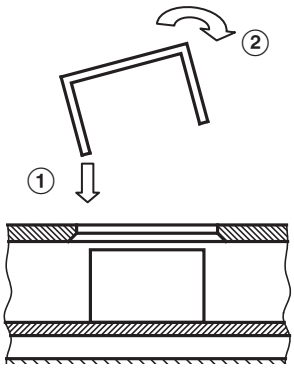
Note Backplanes produced from July 2005 have screw holes that allow an Expansion Rack Cable Mounting Bracket to be attached to secure the cable.

CPU Backplane for Single CPU Systems: CS1D-BC082S



Note To protect unused connectors, always cover them with CV500-COV01 I/O Unit Connector Covers (sold separately) or mount the CS1W-SP001 Spacer Unit (sold separately).

Covering the connector with the CV500-COV01 (sold separately) will be easier if you insert it into the side with the larger gap next to the connector first and then rotate it and insert it in the smaller gap.

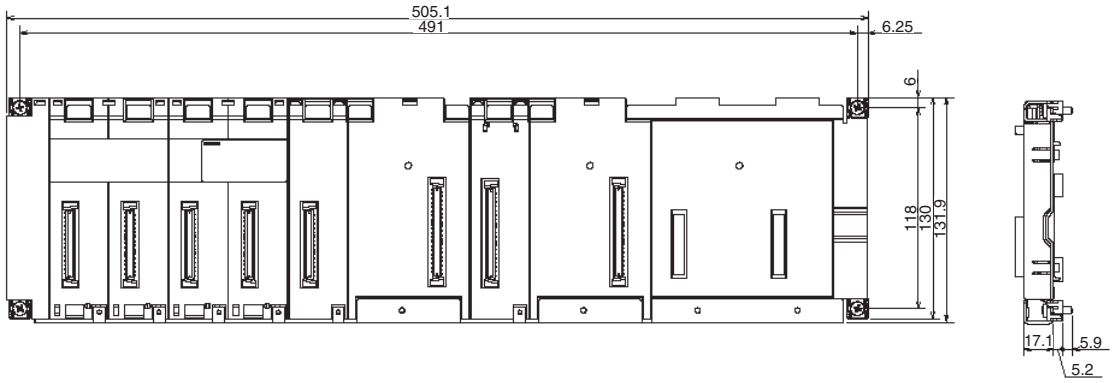


When using only one Power Supply Unit, cover the unused Power Supply Unit connector with a C500-COV01 Power Supply Unit Connector Covers (sold separately).

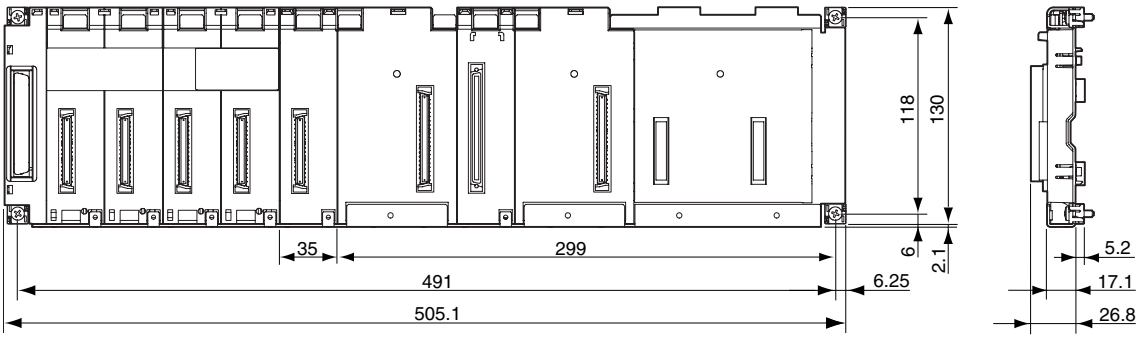
Name	Model
I/O Unit Connector Cover	CV500-COV01
I/O Unit Spacer Unit	CS1W-SP001
Power Supply Unit Connector Cover	C500-COV01
Power Supply Unit Spacer Cover (same shape as PA207R)	CS1D-SP001
Power Supply Unit Spacer Cover (same shape as PD024)	CS1D-SP002

Dimensions

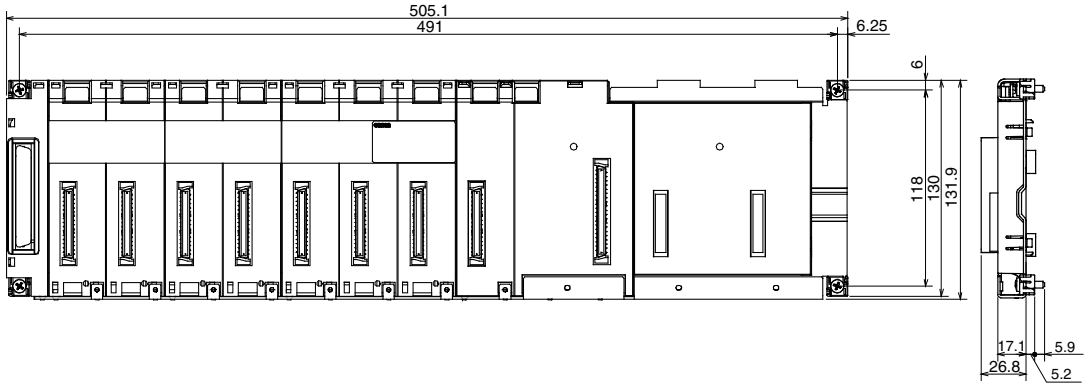
CPU Backplane for Duplex CPU, Dual I/O Expansion Systems: CS1D-BC042D



CPU Backplane for Duplex CPU, Single I/O Expansion Systems: CS1D-BC052



CPU Backplane for Single CPU Systems: CS1D-BC082S



2-8-2 Expansion Backplanes for Online Replacement

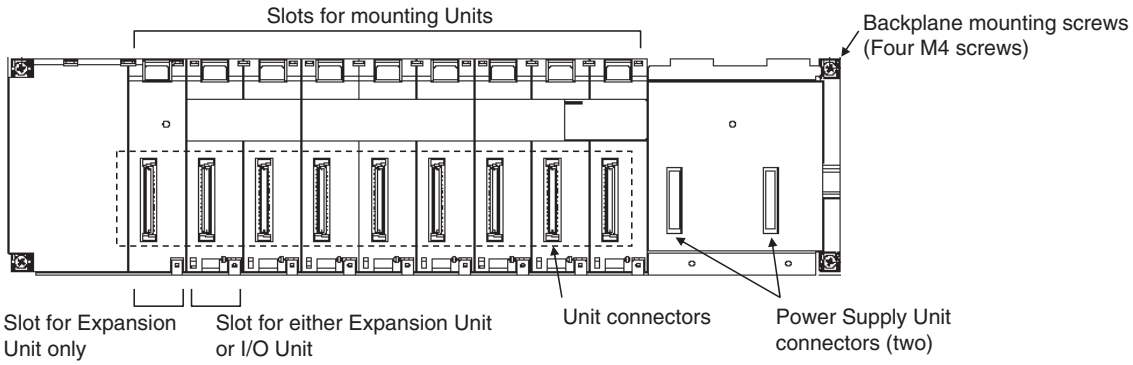
These Backplanes are used for CS1D Expansion Racks and CS1D Long-distance Expansion Racks.

Model

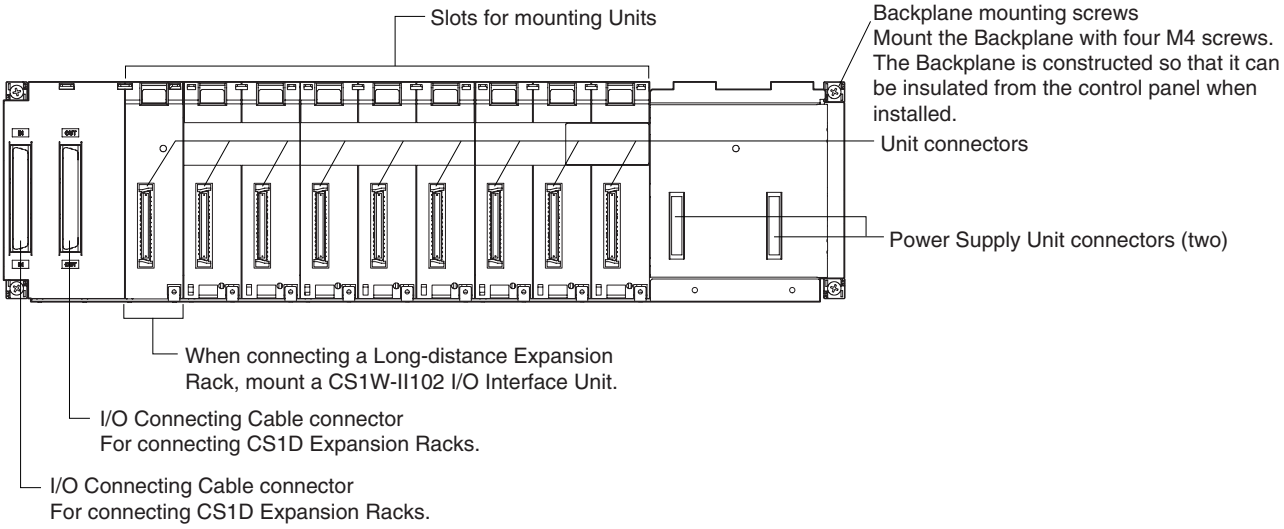
Number of slots	Model	Application	Weight
7 or 8	CS1D-BI082D	Duplex CPU, Dual I/O Expansion System	1,600 g max.
9	CS1D-BI092	Duplex CPU, Single I/O Expansion System	1,600 g max.

Nomenclature

Backplane for Duplex CPU, Dual I/O Expansion Systems: CS1D-BI082D

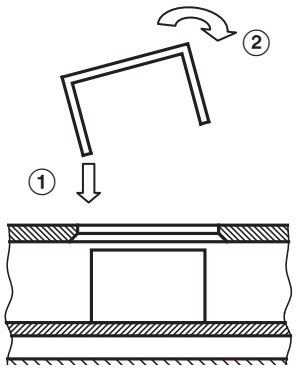


CPU Backplane for Duplex CPU, Single I/O Expansion Systems or Single CPU Systems: CS1D-BI092



Note

1. Backplanes produced from July 2005 have screw holes that allow an Expansion Rack Cable Mounting Bracket to be attached to secure the cable.
2. To protect unused connectors, always cover them with CV500-COV01 I/O Unit Connector Covers (sold separately) or mount the CS1W-SP001 Spacer Unit (sold separately).
   Covering the connector with the CV500-COV01 (sold separately) will be easier if you insert it into the side with the larger gap next to the connector first and then rotate it and insert it in the smaller gap.

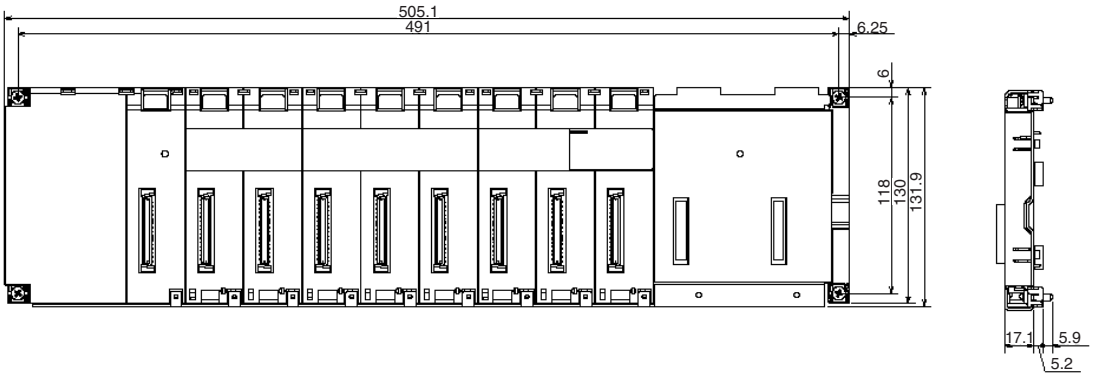


When using only one Power Supply Unit, cover the unused Power Supply Unit connector with a C500-COV01 Power Supply Unit Connector Covers (sold separately).

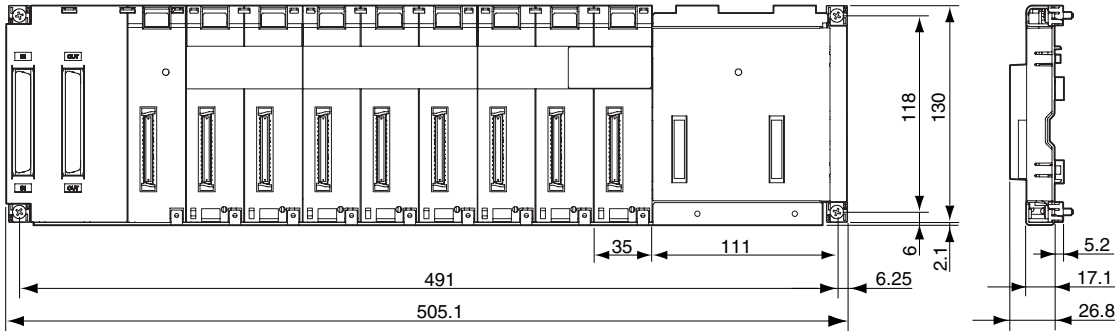
Name	Model
I/O Unit Connector Cover	CV500-COV01
I/O Unit Spacer Unit	CS1W-SP001
Power Supply Unit Connector Cover	C500-COV01
Power Supply Unit Spacer Cover (same shape as PA207R)	CS1D-SP001
Power Supply Unit Spacer Cover (same shape as PD024)	CS1D-SP002

Dimensions

Backplane for Duplex CPU, Dual I/O Expansion Systems: CS1D-BI082D



CPU Backplane for Duplex CPU, Single I/O Expansion Systems or Single CPU Systems: CS1D-BI092



2-9 Units for Duplex CPU, Dual I/O Expansion Systems

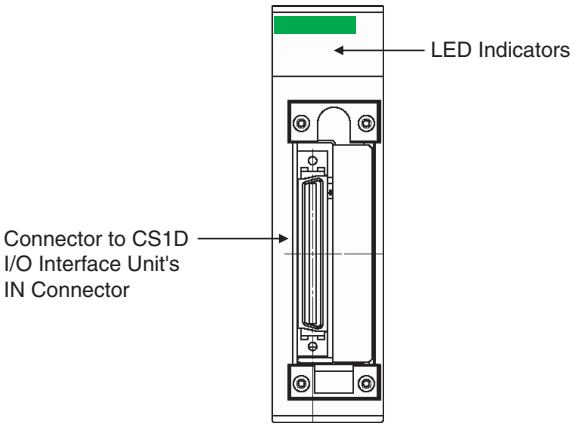
CS1D I/O Control Units and CS1D I/O Interface Units are required to construct a Duplex CPU, Dual I/O Expansion System.

2-9-1 CS1D-IC102D I/O Control Unit

Mount the CS1D-IC102D I/O Control Units in the CS1D CPU Rack.

Note The CS1D-IC102D I/O Control Unit cannot be used in a Duplex CPU Single I/O Expansion System or Single CPU System.

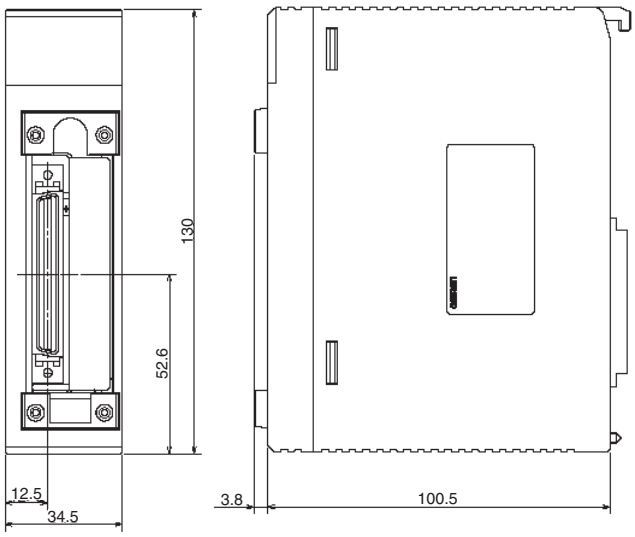
Nomenclature and Functions



LED Indicators

Indicator	Status	Meaning
RDY (Green)	ON (lit)	Operating normally.
	OFF (not lit)	• PLC error • Error in connected Expansion Rack • There is only a CPU Rack.
CABLE ERR L (Red)	ON (lit)	Error in connected Expansion Rack
	OFF (not lit)	Operating normally.
END RACK (Yellow)	ON (lit)	There is only a CPU Rack (no Expansion Rack).
	OFF (not lit)	There is an Expansion Rack.

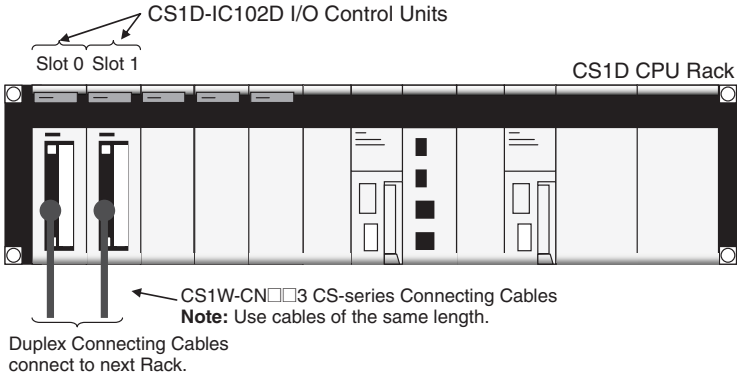
Dimensions (mm)



Connecting the Units

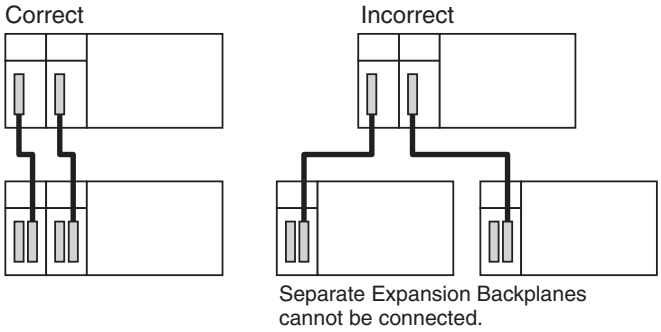
Mount the CS1D I/O Control Unit in either slot 0 or slot 1 (or mount two Units in both slots) of the CS1D-BC042D CPU Backplane.

If CS1D I/O Control Units are mounted in slot 0 and slot 1, the Connecting Cables can be duplexed.

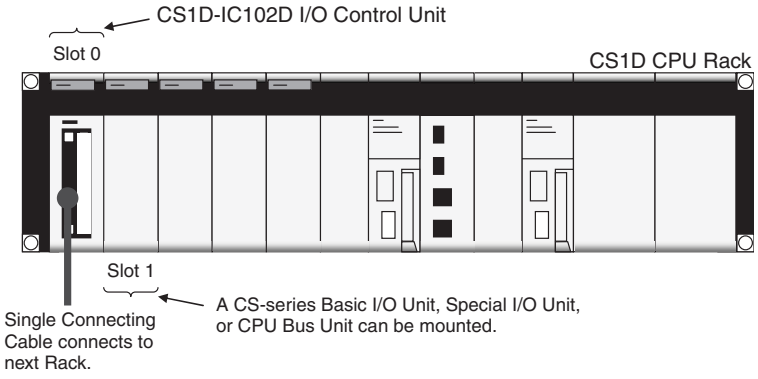


Note

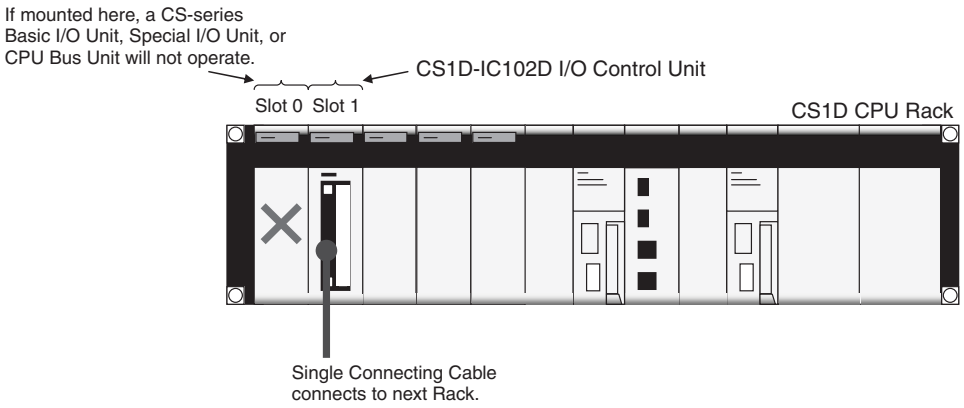
1. When using duplex Connecting Cables, always use cables that are the same length.
2. Do not connect separate Expansion Backplane systems with the two Connecting Cables. Connecting two Expansion Backplane systems will cause improper operation.



If a CS1D I/O Control Unit is mounted in slot 0 only, a Basic I/O Unit, Special I/O Unit, or CPU Bus Unit can be mounted in slot 1.



If a CS1D I/O Control Unit is mounted in slot 1 only, a Basic I/O Unit, Special I/O Unit, or CPU Bus Unit cannot used in slot 0.

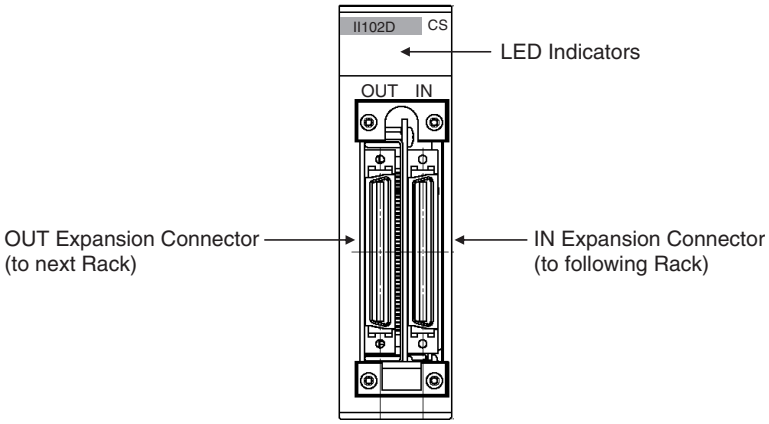


2-9-2 CS1D-II102D I/O Interface Unit

Mount the CS1D-II102D I/O Interface Units in the CS1D Expansion Racks.

Note The CS1D-II102D I/O Interface Units cannot be used in a Duplex CPU Single I/O Expansion System or Single CPU System.

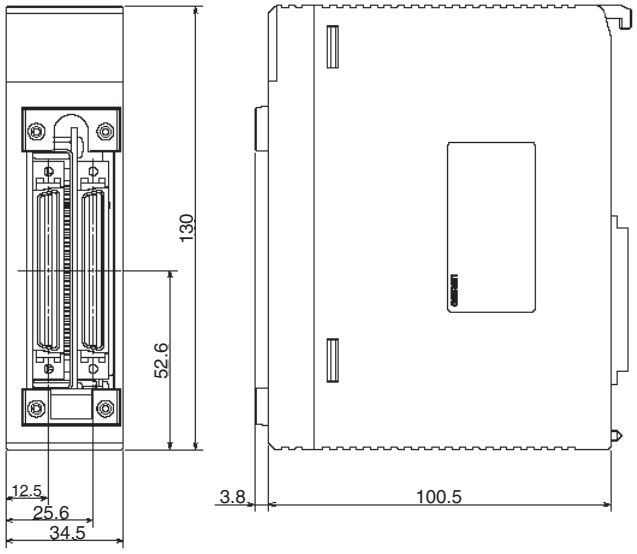
Nomenclature and Functions



LED Indicators

Indicator	Status	Meaning
RDY (Green)	ON (lit)	Operating normally.
	OFF (not lit)	• PLC error • Error in Expansion Rack connection
CABLE ERR L (Red)	ON (lit)	Error in lower (OUT) Expansion Rack connection
	OFF (not lit)	Operating normally.
CABLE ERR R (Red)	ON (lit)	Error in higher (IN) Expansion Rack connection
	OFF (not lit)	Operating normally.
END RACK (Yellow)	ON (lit)	The Rack is the last Rack. (No lower Expansion Rack is connected.)
	OFF (not lit)	There is a lower Expansion Rack connected.

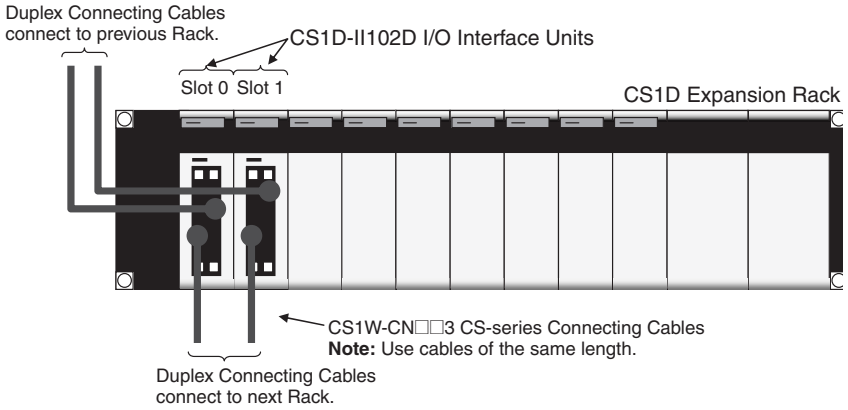
Dimensions (mm)



Connecting the Units

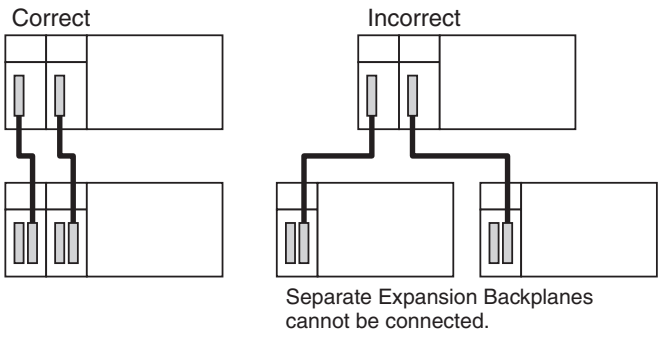
Mount the CS1D I/O Interface Unit in either slot 0 or slot 1 (or mount Units in both slots) of the CS1D-BI082D Expansion Backplane.

If CS1D I/O Interface Units are mounted in slot 0 and slot 1, the Connecting Cables can be duplexed.

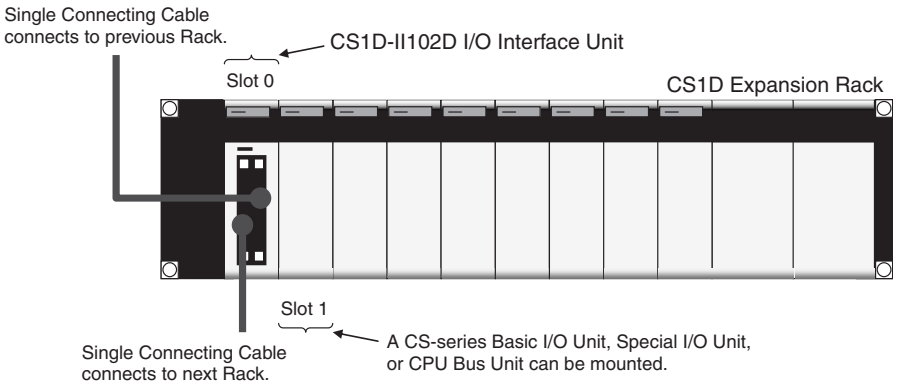


Note

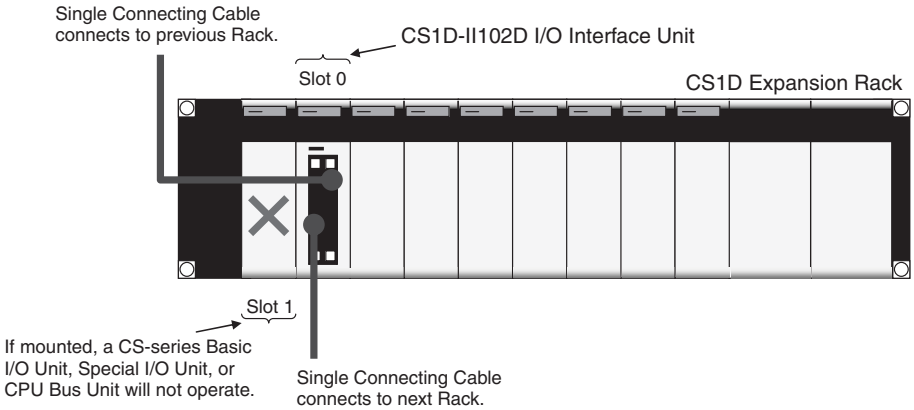
1. When using duplex Connecting Cables, always use cables that are the same length.
2. Do not connect separate Expansion Backplane systems with the two Connecting Cables. Connecting two Expansion Backplane systems will cause improper operation.



If a CS1D I/O Interface Unit is mounted in slot 0 only, a Basic I/O Unit, Special I/O Unit, or CPU Bus Unit can be used in slot 1.



If a CS1D I/O Interface Unit is mounted in slot 1 only, a Basic I/O Unit, Special I/O Unit, or CPU Bus Unit cannot be mounted in slot 0.



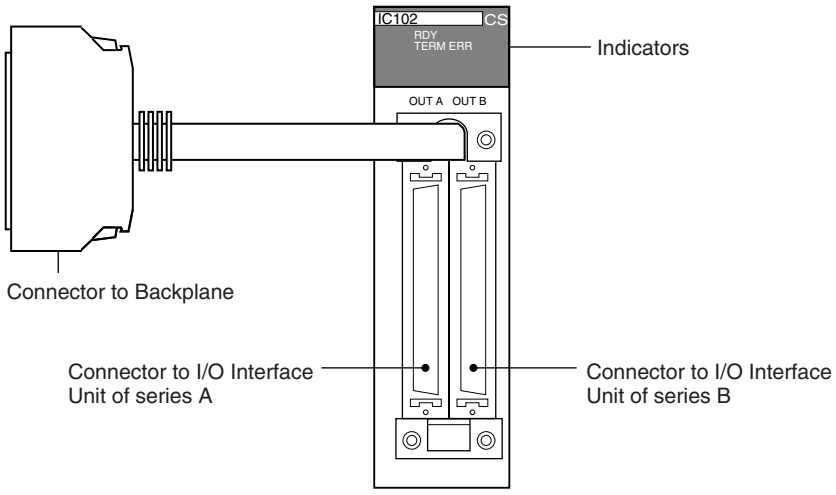
2-10 Units on CS1D Long-distance Expansion Racks

I/O Control Units and I/O Interface Units are required when creating CS1D Long-distance Expansion Racks. Terminators (CV500-TER01) are connected to the last CS1D Long-distance Expansion Rack in each series. (Up to two series of CS1D Long-distance Expansion Racks can be connected.)

2-10-1 CS1W-IC102 I/O Control Units

When connecting Expansion Racks, connect an I/O Control Unit to the left-most slot on the CPU Rack.

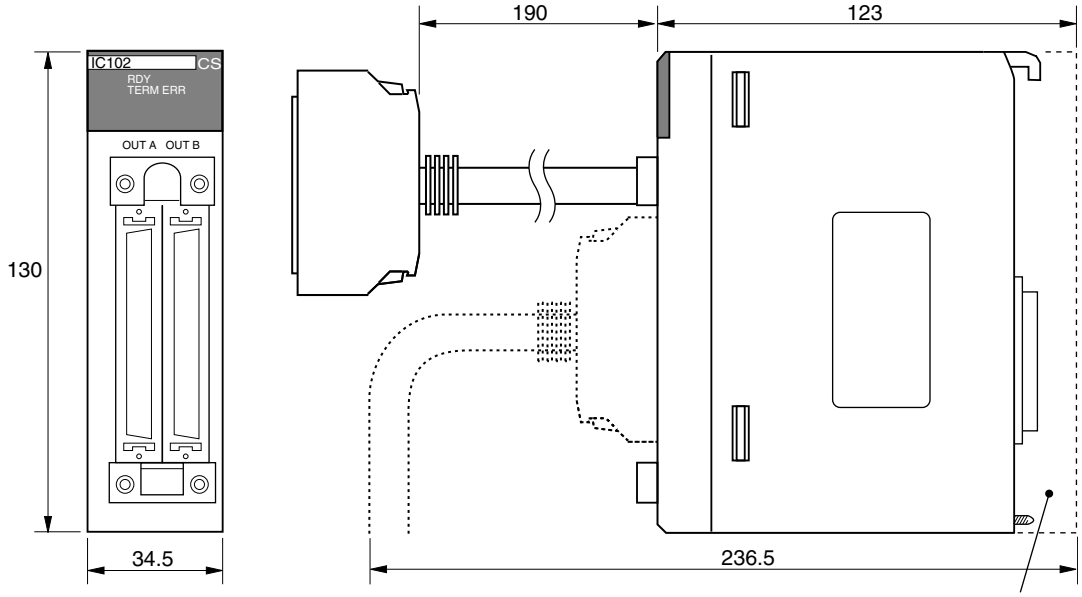
Part Names and Functions



Indicators

Indicator	Status	Meaning
RDY (green)	ON	Operating normally.
	OFF	Bus error
TERM ERR (red)	ON	Terminator missing
	OFF	Terminator connected.

Dimensions and Weight



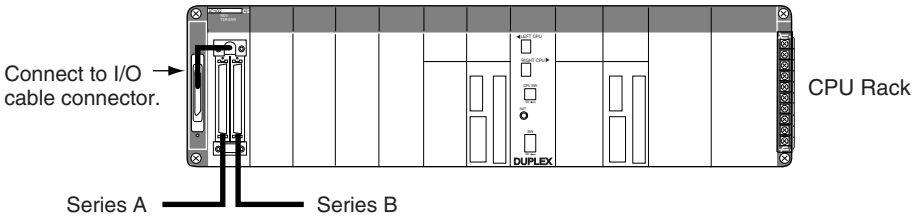
Weight: 300 g max. (including cable to Backplane)

Connection Method

Note Connect a Terminator (CV500-TER01) to the unused connector when connecting only series A or series B.

When Mounting to CPU Rack

Connect the Backplane connector to the I/O expansion connector.

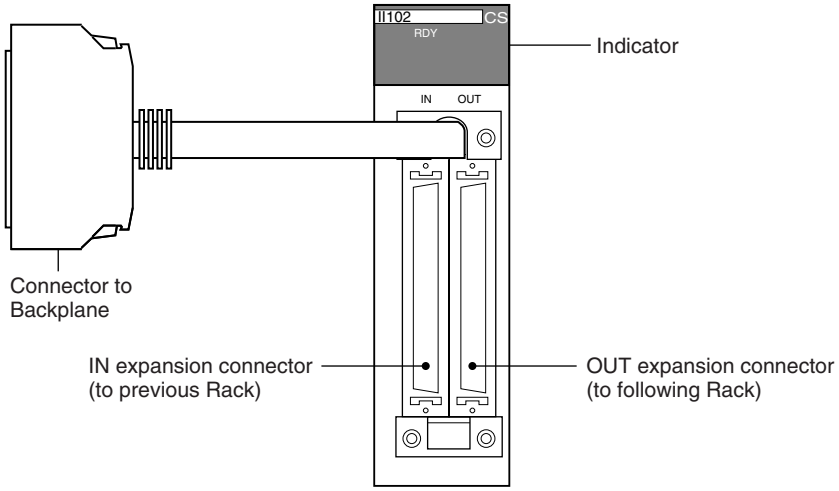


Note An I/O Control Unit cannot be mounted on an Expansion Backplane.

2-10-2 CS1W-II102 I/O Interface Units

Mount a CS1W-II102 I/O Interface Unit to the leftmost slot on each Long-distance Expansion Rack. Always use a CS1D-BI092 Expansion Backplane (for online replacement).

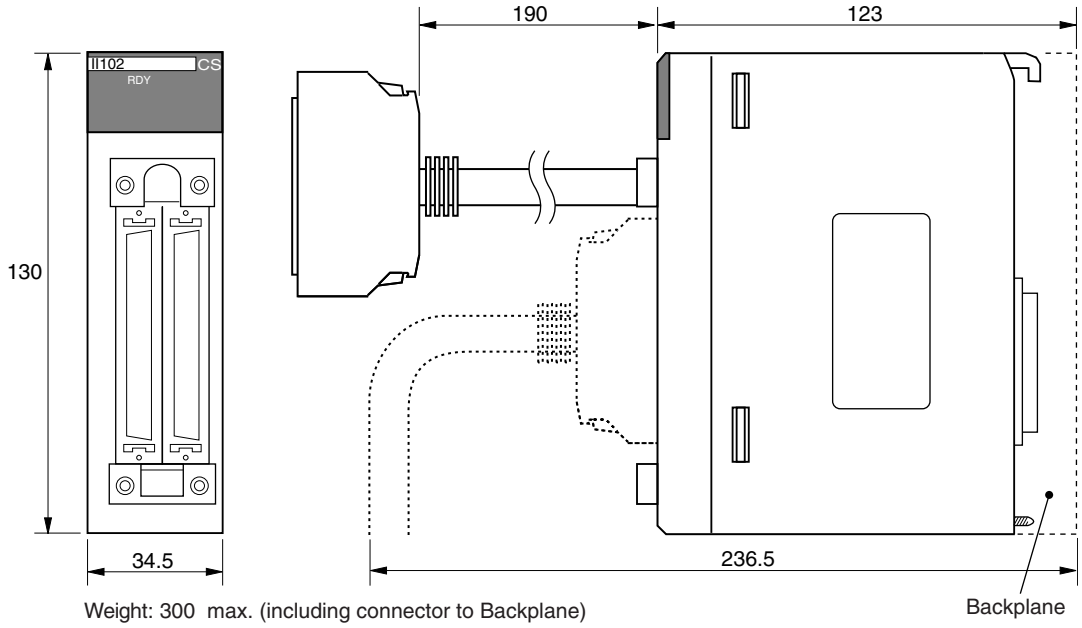
Part Names and Functions



Indicator

Indicator	Status	Meaning
RDY (green)	ON	Operating normally
	OFF	Bus error (bus reset) or system error

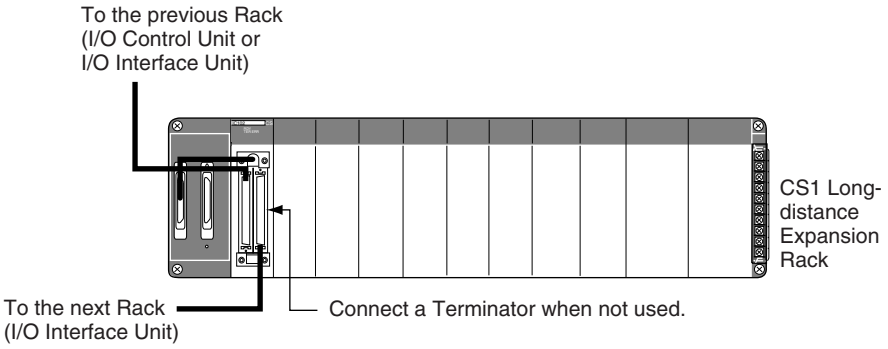
Dimensions and Weight



Weight: 300 max. (including connector to Backplane)

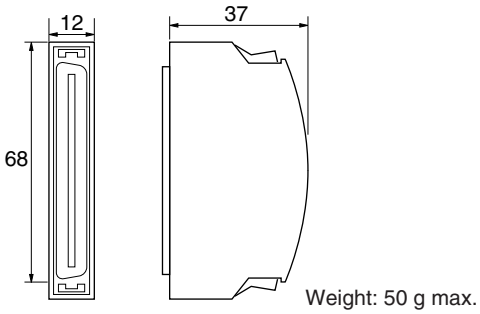
Connection Method

Connect the I/O Interface Unit to the input I/O cable connector on the Backplane (left side). Always connect a Terminator (CV500-TER01) to the connector for the next Rack when it is not used (i.e., on the last Long-distance Expansion Rack in the series).



CV500-TER01 Terminator

Two Terminators are provided with an I/O Control Unit.



Weight: 50 g max.

Long-distance Expansion Cable

Use CV-series Expansion Cable for long-distance expansion cable.

Model number	Length
CV500-CN312	0.3 m
CV500-CN612	0.6 m
CV500-CN122	1 m

Model number	Length
CV500-CN222	2 m
CV500-CN322	3 m
CV500-CN522	5 m
CV500-CN132	10 m
CV500-CN232	20 m
CV500-CN332	30 m
CV500-CN432	40 m
CV500-CN532	50 m

2-11 Basic I/O Units

2-11-1 CS-series Basic I/O Units with Terminal Blocks

Name		Specifications	Model	Page
Basic Input Units (with terminal blocks)	AC Input Units	100 to 120 V AC, 100 to 120 V DC, 16 inputs	CS1W-IA111	485
		200 to 240 V AC, 16 inputs	CS1W-IA211	485
	DC Input Units	24 V DC, 16 inputs	CS1W-ID211	486
	Interrupt Input Units	24 V DC, 16 inputs	CS1W-INT01 (See note 2.)	488
	High-speed Input Unit	24 V DC, 16 inputs	CS1W-IDP01	489
Basic Output Units (with terminal blocks)	Relay Output Units	2 A at 250 V AC/24 V DC max., 0.1 A at 120 V DC, independent contacts, 8 outputs	CS1W-OC201	495
		2 A at 250 V AC/24 V DC max., 0.1 A at 120 V DC, 16 outputs	CS1W-OC211	494
	Triac Output Units	1.2 A at 250 V AC max., 8 outputs, with fuse burnout detection circuit	CS1W-OA201	497
		0.5 A at 250 V AC max., 16 outputs	CS1W-OA211	496
	Transistor Output Units, Sinking	0.5 A at 12 to 24 V DC, 16 outputs	CS1W-OD211	498
	Transistor Output Units, Sourcing	0.5 A at 24 V DC, load short-circuit protection, 16 outputs	CS1W-OD212	503

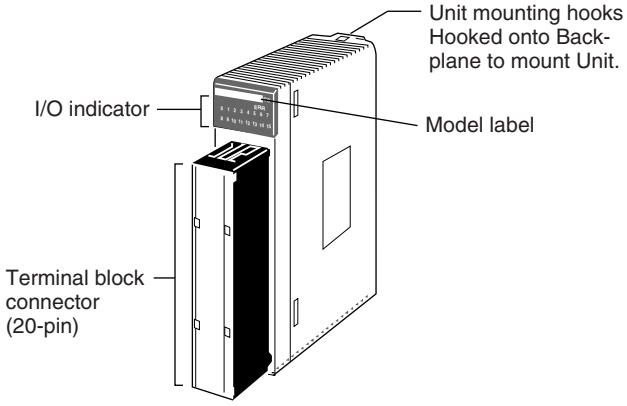
Note
1. C200H I/O Units cannot be used.
2. An Interrupt Input Unit can be used to input interrupts for a Single CPU System. With a Duplex CPU System, however, interrupt inputs cannot be used, i.e., the Interrupt Input Unit will function only as a standard Input Unit.

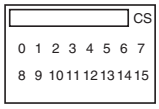
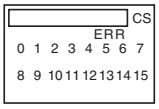
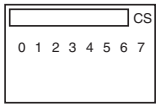
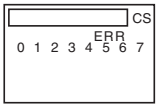
Optional Product

Name	Specifications	Model
CS-series Special I/O Unit Connector Cover	For protecting unused connectors on Backplane.	CV500-COV01

Components and Switch Settings

CS-series Basic Input Units (20-pin Terminal Block)

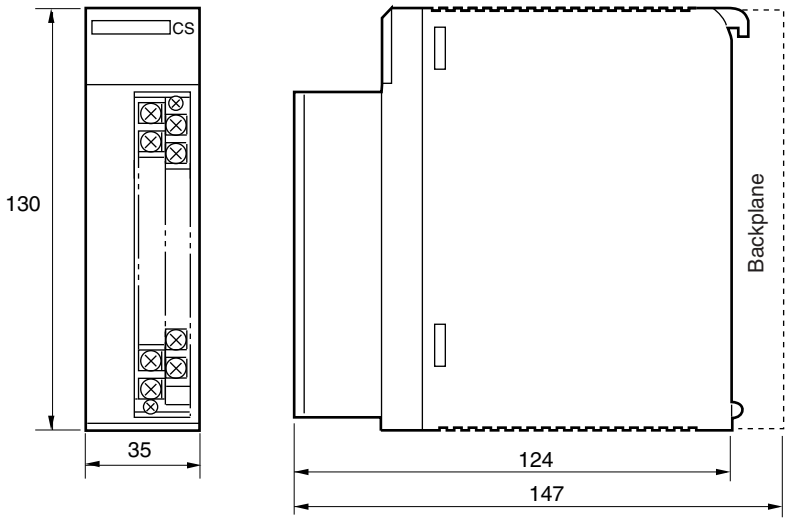


20-pin terminal block					
	16-point Unit	CS1W-ID211 CS1W-INT01 CS1W-IDP01 CS1W-OD211 CS1W-IA111 CS1W-IA211 CS1W-OC211 CS1W-OA211		16-point Units with ERR indicator (load short-circuit)	CS1W-OD212
	8-point Unit	CS1W-OC201		8-point Units with ERR indicator (fuse burnout)	CS1W-OA201

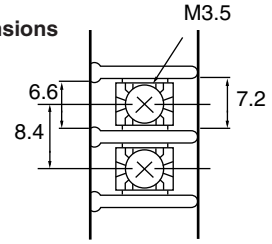
Dimensions

CS-series Basic I/O Units (20-pin Terminal Blocks)

CS1W-IA111
CS1W-IA211
CS1W-ID211
CS1W-INT01
CS1W-IDP01
CS1W-OD211
CS1W-OD212
CS1W-OA201
CS1W-OA211
CS1W-OC201
CS1W-OC211



Terminal Dimensions



2-11-2 Interrupt Input Units

An Interrupt Input Unit can be used to input interrupts for a Single CPU System. With a Duplex CPU System, however, interrupt inputs cannot be used, i.e., the Interrupt Input Unit will function only as a standard 16-point Input Unit.

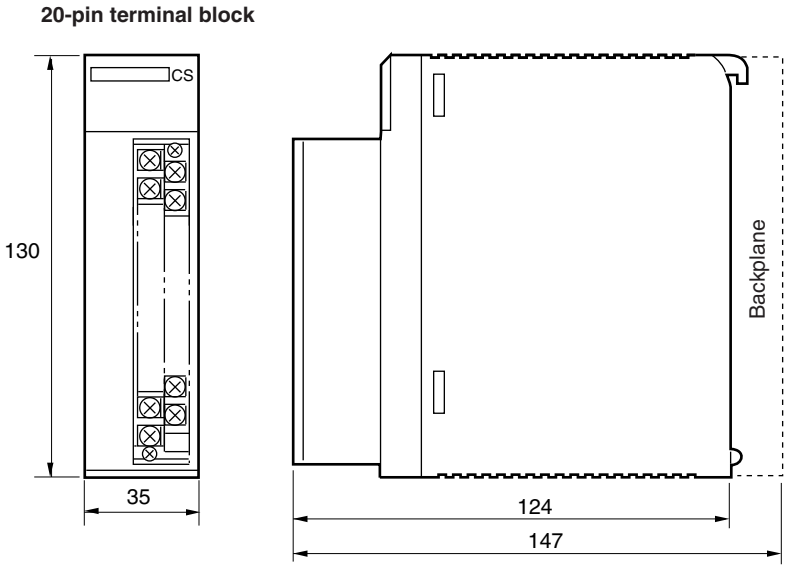
Model

Model	Specifications	No. of Units mountable to CPU Rack	Reference
CS1W-INT01	24 V DC 16 inputs	2 max.	488

C200H Interrupt Input Units cannot be used.

Dimensions

CS1W-INT01



2-11-3 High-speed Input Units

Functions

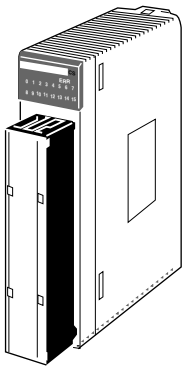
The CS1W-IDP01 High-speed Input Unit enables inputting pulse signals that are shorted than the cycle time of the CPU Unit.

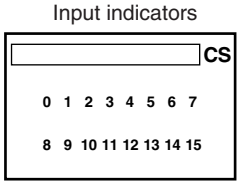
High-speed Inputs Units

Model	Name	Specifications	Reference
CS1W-IDP01	High-speed Input Unit	24 V DC, 16 inputs	489

C200H Input Units cannot be used.

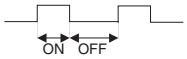
Components





Input Signal Width

High-speed input signals must meet the following conditions for the ON time.



Model	ON time
CS1W-IDP01	0.1 ms min.

Dimensions

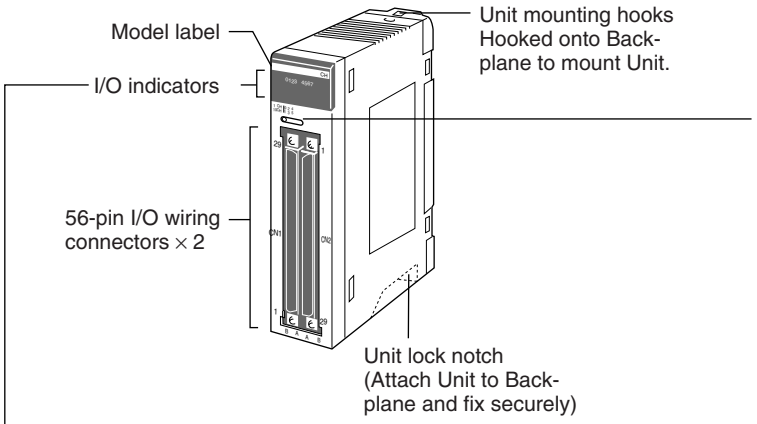
The High-speed Input Unit has the same dimensions as the Units with a 20-terminal block.

2-11-4 CS-series Basic I/O Units with Connectors (32-, 64-, and 96-pt Units)

CS-series Basic I/O Units are classified as Basic I/O Units.

Name	Specifications	Model	Page
DC Input Unit	24 V DC, 32 inputs	CS1W-ID231	490
	24 V DC, 64 inputs	CS1W-ID261	491
	24 V DC, 96 inputs	CS1W-ID291	492
Transistor Output Unit, Sinking	0.5 A at 12 to 24 V DC, 32 outputs	CS1W-OD231	499
	0.3 A at 12 to 24 V DC, 64 outputs	CS1W-OD261	500
	0.1 A at 12 to 24 V DC, with fuse burnout detection circuit, 96 outputs	CS1W-OD291	501
Transistor Output Unit, Sourcing	0.5 A at 24 V DC, load short-circuit protection, 32 outputs	CS1W-OD232	504
	0.3 A at 24 V DC, load short-circuit protection, 64 outputs	CS1W-OD262	506
	0.1 A at 24 V DC, with fuse burnout detection circuit, 96 outputs	CS1W-OD292	507
DC Input/Transistor Output Unit, Sinking	24 V DC input, 0.3 A output at 12 to 24 V DC, 32 inputs/32 outputs	CS1W-MD261	509
	24 V DC input, 0.1 A output at 12 to 24 V DC, with fuse burnout detection circuit, 48 inputs/48 outputs	CS1W-MD291	511
DC Input/Transistor Output Unit, Sourcing	24 V DC input, 0.3 A output at 24 V DC, load short-circuit protection, 32 inputs/32 outputs	CS1W-MD262	513
	24 V DC input, 0.1 A output at 24 V DC, with fuse burnout detection circuit, 48 inputs/48 outputs	CS1W-MD292	515
TTL I/O Unit	3.5 mA input at 5 V DC, 35 mA output at 5 V DC, 32 inputs/32 outputs	CS1W-MD561	517

Note Immediate refreshing is possible for the CS-series Basic I/O Units (with 32-, 64-, and 96-point connectors) using the IORF instruction.



I CH II CH
0 1
2 3
DISPLAY

	Display switch	
	0, 1	2, 3
Area 1	m	m+2
Area 2	m+1	m+3

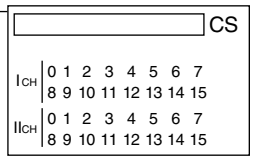
Display Switch for 96-point I/O Units

I CH | 0 2 4
II CH | 1 3 5
DISPLAY

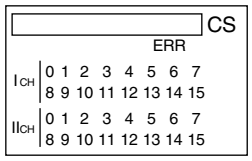
Display switch (3-level selection)

	Display switch		
	0, 1	2, 3	4, 5
Area 1	m	m+2	m+4
Area 2	m+1	m+3	m+5

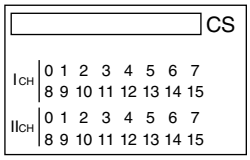
32-point Units
CS1W-ID231
CS1W-OD231



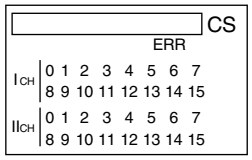
32-point Units with ERR indicator (load short-circuit indicator)
CS1W-OD232



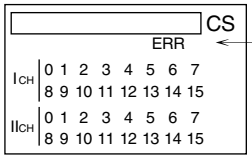
64-point Units
CS1W-ID261
CS1W-OD261
CS1W-MD261



64-point Units with ERR indicator (load short-circuit indicator)
CS1W-OD262
CS1W-MD262



96-point Units
CS1W-ID291/OD291/OD292/MD291/MD292



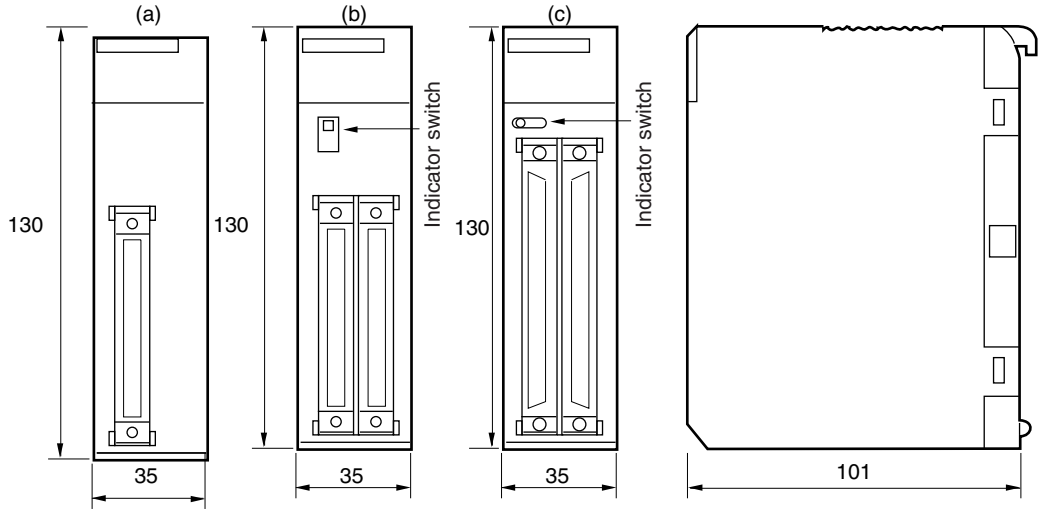
F (fuse burnt out) indicator
Available on Output Units.
Lights when one or more fuses in the Unit blows.
Lights when external power is OFF.

Dimensions

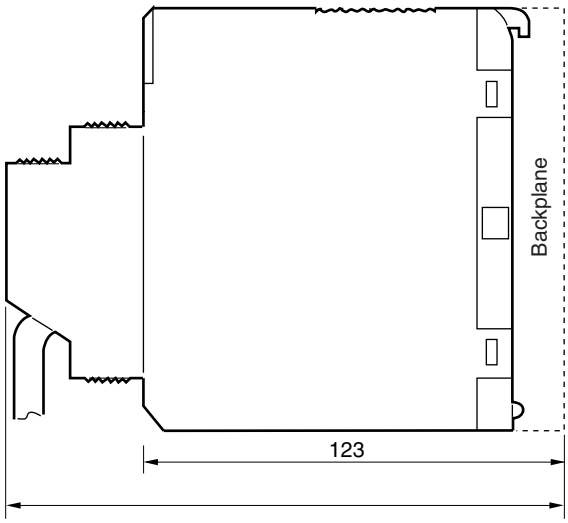
Units with One 40-pin connector (a)
CS1W-ID231
CS1W-OD231
CS1W-OD232

Units with Two 40-pin connectors (b)
CS1W-ID261
CS1W-OD261
CS1W-OD262
CS1W-MD261
CS1W-MD262

Units with 56-pin connectors (c)
CS1W-ID291
CS1W-OD291
CS1W-OD292
CS1W-MD291
CS1W-MD292

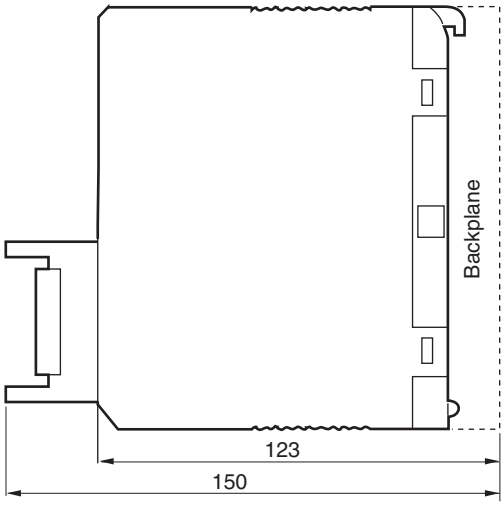


Using Soldered or Crimped Connector



Approx. 169 for 32- and 64-pt Units/Approx. 179 for 96-pt Units

Using Pressure-welded Connector Connecting Cables:
XW2Z-R□□□C-□□□-□□□
XW2Z-□□□



2-12 Unit Current Consumption

There are fixed amounts of current and power that can be provided to the Units on the Rack. Even when using only one Power Supply Unit, design the system so that the total current consumption of Units on the Rack does not exceed the values for the maximum Power Supply Unit current and the maximum total power.

Calculate the total current consumption under normal conditions (i.e., with one Power Supply Unit mounted), taking into account the load when an error occurs at one of the Power Supply Units. If two different kinds of Power Supply Units are to be used, calculate the current consumption using the output of the smaller-capacity Power Supply Unit.

Note When duplex Power Supply Units are used, the load for each CS1D Power Supply Unit is reduced by approximately half.

2-12-1 CPU Rack and Expansion Racks

The maximum current and power provided for the CPU Rack and Expansion Racks is shown below.

Note
1. CPU Rack: When making calculations, include the current and power consumption for a CPU Backplane for Duplex CPU System, a Duplex Unit, and two CS1D Power Supply Units.
2. When making calculations, include the current and power consumption for an Online Replacement Expansion Backplane.

Power Supply Unit model	Maximum current provided			Maximum total power provided
	5-V (internal logic power supply)	26-V (relay power supply)	24-V (service power supply)	
CS1D-PA207R	7 A	1.3 A	None	35 W
CS1D-PD024	4.3 A	0.56 A	None	28 W
CS1D-PD025	5.3 A	1.3 A	None	40 W

Note

1. When duplexing by combining the CS1D-PA207R and CS1D-PD024, design the total current consumption for all Units on the Rack to be within the power supply capacity of the CS1D-PD024.
2. When duplexing by combining the CS1D-PA207R and CS1D-PD025, design the total current consumption for all Units on the Rack to be within the power supply capacity for the CS1D-PA207R.
3. When duplexing by combining the CS1D-PD025 and CS1D-PD024, design the total current consumption for all Units on the Rack to be within the power supply capacity for the CS1D-PD024.

2-12-2 Total Current and Power Consumption Calculation Example

Example 1: Mounting the Following Units on a CPU Rack with a CS1D-PA207R Power Supply Unit

Item	Model	Quantity	Voltage group	
			5-V	26-V
CPU Backplane for Duplex CPU System (5 slots)	CS1D-BC052	1	0.55 A	---
Duplex Unit	CS1D-DPL01	1		
CPU Unit	CS1D-CPU67H	2	0.82 A	---
Input Unit	CS1W-ID291	1	0.20 A	---
Output Unit	CS1W-OC221	1	0.13 A	0.096 A
Special I/O Unit	CS1W-MAD44	2	0.20 A	0.20 A
CPU Bus Unit	CS1W-CLK21-V1	1	0.33 A	---
Service power supply	---		---	---
Current consumption	Calculation		0.55 + 0.82 × 2 + 0.20 + 0.13 + 0.20 × 2 + 0.33	0.096 + 0.20 × 2
	Result		3.25 A (≤7 A)	0.496 A (≤1.3 A)
Power consumption	Calculation		3.25 A × 5 V = 16.3 W	0.496 A × 26 V = 12.9 W
	Result		16.3 + 12.9 = 29.2 W (≤35 W)	

Example 1: Mounting the Following Units on an Expansion Rack with a CS1D-PA207R Power Supply Unit

Item	Model	Quantity	Voltage group	
			5-V	26-V
Online Replacement Expansion Backplane	CS1D-BI092	1	0.28 A	---
Input Unit	CS1W-ID291	2	0.20 A	---
Output Unit	CS1W-OD291	7	0.48 A	---
Current consumption	Calculation		0.28 A + 0.20 A × 2 + 0.48 A × 7	---
	Result		4.04 A (≤7 A)	---
Power consumption	Calculation		4.04 A × 5 V = 20.2 W	---
	Result		20 2 W (≤35 W)	

2-12-3 Current Consumption Tables

Note For the current consumption of Units not shown in these tables, refer to the individual user manuals for those Units.

5-V Voltage Group

Name	Model	Current consumption (A)
CPU Backplane for Single CPU Systems	CS1D-BC082S	0.17
CPU Backplane for Duplex CPU, Dual I/O Expansion Systems	CS1D-BC042D	1.2
Duplex Unit for Duplex CPU, Dual I/O Expansion Systems	CS1D-DPL02D	0.41
CPU Backplane for Duplex CPU, Single Expansion I/O Systems	CS1D-BC052	0.55 (total for Backplane and Duplex Unit)
Duplex Unit for Duplex CPU, Single Expansion I/O Systems	CS1D-DPL01	
CS1D CPU Units **Note** The values shown on the right include the current consumption of a Programming Console.	CS1D-CPU67HA	0.82 (See note 1.)
	CS1D-CPU68HA	0.82 (See note 1.)
	CS1D-CPU65H	0.82 (See note 1.)
	CS1D-CPU67H	0.82 (See note 1.)
	CS1D-CPU44SA	0.82 (See note 1.)
	CS1D-CPU67SA	0.82 (See note 1.)
	CS1D-CPU42S	0.78 (See note 1.)
	CS1D-CPU44S	0.78 (See note 1.)
	CS1D-CPU65S	0.82 (See note 1.)
	CS1D-CPU67S	0.82 (See note 1.)
Serial Communications Boards (See note 2.)	CS1W-SCB21-V1	0.28 (See note 1.)
	CS1W-SCB41-V1	0.36 (See note 1.)
Loop Control Boards (See note 2.)	CS1W-LCB01	0.22 (See note 3.)
	CS1W-LCB05	0.22 (See note 3.)
Online Replacement Expansion Backplane for Duplex CPU, Dual I/O Expansion Systems	CS1D-BC082D	1.21
Online Replacement Expansion Backplane for Duplex CPU, Single Expansion I/O Systems or Single CPU Systems	CS1D-BI092	0.28
CS1D I/O Control Unit	CS1W-IC102D	0.2
CS1D I/O Interface Unit	CS1W-II102D	0.22
I/O Control Unit	CS1W-IC102	0.92
I/O Interface Unit	CS1W-II102	0.23

Note

1. NT-AL001 Link Adapters consume an additional 0.15 A each when used.
   Add 0.04 A for each CJ1W-CIF11 RS-422A Adapter that is used.
   Add 0.20 A for each NV3W-M□20L Programmable Terminal that is used.
2. Only one CS1 Inner Board can be mounted to the Inner Board mounting section in the CPU Unit of a single-CPU system.
3. With the NT-AL001 connected: Add 0.15 A per Board.

Basic I/O Units

Name	Model	Current consumption (A)
DC Input Units	CS1W-ID211	0.10
	CS1W-ID231	0.15
	CS1W-ID261	0.15
	CS1W-ID291	0.20
AC Input Unit	CS1W-IA111	0.11
	CS1W-IA211	0.11
B7A Input Unit	CS1W-B7A12	0.09
Interrupt Input Unit	CS1W-INT01	0.10
High-speed Input Unit	CS1W-IDP01	0.10
Relay Output Unit	CS1W-OC201	0.10
	CS1W-OC211	0.13
Transistor Output Unit	CS1W-OD211	0.17
	CS1W-OD212	0.17
	CS1W-OD231	0.27
	CS1W-OD232	0.27
	CS1W-OD261	0.39
	CS1W-OD262	0.39
	CS1W-OD291	0.48
	CS1W-OD292	0.48
Triac Output Unit	CS1W-OA201	0.23
	CS1W-OA211	0.41
B7A Output Unit	CS1W-B7A02	0.09
DC Input/Transistor Output Unit	CS1W-MD261	0.27
	CS1W-MD262	0.27
	CS1W-MD291	0.35
	CS1W-MD292	0.35
TTL I/O Unit	CS1W-MD561	0.27
B7A I/O Units	CS1W-B7A21	0.09
	CS1W-B7A22	0.09

CS-series Special I/O Units

Name	Model	Current consumption (A)
Analog I/O Unit	CS1W-MAD44	0.20
Analog Input Unit	CS1W-AD041-V1/081-V1	0.12
	CS1W-AD161	0.15
Analog Output Unit	CS1W-DA041/08V/08C	0.13
Isolated Thermocouple Input Unit	CS1W-PTS01-V1	0.15
	CS1W-PTS11	0.12
	CS1W-PTS51	0.25
	CS1W-PTS55	0.18
Isolated Resistance Thermometer Input Unit	CS1W-PTS02	0.15
	CS1W-PTS03	0.15
	CS1W-PTS12	0.12
	CS1W-PTS52	0.25
	CS1W-PTS56	0.18
Isolated 2-wire Transmission Device Input Unit	CS1W-PTW01	0.15

Name	Model	Current consumption (A)
Isolated DC Input Unit	CS1W-PDC01	0.15
	CS1W-PDC11	0.12
	CS1W-PDC55	0.18
Isolated Control Output Unit (Analog Output Unit)	CS1W-PMV01	0.15
	CS1W-PMV02	0.12
Power Transducer Input Unit	CS1W-PTR01	0.15
DC Input Unit (100 mV)	CS1W-PTR02	0.15
Isolated Pulse Input Unit	CS1W-PPS01	0.20
Motion Control Units	CS1W-MC221-V1	0.6 (0.80 when connected to a Teaching Box)
	CS1W-MC421-V1	0.7 (1.00 when connected to a Teaching Box)
Position Control Units	CS1W-NC113	0.25
	CS1W-NC133	0.25
	CS1W-NC213	0.25
	CS1W-NC233	0.25
	CS1W-NC413	0.36
	CS1W-NC433	0.36
Customizable Counter Units	CS1W-HIO01-V1	0.60
	CS1W-HCP22-V1	0.80
	CS1W-HCA12-V1	0.75
	CS1W-HCA22-V1	0.75
High-speed Counter Units	CS1W-CT021	0.36
	CS1W-CT041	0.45
GPIB Interface Unit	CS1W-GPI01	0.33
CompoNet Master Unit	CS1W-CRM21	0.40
CompoBus/S Master Unit	CS1W-SRM21	0.15
ID Sensor Units	CS1W-V600C11/V680C11	0.26
	CS1W-V600C12/V680C12	0.32

CS-series CPU Bus Units

Name	Model	Current consumption (A)
Controller Link Unit	CS1W-CLK21-V1	0.33
	CS1W-CLK23	0.33
	CS1W-CLK12-V1	0.52
	CS1W-CLK13	0.52
	CS1W-CLK52-V1	0.65
	CS1W-CLK53	0.65
Serial Communications Units	CS1W-SCU21-V1	0.30 (See note.)
	CS1W-SCU31-V1	0.40
SYSMAC LINK Unit	CS1W-SLK21	0.48
	CS1W-SLK11	0.47
Ethernet Unit	CS1D-ETN21D	0.38
	CS1W-ETN21	0.38
EtherNet/IP Unit	CS1W-EIP21	0.41
FL-net Unit	CS1W-FLN22	0.38
DeviceNet Unit	CS1W-DRM21-V1	0.29

Name	Model	Current consumption (A)
MECHATROLINK-II Position Control Units	CS1W-NC271	0.36
	CS1W-NC471	0.36
	CS1W-NCF71	0.36
SYSMAC SPU Units (High-speed Data Storage Units)	CS1W-SPU01-V2	0.56
	CS1W-SPU02-V2	0.70

Note NT-AL001 Link Adapters consume an additional 0.15 A each when used.
Add 0.04 A for each CJ1W-CIF11 RS-422A Adapter that is used.
Add 0.20 A for each NV3W-M□20L Programmable Terminal that is used.

26-V Voltage Group

Name	Model	Current consumption (A)
Relay Output Units	CS1W-OC201	0.006 per ON output point
	CS1W-OC211	0.006 per ON output point
Analog I/O Unit	CS1W-MAD44	0.20
Analog Input Unit	CS1W-AD04-V11/081-V1	0.09
	CS1W-AD161	0.06
Analog Output Unit	CS1W-DA041/08V	0.18
	CS1W-DA08C	0.25
Isolated Thermocouple Input Unit	CS1W-PTS01-V1	0.15
	CS1W-PTS11	0.08
	CS1W-PTS55	0.06
Isolated Resistance Thermometer Input Unit	CS1W-PTS02	0.15
	CS1W-PTS03	0.15
	CS1W-PTS12	0.07
	CS1W-PTS56	0.06
Isolated 2-wire Transmission Device Input Unit	CS1W-PTW01	0.16
Isolated DC Input Unit	CS1W-PDC01	0.16
	CS1W-PDC11	0.12
	CS1W-PDC55	0.06
Isolated Control Output Unit (Analog Output Unit)	CS1W-PMV01	0.16
	CS1W-PMV02	0.12
Power Transducer Input Unit	CS1W-PTR01	0.08
DC Input Unit (100 mV)	CS1W-PTR02	0.08
Isolated Pulse Input Unit	CS1W-PPS01	0.16
Customizable Counter Unit	CS1W-HCA12-V1	0.15
	CS1W-HCA22-V1	0.15
ID Sensor Units	CS1W-V600C11	0.12
	CS1W-V680C11	0.13 (See note.)

Note With the V680-H01 connected: The value is 0.28 A. For details, refer to the product catalog (V680-series RFID System, Cat. No. Q151).

2-13 CPU Bus Unit Setting Area Capacity

Settings for most CPU Bus Units and Inner Boards are stored in the CPU Bus Unit Setting Area in the CPU Unit. Refer to *8-22 Parameter Areas* for details. The CPU Bus Units are allocated the required number of words for settings from this area.

There is a limit to the capacity of the CPU Bus Unit Setting Area of 10,752 bytes (10 Kbytes). The system must be designed so that the number of words used in the CPU Bus Unit Setting Area by all of the CPU Bus Units and the Inner Board does not exceed this capacity. If the wrong combination of Units is used, the capacity will be exceeded and either Units will operate from default settings only or will not operate at all.

The following table shows the number of bytes required in the CPU Bus Unit Setting Area by each Unit and the Inner Board. Any Unit or Inner Board with a usage of "0" does not use the CPU Bus Unit Setting Area at all.

2-13-1 Memory Required for Units and Inner Boards

Classification	Name	Model number	Memory required (bytes)
CS-series CPU Bus Units	Controller Link Unit	CS1W-CLK21/12/52-V1 CS1W-CLK13/53 CS1W-CLK11	512
	SYSMAC LINK Unit	CS1W-SLK21/11	512
	Serial Communications Unit	CS1W-SCU21	0
	Ethernet Unit	CS1W-ETN21	994
	Duplex Ethernet Unit (See note 2.)	CS1D-ETN21D	384
	DeviceNet Unit	CS1W-DRM21-V1	0
Inner Boards	Loop Control Board built into Process-control CPU Unit (See note 3.)	CS1D-LCB05D	0
	Loop Control Board (See note 4.)	CS1W-LCB01/02	0
	Serial Communications Board (See note 4.)	CS1W-SCB21-V1/41-V1	0

Note

1. Units that are allocated no bytes do not use the CPU Bus Unit Setting Area at all.
2. When duplex Ethernet communications are used, twice the listed memory will be required (i.e., memory will be required for two Units). With Duplex Controller Link communications (CS1W-CLK12/52-V1, CS1W-CLK13/53), memory is required only for one Unit even though two Controller Link Units are mounted.
3. Only for Process-control CPU Units.
4. Only for Single CPU Systems.

2-14 I/O Table Settings

The following settings are used in the I/O tables on the CX-Programmer.

Note Refer to the CX-Programmer manual for Units not listed in the table.

2-14-1 Basic I/O Units

Name	Model	Unit type
AC Input Unit	CS1W-IA111	16-point Input Unit
	CS1W-IA211	16-point Input Unit
DC Input Unit	CS1W-ID211	16-point Input Unit
	CS1W-ID231	32-point Input Unit
	CS1W-ID261	64-point Input Unit
	CS1W-ID291	96-point Input Unit
TTL I/O Unit	CS1W-MD561	64-point I/O Unit
Interrupt Input Unit	CS1W-INT01	16-point Interrupt Input Unit
High-speed Input Unit	CS1W-IDP01	16-point Input Unit
Contact Output Unit	CS1W-OC201	16-point Output Unit
	CS1W-OC211	16-point Output Unit
Triac Output Unit	CS1W-OA201	16-point Output Unit
	CS1W-OA211	16-point Output Unit
Transistor Output Unit	CS1W-OD211/212	16-point Output Unit
	CS1W-OD231/232	32-point Output Unit
	CS1W-OD261/262	64-point Output Unit
	CS1W-OD291/292	96-point Output Unit
DC Input/Transistor Output Unit	CS1W-MD261/262	64-point I/O Unit
	CS1W-MD291/292	96-point I/O Unit

Note

1. An I/O setting error will occur if Units are not set correctly.
2. An I/O verification error will occur if the number of input or output words is set incorrectly.

2-14-2 CS-series Special I/O Units

Name	Model	Unit type	Number of unit numbers	Allocated words	
				Inputs	Outputs
Analog I/O Unit	CS1W-MAD44	Other Special I/O Units	1	5	5
Analog Input Units	CS1W-AD041/081(-V1)	Other Special I/O Units	1	9	1
Analog Output Units	CS1W-DA041/08V/08C	Other Special I/O Units	1	1	9
Isolated Thermocouple Input Unit	CS1W-PTS01-V1/11	Other Special I/O Units	1	10	0
Isolated Resistance Thermometer Input Unit	CS1W-PTS02/03/12	Other Special I/O Units	1	10	0
Isolated Ni508Ω Resistance Thermometer Input Unit	CS1W-PTS03	Other Special I/O Units	1	10	0
Isolated 2-wire Transmission Device Input Unit	CS1W-PTW01	Other Special I/O Units	1	10	0
Isolated DC Input Unit	CS1W-PDC01/11	Other Special I/O Units	1	10	0
Isolated Control Output Unit (Analog Output Unit)	CS1W-PTR01	Other Special I/O Units	1	10	0
Power Transducer Input Unit	CS1W-PTR02	Other Special I/O Units	1	10	0
DC Input Unit (100 mA)	CS1W-PMV01	Other Special I/O Units	1	5	5
Isolated Pulse Input Unit	CS1W-PPS01	Other Special I/O Units	1	10	0
Motion Control Units	CS1W-MC221(-V1)	Other Special I/O Units	3	20	10
	CS1W-MC421(-V1)	Other Special I/O Units	5	32	18
Position Control Units	CS1W-NC113/133	Other Special I/O Units	1	3	2
	CS1W-NC213/233	Other Special I/O Units	1	6	4
	CS1W-NC413/433	Other Special I/O Units	2	12	8
Customizable Counter Units	CS1W-HIO01/HCP22/HCA22-V1	Other Special I/O Units	1	5	5
High-speed Counter Unit	CS1W-CT021/041	Other Special I/O Units	4	26	14
GPIB Interface Unit	CS1W-GPI01	Other Special I/O Units	1	5	5

Note A Special I/O setting error will occur if Units, the number of input, or the number of output words is set incorrectly.

2-14-3 CS-series CPU Bus Units

Name	Model	Unit type
Controller Link Units	CS1W-CLK11 CS1W-CLK21/12/52-V1	Controller Link Unit
Serial Communications Unit	CS1W-SCU21-V1	Serial Communications Unit
Ethernet Units	CS1W-ETN21	Ethernet Unit
CS1D Ethernet Unit	CS1D-ETN21D	CS1D Ethernet Unit (See note.)
NX Service Units	CS1W-NXS01/11	NX Service Unit
SYSMAC LINK Unit	CS1W-SLK21	SYSMAC LINK Unit
DeviceNet Unit	CS1W-DRM21-V1	DeviceNet Unit
FL-Net Units	CS1W-FLN12	FL-Net Unit
PROFIBUS-DP Master Unit	CS1W-PRM21	PROFIBUS Master Unit
Open Network Controllers	ITNC-EIS/EIX-CST	ONC/CS1 Bus IF
	ITBC-CST01	

Note Supported from CS-Programmer version 4.0 or higher.

SECTION 3
Duplex Functions

This section describes the basic operation of a Duplex System.

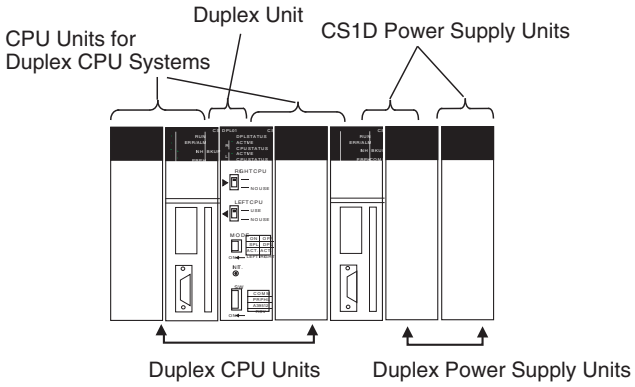
3-1 Duplex CPU Units

3-1-1 Duplex CPU Systems

A Duplex CPU System consists of two CPU Units for Duplex CPU Systems and one Duplex Unit mounted to a CS1D Backplane for Duplex CPU Systems.

Note

1. A Duplex CPU System must be used for Duplex CPU Unit operation. Duplex CPU Units cannot be used in a Single CPU Systems.
   Also, Duplex can be performed only among CPU Units of the same model. For example, Duplex cannot be performed through a combination of the CS1D-CPU65H and the CS1D-CPU67H, or the CS1D-CPU67H and the CS1D-CPU67HA, etc.
   However, CS1D-CPU67HA has a function that enables Duplex with the CS1D-CPU65/67H. (Refer to *3-1-8 Duplex CPU Compatible Setting* for details)
2. Inner Boards cannot be mounted in CPU Units for Duplex CPU Systems. The only Inner Boards that can be used for Duplex CPU Systems is the CS1D-LCP05D built into the CS1D-CPU□□P Process-control CPU Units.
3. Memory Card functions can be executed in duplex only when the doing so is enabled in the PLC Setup. No processing, however, is executed during duplex initialization to match the data on the Memory Cards mounted in the active and standby CPU Units. Therefore, before enabling duplex operation for Memory Cards, make sure that the contents and the capacities are the same for both of the Memory Cards. If the free space or the contents are different, write processing to the Memory Cards may not be completely correctly.
4. EM file memory is configured in duplex between the two CPU Units.



Two Modes in a Duplex CPU System

A Duplex CPU System can be operated in either Duplex Mode or Simplex Mode.

Duplex Mode	In Duplex Mode, two CPU Units (active and standby) operate in a duplex configuration. When an error causing operation to switch to the standby occurs, the standby CPU Unit automatically switches to active status.
Simplex Mode	In Simplex Mode, a single CPU Unit controls operations independently. The Duplex System goes into Simplex Mode either as a result of an error causing operation to switch to the standby while in Duplex Mode or when Simplex Mode is selected using the Mode Setting Switch.

- The mode can be toggled between Duplex Mode and Simplex Mode by means of the Mode Setting Switch on the Duplex Unit.

- The present mode status is displayed by the DPL STATUS indicator on the Duplex Unit (green flashing: Duplex Mode; OFF: Simplex Mode). It can also be checked by means of A32808 in the Auxiliary Area (ON: Duplex Mode, OFF: Simplex Mode).

Active and Standby CPU Units

In Duplex Mode, the two CPU Units run the same user program. One of them executes actual control (e.g., refreshing the other Units), and the other one remains on standby as a backup.

The two CPU Units use synchronized processing and the same user program, I/O memory, and Parameter Area data.

Active CPU Unit	The active CPU Unit is the main CPU Unit that executes control. It runs the user program and exchanges data with external devices (through mounted Units and communications).
Standby CPU Unit	The standby CPU Unit runs the user program in parallel with the active CPU Unit, and remains on standby to switch to active status in case the active CPU Unit goes down. It constantly receives updated data from the active CPU Unit.

- The setting at the Active Setting Switch on the Duplex Unit determines which of the two CPU Units is to be active.
- The R and L ACTIVE indicators on the Duplex Unit show which of the two CPU Units is active. The active/standby status can also be checked using A32809 in the Auxiliary Area.

Active and Standby CPU Unit Operations

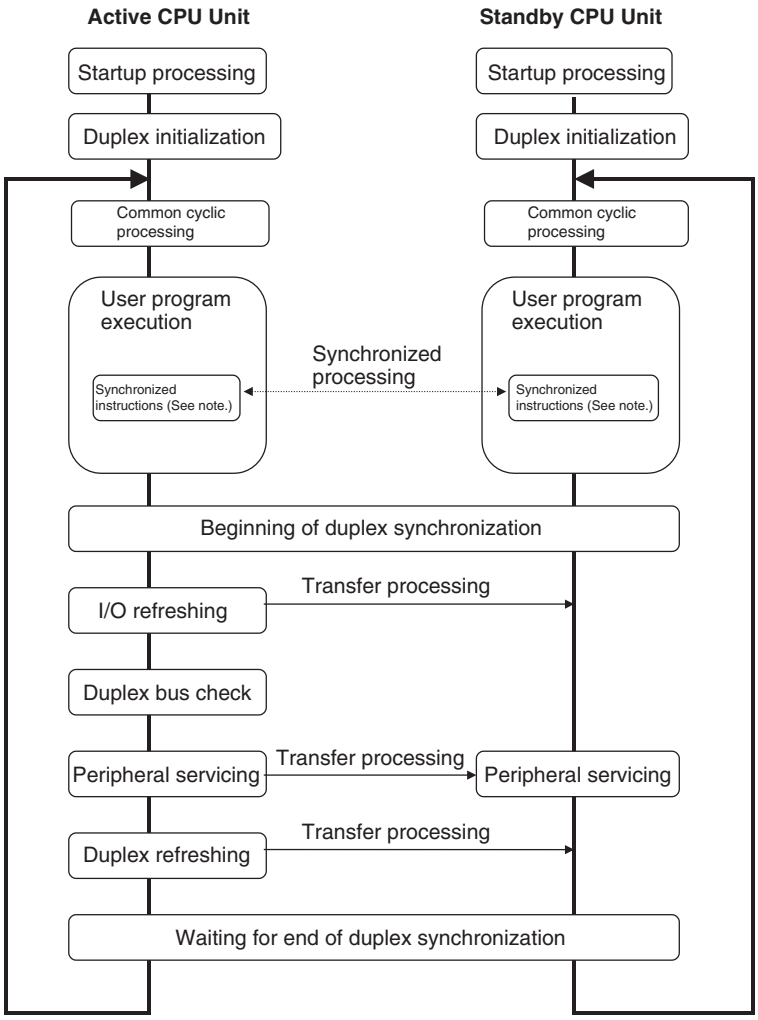
When the user program or parameters (e.g., PLC Setup) are changed, they are transferred from the active CPU Unit to the standby CPU Unit. I/O memory is transferred with each cycle. (These transfers are called “duplex transfers.”)

The details of active and standby CPU Unit operations are described below.

Data Transfers

Data	CPU Unit		
	Active CPU Unit	→	Standby CPU Unit
User program	Transferred from active to standby CPU Unit whenever changed.		
I/O memory	Constantly transferred from active to standby CPU Unit.		
Parameters	Transferred from active to standby CPU Unit whenever changed.		

Cyclic Operations



Note These instructions include IORF(097) (I/O REFRESH), DLINK(226) (CPU BUS UNIT I/O REFRESH), IORD(222) (INTELLIGENT I/O READ), IOWR(223) (INTELLIGENT I/O WRITE), PID(190) (PID), RXD(235) (RECEIVE), FREAD(700) (READ DATA FILE), FWRIT(701) (WRITE DATA FILE) and TWRIT(704) (WRITE TEXT FILE) .

The following table shows the processing related to duplex operation. For details, refer to *SECTION 9 CPU Unit Operation and the Cycle Time*.

Processing	Duplex-related processing
Startup processing	Duplex status is checked (i.e., whether the Unit status is active or standby).
Duplex initialization	Data is transferred from the active CPU Unit to the standby CPU Unit, and verified. (Details are provided below.)
Beginning of duplex synchronization and Waiting for end of duplex synchronization	In a Duplex CPU System, synchronization processing is executed in order to coordinate the timing of active and standby CPU Unit operations.

Processing	Duplex-related processing
User program execution	The same user program is executed. Synchronized instructions (see note) are executed simultaneously for both the active and standby CPU Units. **Note** These instructions include IORF(097) (I/O REFRESH), DLINK(226) (CPU BUS UNIT I/O REFRESH), IORD(222) (INTELLIGENT I/O READ), IOWR(223) (INTELLIGENT I/O WRITE), PID(190) (PID), RXD(235) (RECEIVE), FREAD(700) (READ DATA FILE), FWRIT(701) (WRITE DATA FILE) and TWRIT(704) (WRITE TEXT FILE) .
I/O refreshing	Inputs and outputs are refreshed only by the active CPU Unit. When inputs are refreshed, the input data is transferred to the standby CPU Unit.
Duplex bus check	A bus check is executed between the active CPU Unit, Duplex Unit, and standby CPU Unit.
Peripheral servicing	Writing for file accessing and FINS command execution is processed only for the active CPU Unit. Reading for file accessing and FINS command execution is processed for both the active and standby CPU Units. With RS-232C port servicing, only reading can be processed at the standby CPU Unit (i.e., when enabled in the PLC Setup). Peripheral servicing other than the above is executed only at the active CPU Unit.
Duplex refreshing	The Auxiliary Area status and error content at the active CPU Unit are copied to the standby CPU Unit.

Duplex Power Supply Units

Power Supply Units can be used in a duplex configuration.

The mode does not change between Duplex Mode and Simplex Mode as a result of Power Supply Unit errors.

Note CS1D Power Supply Units must be used.

Duplex Communications Units

Optical Controller Link Units or Ethernet Units can be used in a duplex configuration.

The mode does not change between Duplex Mode and Simplex Mode as a result of Communications Unit errors.

Note Duplex Ethernet Units are supported only by CPU Unit Ver. 1.1 or later.

3-1-2 Errors Causing Operation to Switch to the Standby CPU Unit

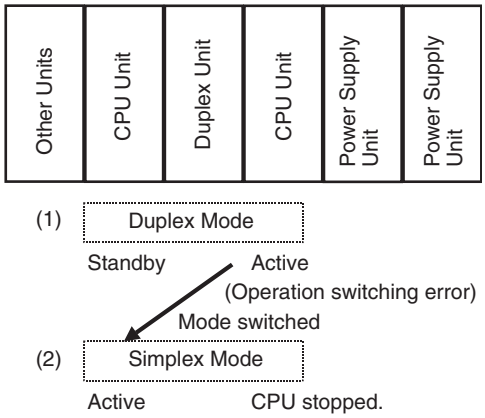
If any of the “operation switching” errors listed below occur in the active CS1D CPU Unit, causing it to stop operating, control is automatically switched to the standby CPU Unit. At that time, the mode is also switched to Simplex Mode.

If, however, an operation switching error or a fatal error occurs simultaneously at the active and standby CPU Units, the system will stop operating.

Operation switching errors

- Watchdog timer error (CPU error)
- Memory error: Memory Error Flag (A40115) turns ON. (Previously this was a fatal error.)
- Program error: Program Error Flag (A40109) turns ON. (Previously this was a fatal error.)
- Cycle time overrun: Cycle Time Overrun Flag (A40108) turns ON.

- Fatal Inner Board error: Fatal Inner Board Error Flag (A40112) turns ON. (This is a fatal error for Single CPU Systems or the CS1-H.) (Process-control CPU Units only)
- FALS error: FALS Error Flag (A40106) turns ON. (Previously this was a fatal error.)
- Power OFF (when the CPU Setting Switch on the active CPU Unit is switched from USE to NO USE)



The CPU Unit where the error occurred can be replaced while the system continues operating using the CPU Unit online replacement function.

Note

1. To determine the cause of a switch to the standby CPU Unit, refer to A023 in the Auxiliary Area or to *Mode Switch Reference*, below.
2. In Simplex Mode, or in a Simplex System, operation stops when any of the above errors occur.
3. When the mode is switched from Duplex Mode to Simplex Mode due to an operation switching error or a duplex error, the cause of the mode switch and the time at which it occurred are stored in the Auxiliary Area of the newly active CPU Unit (i.e., the active CPU Unit following the mode switch).

Causes of Mode Switching

Word	Bit	Description
A023	A02300	ON when mode is switched due to a duplex verification error.
	A02301	ON when mode is switched due to a duplex bus error.
	A02303	ON when mode is switched by the CPU Setting Switch.
	A02304	ON when mode is switched due to a CPU error (watchdog timer error).
	A02306	ON when mode is switched due to a FALS error.
	A02308	ON when mode is switched due to cycle time overrun error.
	A02309	ON when mode is switched due to a program error.
	A02312	ON when mode is switched due to a fatal Inner Board error.
	A02315	ON when mode is switched due to a memory error.

Time when Switching Occurred

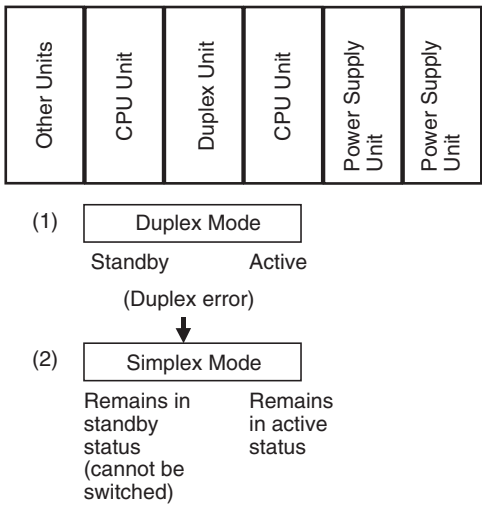
Words	Description
A024 to A026	The time at which the mode was switched from Duplex Mode to Simplex Mode is stored as follows: A02400 to A02407: Second (00 to 59) A02408 to A02415: Minute (00 to 59) A02500 to A02507: Hour (00 to 23) A02508 to A02515: Day (01 to 31) A02600 to A02607: Month (01 to 12) A02608 to A02615: Year (00 to 99)

The above Auxiliary Area words are cleared when the mode is restored from Simplex Mode to Duplex Mode. At that time, the contents of A023 are transferred to A019, and the contents of A024 to A026 are transferred to A020 to A022, as an error log.

3-1-3 Duplex Errors

If an error occurs in the duplex processing itself, the mode is switched from Duplex Mode to Simplex Mode. At that time, operation continues with the presently active CPU Unit retaining its active status and the standby CPU Unit remaining on standby.

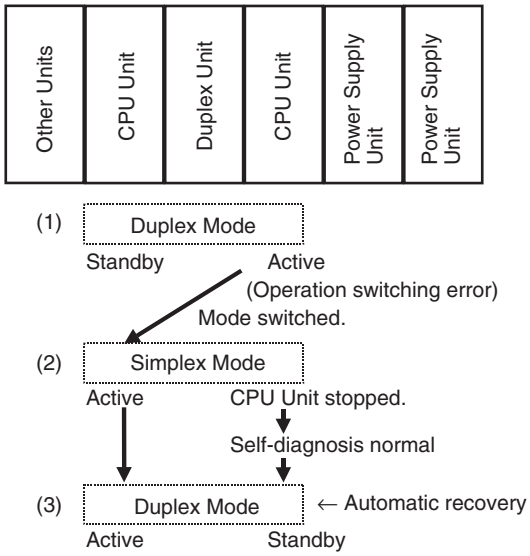
Duplex errors	Duplex bus error	An error has occurred in the Duplex System's duplex bus. (A31601 turns ON. Error code: 0010 hex)
	Duplex verification errors	One of the following items does not match between the active and standby CPU Units. (A31600 turns ON. Error code: 0011 hex) User program or Parameter Area data System configuration (CPU Unit models or Duplex Inner Boards) **Note** 1. There is no verification of Memory Card, including installation, models, and data contents, or verification of front-panel DIP switch status. Even if any of these do not match, operation will continue in Duplex Mode. 2. The causes of duplex verification errors are stored in the following bits of A317 in the Auxiliary Area. Bit 07: CPU Unit Model Verification Error Flag Bit 08: CPU Unit Version Verification Error (CS1D CPU Unit Ver. 1.1 or later only) Bit 10: Duplex Inner Board Model Verification Error Flag (Process-control CPU Units only) Bit 13: Parameter Area Verification Error Flag Bit 14: No Active CPU Unit Error Flag Bit 15: User Program Verification Error Flag



3-1-4 Automatic Recovery to Duplex Operation by Self-diagnosis

After the mode has been switched from Duplex Mode to Simplex Mode due to an operation switching error or a duplex error, an automatic attempt is made to return to Duplex Mode if this function has been enabled in the PLC Setup. This function is mainly useful for momentary or incidental disruptions (to memory, bus, etc.) due to factors such as noise, rather than for hardware breakdowns.

When this automatic recovery function is executed, it does not return standby status to active.



Note

1. In order for automatic recovery to be enabled, the power to the other CPU Unit must not be OFF and the Mode Setting Switch must be set to DPL. If the mode cannot be automatically returned to Duplex Mode, the following bits in the Auxiliary Area (CPU Unit Duplex Unit Recovery Flags) will turn ON.
   Right CPU Unit: A32814 turns ON.
   Left CPU Unit: A32815 turns ON.
2. When Duplex Mode operation has been recovered, the error log automatically will be transferred from the new active CPU Unit to the new standby CPU Unit (i.e., the one that was the active CPU Unit before). To check the

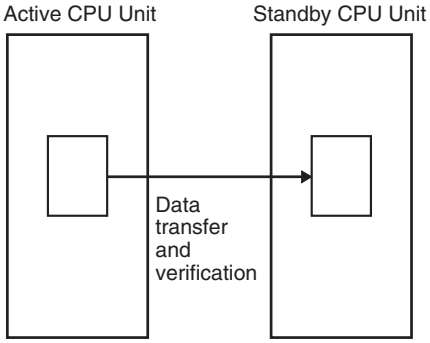
reason the standby CPU Unit previously failed (i.e., the reason for switching to Simplex Operation) or the time the switch was made, use A019 (reasons for switching) and A020 to A022 (time of switching).

3-1-5 Duplex Initialization

In Duplex Mode, duplex initialization is executed automatically at certain times in order to synchronize the data in the active and standby CPU Units. The duplex initialization is executed at times such as when the power is turned ON, when operation is started, when transferring user programs or PLC Setup data, etc.

By means of this duplex initialization, data is transferred from the active CPU Unit to the standby CPU Unit and verified.

Duplex Initialization Processing



- During duplex initialization, the DPL STATUS indicator on the Duplex Unit flashes green.
- During duplex initialization, the cycle time is temporarily extended.
- During duplex initialization, the mode is temporarily switched to Simplex Mode. If an operation switching error occurs during this interval, operation will not be continued.

Duplex initialization is executed automatically at the following times.

When power is turned ON	When the power is turned ON while the Mode Setting Switch is set to DPL.
When the Initial Switch is pressed	When the Initial Switch is pressed while the Mode Setting Switch is set to DPL.
At the start of operation	When operation is started while the Mode Setting Switch is set to DPL (i.e., moving from PROGRAM Mode to RUN or MONITOR Mode).
When data is transferred	When a user program is transferred to the active CPU Unit. When PLC Setup data is transferred to the active CPU Unit. When I/O tables are created at the active CPU Unit. When CPU Bus Unit system settings are written to the active CPU Unit. When online editing is executed at the active CPU Unit. When Timer/Counter set values are changed at the active CPU Unit.

During duplex initialization, the cycle time becomes longer than normal, as follows:

Maximum cycle time = Normal cycle time + α

CS1D CPU Unit model	α (Maximum time beyond normal cycle time)
CS1D-CPU67HA	520 ms
CS1D-CPU68HA	900 ms
CS1D-CPU65H	190 ms + A
CS1D-CPU67H	520 ms + A

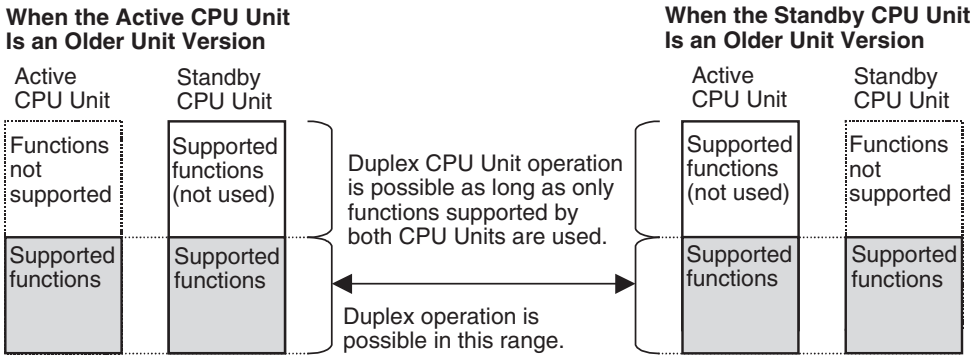
A is the time added when duplex Inner Boards are mounted. Refer to the Inner Board Operation Manual for the value of A.

3-1-6 Duplex CPU Units with Different Unit Versions

Unit versions are used to identify functional additions to CS1D CPU Units. (Refer to information on unit versions at the front of this manual for details.) Upward compatibility is provided for all functional additions to CS1D CPU Units. Duplex CPU Unit operation is thus possible for CPU Units of different unit versions as long as only the functions supported by both unit versions are used.

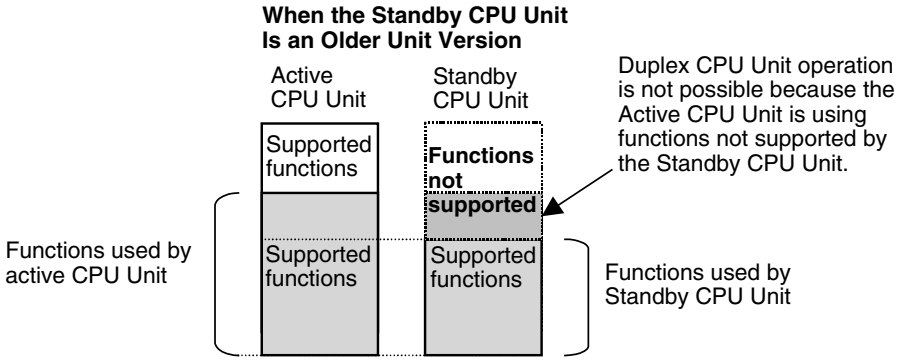
Requirements for Duplex CPU Units

Duplex CPU Unit operation is possible as long as the active CPU Unit does not use any functions not supported by the standby CPU Unit.



When Duplex CPU Unit Operation Is Not Possible

Duplex CPU Unit operation is not possible if the unit version of the active CPU Unit is earlier than that of the standby CPU Unit and the Active CPU Unit uses functions not supported by the Standby CPU Unit. If this happens, a Duplex Verification Error will occur and operation will be in Simplex Mode.



A31708 will turn ON to indicate a CPU Unit Version Verification Error as the cause of the Duplex Verification Error. This error will be detected at the following times.

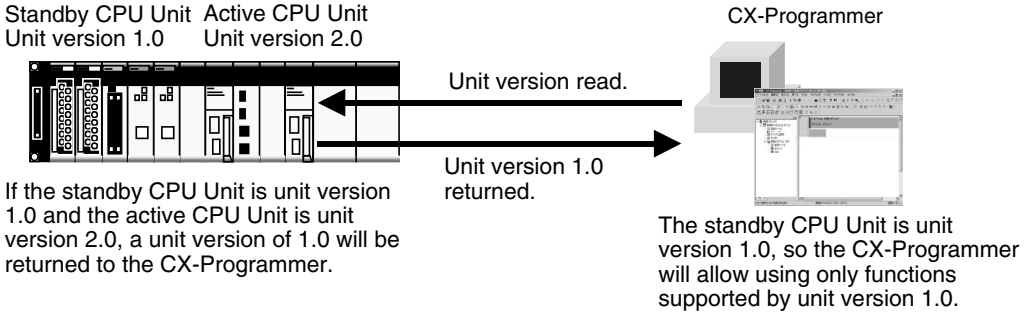
- When the system is started (i.e., when the power supply is turned ON)
- When operation is switched from Simplex Mode to Duplex Mode

- When using new functions is specified

If duplex operation is prevented by a Duplex Verification Error, duplex operation can be recovered by stopping functions on the active CPU Unit that are not supported by the standby CPU Unit. When a CPU Unit Version Verification Error has occurred, the flags in A804 can be checked to identify the functions that are not supported in the standby CPU Unit. (This function is supported by CS1D CPU Units with unit version 1.3 or later only.)

Unit new functions can be specified from the Programming Console, by downloading files from a Memory Card, or by FINS write commands.

The CX-Programmer detects the unit versions of the CPU Units and allows only functions supported by both. (The active CPU Unit compares it's unit version to that of the standby CPU Unit and transfers the earlier unit version to the CX-Programmer.) It is thus not possible to specify using functions not supported by the standby CPU Unit.



Note The CX-Programmer checks the unit version when going online with the PLC or when opening any of the setting windows, such as the PLC Setup Window. The CX-Programmer will not update the unit version following online replacement of a Unit, and thus any data transfers will be performed as if the previous unit version was still valid even if the unit version has been changed in the online replacement procedure. After replacing a Unit online, restart the CX-Programmer or perform another action to update the unit version information before transferring data.

3-1-7 Duplex CPU System Restrictions

This section describes the restrictions that apply to CS1D Duplex CPU Systems.

System Configuration Restrictions

- C200H Units (e.g., C200H Basic I/O Units, Group-2 High-density I/O Units, and C200H Special I/O Units) cannot be used.
- Inner Boards cannot be mounted in CPU Units for Duplex CPU Systems. The only Inner Boards that can be used for Duplex CPU Systems is the CS1D-LCP05D built into the CS1D-CPU□□PProcess-control CPU Units. (The CS1D-LCP05D Loop Control Board cannot be ordered separately and must be ordered as part of a CS1D-CPU□□P Process-control CPU Unit.)
- Memory Card functions can be executed in duplex only when the doing so is enabled in the PLC Setup. No processing, however, is executed during duplex initialization to match the data on the Memory Cards mounted in the active and standby CPU Units. Therefore, before enabling duplex operation for Memory Cards, make sure that the contents and the capacities are the same for both of the Memory Cards. If the free space or the

contents are different, write processing to the Memory Cards may not be completely correctly.

- Duplex operation is possible for EM file memory.

Operational Restrictions

- Interrupts (including scheduled interrupt tasks, external interrupt tasks, and power OFF interrupt tasks) cannot be used.
- Parallel processing for peripheral servicing (Parallel Processing Mode and Peripheral Servicing Priority Mode) cannot be executed.
- The clock function is synchronized with the active CPU Unit.

Instruction Restrictions

- Instructions with the immediate refresh option (!) cannot be used. (The IORF instruction, however, is available.)
- The accuracy of timer instructions (TIM, TIMX, TIMH(015), TIMHX(551), TMHH(540), TMHHX(552), TTIM(087), TTIMX(555), TIMW(813), TIMWX(816), TMHW(815), TMHWX(817), TIML(542), TIMLX(553), MTIM(543), and MTIMX(554)) is less than for CS1-H CPU Units. The accuracy is as follows:
  TIM, TIMX, TIMH(015), TIMHX(551), TMHH(540), TMHHX(552), TTIM(087), TTIMX(555), TIML(542), TIMLX(553), MTIM(543), MTIMX(554), TIMW(813), TIMWX(816), TMHW(815), TMHWX(817): ±(10 ms + cycle time)

Note If the mode is changed from Duplex Mode to Simplex Mode during execution of a timer instruction, the accuracy in the first cycle following the mode switch is less than normal (as shown below).
TIM, TIMX, TIMH(015), TIMHX(551), TTIM(087), TTIMX(555), TIML(542), TIMLX(553), MTIM(543), MTIMX(554), TIMW(813), TIMWX(816), TMHW(815), TMHWX(817) : ±(10 ms + cycle time) ±10 ms
TMHH(540), TMHHX(552) : ±(10 ms + cycle time) ±20 ms

Reference: Timer accuracy for the CS1-H is as follows:
TIM, TIMX, TIMH(015), TIMHX(551), TTIM(087), TTIMX(555), TIML(542), TIMLX(553), MTIM(543), MTIMX(554), TIMW(813), TIMWX(816), TMHW(815), TMHWX(817) : 0 to −10 ms
TMHH(540), TMHHX(552) : 0 to −1 ms

- PV refresh operations during timer instruction jumps, or while a block program is stopped, are described below. (Operation is different from CS1-H CPU Units.)
  a) TIM, TIMX, TIMH(015), TIMHX(551), TMHH(540), TMHHX(552), TTIM(087), TTIMX(555):
  When a jump is executed for a JMP, CJMP, or CMPN-JME instructions, the timer PV is not refreshed (unlike CS1-H CPU Units). The next time the instruction is executed (i.e., the next time the jump is not made) the timer is refreshed for the period of time that elapsed since it was last refreshed.
  b) TIMW(813), TIMWX(816), TMHW(815), and TMHWX(817):
  The timer PV is not refreshed when the BPRG instruction input condition is OFF or when the block program is paused by the BPPS instruction. (It is refreshed for CS1-H CPU Units.)
- Background execution cannot be used for text string processing instructions, table data instructions, or data shift instructions.
- Interrupt control instructions (MSKS, MSKR, CLI) and peripheral servicing disable/enable instructions (IOSP/IORS) cannot be used. (They will be executed as NOPs.)

- Execution of the following instructions (called “synchronized instructions”) is synchronized between the two CPU Units, so their instruction execution times are longer than for the CS1-H. (For details on processing time, refer to *9-5 Instruction Execution Times and Number of Steps*.
  Synchronized instructions:
  IORF(097) (I/O REFRESH), DLINK(226) (CPU BUS UNIT I/O REFRESH), IORD(222) (INTELLIGENT I/O READ), IOWR(223) (INTELLIGENT I/O WRITE), PID(190) (PID), RXD(235) (RECEIVE), FREAD(700) (READ DATA FILE), FWRIT(701) (WRITE DATA FILE) and TWRIT(704) (WRITE TEXT FILE) .
- If the active and standby CPU Units cannot be synchronized when any of the above instructions are executed (except for PID), the ER Flag will turn ON. If that occurs, execute the instruction again.
- Also refer to the precautions in *Appendix E Precautions in Replacing CS1-H PLCs with CS1D PLCs*.

CS1D Error Classifications (Reference)

The underlined errors are related to duplex operation.

Error status		Operation status	
		Duplex Mode	Simplex Mode or Simplex System
Operation switching errors • CPU error • Memory error • Fatal Inner Board error • Program error • Cycle time overrun error • FALS error		Operation continues in Simplex Mode. (The status is switched from standby to active.)	Operation stopped.
Fatal errors • I/O bus error • Duplication error • Too many I/O points error • I/O setting error		Operation stopped.	Operation stopped.
Non-fatal errors	Errors causing a switch to Simplex Mode (duplex errors) • Duplex verification error (See note 1.) • Duplex bus error (See note 1.)	Operation continues in Simplex Mode. (Standby or active status remains unchanged.)	Operation continues in Simplex Mode. **Note** Duplex verification errors and duplex bus errors do not occur in Simplex Mode.
	Non-fatal errors in Duplex Mode • Duplex power supply error • Duplex communications error • FAL error • PLC Setup error • I/O verification error • Non-fatal Inner Board error • CPU Bus Unit error • Special I/O Unit error • Battery error • CPU Bus Unit setting error • Special I/O Unit setting error	Operation continues in Duplex Mode.	
CPU standby (See notes 1 and 2.)		Waits for operation.	Waits for operation.
Expansion Rack power interruption			

Note
1. When a duplex verification error or duplex bus error occurs when the power is turned ON, the CPU Unit goes into “CPU standby” status.
2. The cause of the “CPU standby” is stored in A322 in the Auxiliary Area.

Conditions for Mode Switching in a Duplex System (Reference)

Condition		System operation	Duplex Mode	Active/standby status	
				Active CPU Unit	Standby CPU Unit
When an operation switching error occurs at the active CPU Unit.	Power interruption (when the CPU Setting Switch on the active CPU Unit is switched from USE to NO USE).	Operation continues.	Switched to Simplex Mode	Power interruption	Switched to active. (Operation continues.)
	Watchdog timer error (CPU error)			CPU stopped.	
	Memory error				
	Cycle time overrun				
	Program error				
	FALS error				
	Fatal Inner Board error (Process-control CPU Units only)				
When a duplex error occurs.	Duplex bus error			Remains active. (Operation continues.)	Remains in standby.
	Duplex verification error				
During duplex initialization.			Switched to Simplex Mode	Switching between active and standby is disabled. **Note** If a cause of duplex switching occurs during this interval, operation stops.	
Standby CPU Unit	Power interruption (when the CPU Setting Switch is switched from USE to NO USE).		Switched to Simplex Mode	Remains active. (Operation continues.)	Power interruption
	When one of the following errors occurs: Watchdog timer error, memory error, cycle time overrun error, program error, FALS error, fatal Inner Board error.				Remains in standby.
Mode Setting Switch on Duplex Unit	When set to SPL, and when the Initial Switch is pressed.		Switched to Simplex Mode	Remains active. (Operation continues.)	Remains in standby.
	When set to DPL, and when the Initial Switch is pressed.		No change from Duplex Mode.	Remains active.	Remains in standby.
When a non-fatal error such as a battery error occurs.				Remains active.	Remains in standby.
				Remains active.	Remains in standby.
When a fatal error other than an operation switching error occurs.		Operation stops		Operation stops	Operation stops

3-1-8 Duplex CPU Compatible Setting

The Duplex CPU Compatible Setting on the CS1D-CPU67HA enables the CPU Unit duplexity with the CS1D-CPU65H or CS1D-CPU67H.

■ °**Method of enabling the Duplex CPU Compatible Setting**

Make the changes with the DIP switches (Pin 4, 5, and 6) on the front panel of the CS1D-CPU67HA.

Duplex CPU Compatible Setting	Pin4	Pin5	Pin6	FB/ST/SFC Usage support	Operation
CS1D-CPU67HA (Not set)	OFF	OFF	OFF	Supported	Operates as CS1D-CPU67HA. When you use the programming software, specify CS1D-CPU67HA as PLC type and CPU model and connect to that CPU Unit.
CPU67H mode	ON	OFF	ON	Not supported	Operates as CS1D-CPU67H Ver.1.4. When you use the programming software, specify CS1D-CPU67H as PLC type and CPU model and connect to that CPU Unit.
CPU65H mode	ON	ON	OFF	Not supported	Operates as CS1D-CPU65H Ver.1.4. When you use the programming software, specify CS1D-CPU65H as PLC type and CPU model and connect to that CPU Unit

Note

1. If you set the DIP switches (Pin 4, 5, and 6) to a setting other than the above table and turn ON the power, the DIP switch settings error occurs and the Programming Device can not be connected to that CPU Unit.
2. If the power is turned on with DIP Switches Pin 7 and Pin 8 both ON, a DIP Switch setting error will occur and the peripheral tool cannot be connected.

This setting is valid for both active CPU Unit and standby CPU Unit. The following table shows whether or not duplication of the CPU Unit is possible by combining the CPU Unit model and Duplex CPU compatible setting.

OK: Duplex is supported, --- : Duplex is not supported

Standby CPU / Active CPU	CS1D-CPU65H	CS1D-CPU67H	CS1D-CPU67HA (CPU65H mode)	CS1D-CPU67HA (CPU67H mode)	CS1D-CPU67HA (Not set)	CS1D-CPU68HA
CS1D-CPU65H	OK	---	OK	---	---	---
CS1D-CPU67H	---	OK	---	OK	---	---
CS1D-CPU67HA (CPU65H mode)	OK	---	OK	---	---	---
CS1D-CPU67HA (CPU67H mode)	---	OK	---	OK	---	---
CS1D-CPU67HA (Not set)	---	---	---	---	OK	---
CS1D-CPU68HA	---	---	---	---	---	OK

■ **°Replacement Method**

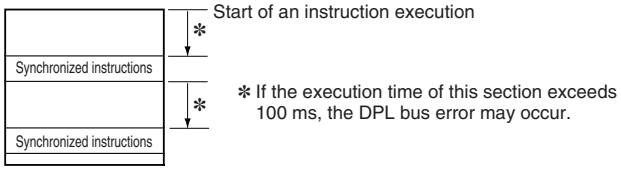
When performing Duplex with CS1D-CPU65H or CPU67H, refer to *11-3 Replacing a CPU Unit for details on the procedure of replacing with the CS1D-CPU67HA*.

■ **Change the Setting**

To change the Duplex CPU Compatible Setting, perform Memory All Clear using the Programming Device and then turn OFF the power supply to the CPU Unit. Changing the duplicated CPU compatible setting without performing Memory All Clearr will result in a memory error (Detailed error: Duplex CPU compatible setting change error).

If all of the following conditions are satisfied, the DPL bus error may occur.

- When duplicating with CS1D-CPU67H and CS1D-CPU67HA (CPU 67H mode)
- When the execution time from the start of instruction execution to the synchronous instruction (*1) or the execution time between synchronous instructions (*1) is 100 ms or more.



If a DPL bus error occurs because one of the above conditions applies, either of the countermeasures below can be taken to remedy the problem.

Countermeasure 1: Use a CS1D-CPU67HA for both the active CPU and the standby CPU.

Countermeasure 2: Add a synchronous instruction so that the execution time from the start of instruction execution until the synchronous instruction, or the execution time between synchronous instructions, is less than 100 ms. Any synchronous instruction can be used.

Put the added synchronous instruction in the execution state.

Example: IORF 999 999

(Use an input/output relay area that is unused)

*1: Instructions requiring synchronization refer to the following instructions.

- IORF (I/O REFRESH)
- DLNK (CPU BUS UNIT I/O REFRESH)
- IORD/IOWR (INTELLIGENT I/O READ/ WRITE)
- PID (PID CONTROL)
- RXD (RECEIVE)
- FREAD/FWRIT/TWRIT (File memory instructions)

■ **List of related AR**

Address		Name	Description	Setting	Held/Cleared		Timing of setting	Related area
Words	Bits				When changing to RUN mode	When power is turned ON		
A317	A31707	CPU Unit Model Verification Error Flag	1 (ON) when the model of the two CPU Units does not match in the Duplex mode, or when the combination of the Duplex CPU compatible setting and CPU model is incorrect.	0: Matched 1: Not matched	Cleared	Cleared	When an error occurs	A316 A32700-03
A327	A32700-03	Duplex CPU Compatible Setting Operating Mode	Indicates the mode in which the CPU Unit is currently operating in the Duplex CPU compatible setting.	0 hex: CPU model which does not support Duplex CPU compatible setting 1 hex: Not set 2 hex: CPU65H mode 3 hex: CPU67H mode	Held	Cleared	When power is turned ON	A40315
A327	A32704-07	Duplex CPU Compatible Setting DIP Switch Setting	The Duplex CPU compatible setting set by the DIP switches is saved.	0 hex: CPU model which does not support Duplex CPU compatible setting 1 hex: Not set 2 hex: CPU65H mode 3 hex: CPU67H mode	Held	Cleared	When power is turned ON	A40315
A403	A40315	Duplex CPU Compatible Setting Change Error	The Duplex CPU compatible setting is changed without executing Memory All Clear.	0: No error 1: Error exists	Held	Cleared	When power is turned ON	A32700-03 A32704-07

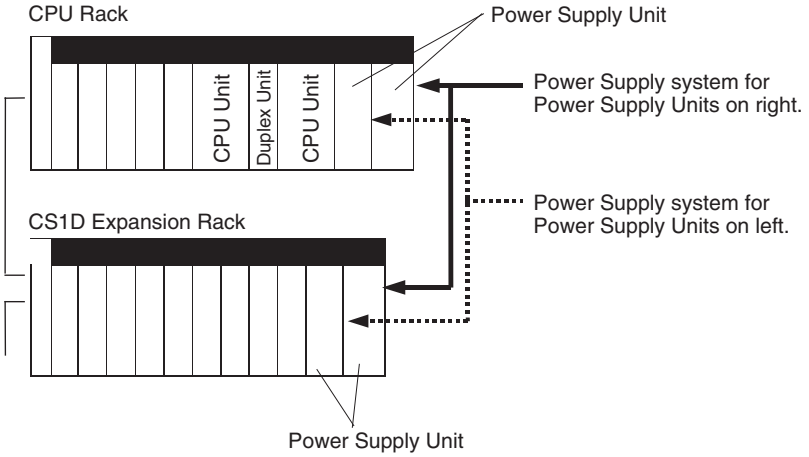
■ **List of related errors**

Error status	Errors that may occur	Detailed error information	Cause	Action
Non-fatal Error	Duplex Verification Error	CPU Unit Model Verification Error Flag (A31707 is 1 (ON))	The CPU Unit model and Duplex CPU compatible setting cannot be combined.	Correct the Duplex CPU compatible setting set by the DIP switches.
Fatal Error	Memory Error	Duplex CPU Compatible Setting Change Error (A40315 is 1 (ON))	The settings of the DIP switches have been changed by mistake during use.	Correct the Duplex CPU compatible setting set by the DIP switches.
			Data has been written to the user program before changing the settings, and the Duplex CPU compatible setting is changed without executing Memory All Clear.	Restart after performing Memory All Clear.
RUN LED flashes and the CPU Unit does not operate. The Programming Device cannot be connected.	DIP Switch Settings Error	None	The DIP switch settings of the CPU Unit are incorrect.	Correct the Duplex CPU compatible setting set by the DIP switches.

3-2 Duplex Power Supply Units

A CS1D Duplex System can be configured with Duplex Power Supply Units to prevent the system from going down due to a Power Supply Unit error.

Be sure to use CS1D-PA/PD□□□ Power Supply Units. No other Power Supply Units can be used in a CS1D System. AC and DC Power Supply Units can be used on the same Backplane.



When two CS1D Power Supply Units (CS1D-PA/PD□□□) are mounted, the Backplane's power supply of 5 V DC and 26 V DC is provided in parallel from the two Power Supply Units.

Even if the power is interrupted at one of the Power Supply Units, or if one of the Power Supply Units breaks down, power can still be provided to the Rack by the other Power Supply Unit alone.

Power Supply Unit errors can be checked using the Programming Console, or by means of A31602, A319, and A320 in the Auxiliary Area.

3-3 Duplex Communications Units

The CS1D supports duplex operation of Ethernet and Controller Link Communications Units. With duplex Communications Units, communications will continue even if errors occur in a Communications Unit or on the communications line.

There are two methods used for duplex communications: Active/standby and primary/secondary. The method that is used depends on the type of Communications Unit that is being used.

Refer to the operation manual for the relative Communications Unit for details on settings and other operating information.

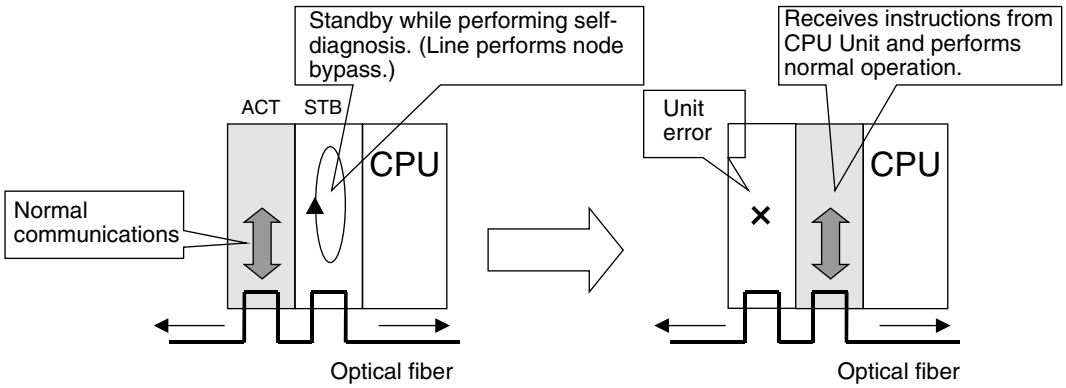
3-3-1 Active and Standby Communications

The active/standby method of communications is used by the following Communications Units. These Units also achieve redundant communications paths by using a loopback.

CS1W-CLK12-V1 Controller Link Unit
CS1W-CLK13 Controller Link Unit
CS1W-CLK52-V1 Controller Link Unit
CS1W-CLK53 Controller Link Unit

Two Communications Units are connected to the same communications line. One of them operates in Active Mode, the other one in Standby Mode. The same unit number and node address are set for both of the Units.

The active (ACT) Communications Unit performs communications with the nodes on the network. The standby (STB) Communications Unit runs on standby while performing self-diagnosis. If the active Communications Unit fails, the standby Communications Unit switches to Active Mode and continues communications operations.



Active/standby communications have been supported since the first CS1D CPU Units were released, so they can be used on any CS1D CPU Unit (including Pre-Ver. 1.1 CPU Units). CX-Programmer version 3.1 or higher is required to make settings for duplex operation.

Up to three pairs of Communications Units using active/standby communications can be used for one CS1D PLC. Even when using Duplex Communications Units, only one unit number is allocated and no restrictions apply to using other CPU Bus Units.

3-3-2 Primary and Secondary Communications

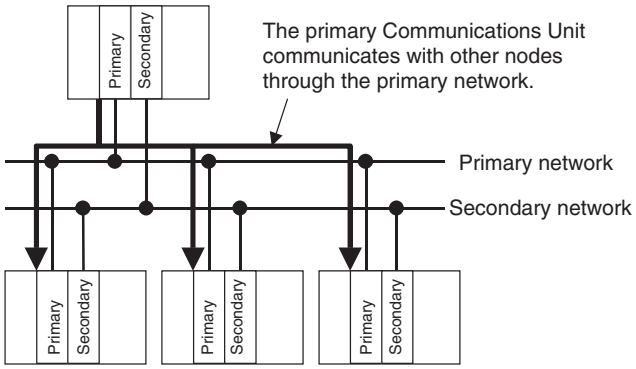
Primary/secondary communications are used with CS1D Ethernet Units (CS1D-ETN21D). Two Communications Units are connected, but each is connected to a different communications line (network). One Unit operates as the primary Communications Unit, the other as the secondary Communications Unit.

The same unit number and node address are set for both of the Units, but two unit numbers (twice the amount of memory) are allocated.

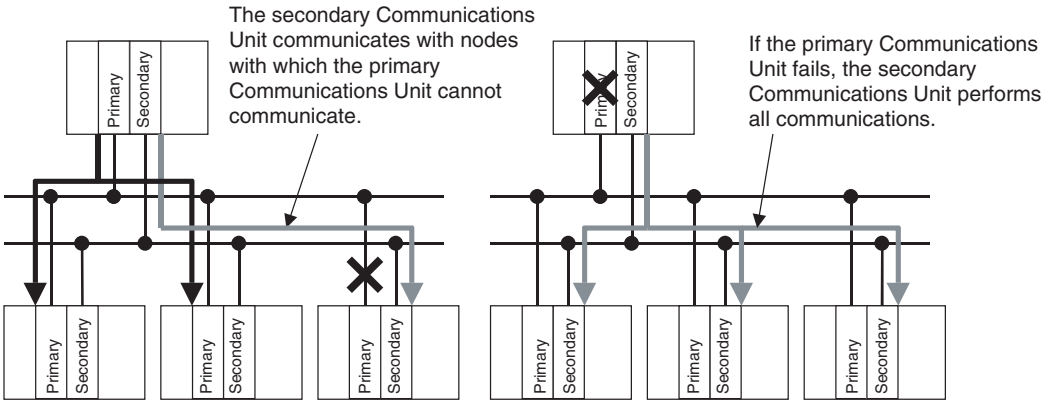
The primary Communications Unit performs communications with the nodes on the primary network while confirming node participation in the primary network. The secondary Communications Unit runs on standby while confirming node participation in the secondary network.

If there is a broken line in the primary network and communications are not possible for a specific node or nodes, the secondary Communications Unit will take over and continue communications with those nodes. If the primary Communications Unit fails, the secondary Communications Unit will take over all communications previously performed by the primary Communications Unit.

Normal Operation



Operation for Errors



CS1D CPU Units for Duplex CPU Systems with a unit version of 1.1 or later or a CS1D CPU Unit for Single CPU Systems with a unit version of 2.0 or later is required to use Duplex Communication Units using primary/secondary communications. CX-Programmer version 2 or higher is required for duplex settings.

Up to three pairs of Communications Units using primary/secondary communications can be used for one CS1D PLC. The are also restrictions in the number of Duplex Communications Units. Refer to the operation manuals for the duplex Communications Units for details.

With duplex communications using primary/secondary communications, memory is allocated for two unit numbers. Although the same unit number is set for both Units, the primary Communications Unit uses the unit number that is set and the secondary Communications Unit uses the next higher unit number. For example, if both Units are set to unit number 0, the memory normally allocated for unit numbers 0 and 1 will be allocated to the duplex Communications Units. The unit number for these duplex Communications Unit cannot be set to 15.

Using a number of pairs of duplex Communications Units using primary/secondary communications will restrict the number of other CPU Bus Units that can be used, as shown in the following table.

Number of pairs of Communications Units using primary/secondary communications	Allowable number of other CPU Bus Units.
0	16
1	14
2	12
3	10

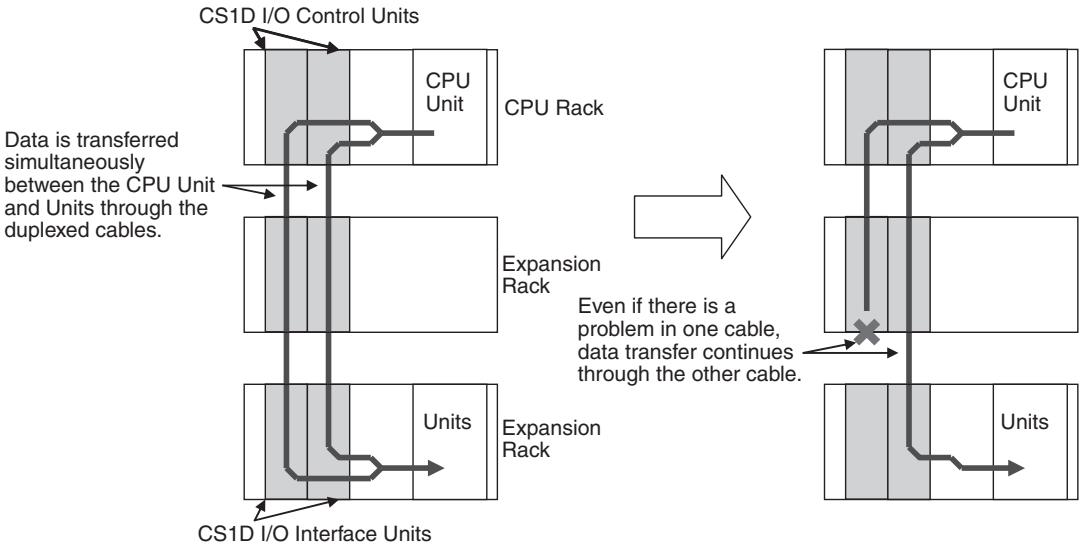
Number of pairs of Communications Units using primary/secondary communications	Allowable number of other CPU Bus Units.
4	8
5	6
6	4
7	2
9	0

Communication Unit settings must be made for both the primary and secondary Communications Unit. Refer to the operation manual for the Communications Units for information on the settings that are required.

Both duplex Ethernet Units will be reset and communications will temporarily stop when I/O tables are created or transferred or Units are added online in a system that uses duplex Ethernet with the CS1D. Confirm that the system will not be adversely affected before executing these operations.

3-4 Duplex Connecting Cables

In a CS1D Duplex CPU, Dual I/O Expansion System, it is possible to duplex the Connecting Cables between the CPU Rack and Expansion Rack and the Connecting Cables between Expansion Racks. The system components required for duplex Connecting Cables are a CS1D-DPL02D Duplex Unit, CS1D-BC042D CPU Backplane, CS1D-BI082D Expansion Backplanes, CS1D-IC102D I/O Control Units, CS1D-II102D I/O Interface Units, and Duplex CPU Units with unit version 1.3 or later.

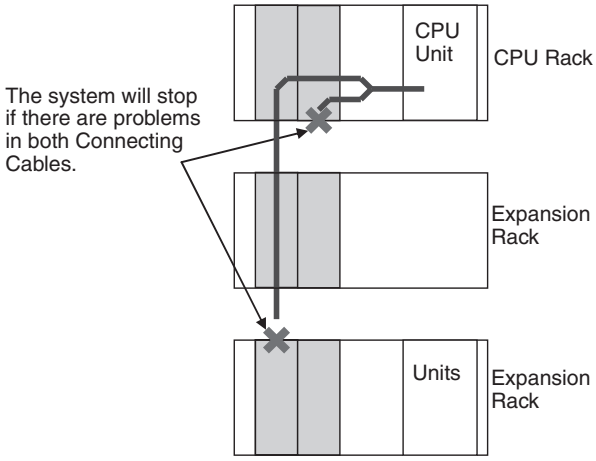


A duplex Connecting Cable system can be configured by mounting two CS1D I/O Control Units in the CPU Rack, mounting two CS1D I/O Interface Units in each Expansion Rack, and connecting the Racks with two Connecting Cables. In a PLC system with duplex Connecting Cables, data is simultaneously transferred over both cables between the CPU Unit and Units in the Expansion Racks.

If one Connecting Cable is disconnected or damaged, data transfer will continue without interruption. When the Cable is reconnected or repaired, duplex Connecting Cable operation will be restored.

Each Connecting Cable's status can be checked with the flags in A270.

Note If there are problems in both Connecting Cables, the system will stop.



SECTION 4
Operating Procedures

This section outlines the steps required to assemble and operate a CS1D PLC system.

4-1 Introduction

The following procedure outlines the recommended steps to follow when preparing a Duplex CPU or Single CPU System for operation.

1,2,3...

1. Installation

   Set the DIP switches on the front of each Unit as required.
   Mount the two CPU Units (see note), Duplex Unit (see note), two Power Supply Units, and other Units to the Backplane. For a Single CPU System, install an Inner Board in the CPU Unit if required.

   Refer to *5-2 Installation* for details.

   Note For a Single CPU System, only one CPU Unit is required and no Duplex Unit is required.

2. Wiring

   Connect the power supply wiring and I/O wiring. Connect communications wiring as required.

   Refer to *5-3 Power Supply Wiring* and *5-4 Wiring Methods* for details on power supply and I/O wiring.

3. Initial Settings (Hardware)

   a) Set the following switches on the front of the Duplex Unit (Duplex CPU Systems only).
   - Set the mode switch (duplex/simplex) to DPL (duplex).
   - Set the active-CPU Unit switch to ACT.RIGHT or ACT.LEFT.
   - Set the CPU USE/NO USE switches to USE.
   - Set the DPL USE/NO USE switch to USE (CS1D-DPL02D only).
   - Set the communications switch on the Duplex Unit.

   b) Set the DIP switches and rotary switches on the front of the CPU Unit and other Units.

   Refer to *SECTION 2 Specifications, Nomenclature, and Functions* for details.

4. Programming Device

   Connect the Programming Device (the CX-Programmer or a Programming Console) to the CPU Unit. (See note.)

   Refer to *2-6 Programming Devices* for details.

   Note With a Duplex CPU System, connect to the active CPU Unit.

5. Checking Initial Operation

   a) Set the operating mode to PROGRAM mode.

   b) Turn the power ON after checking the power supply wiring and voltage. Confirm that the POWER indicator is lit on the Power Supply Unit.

   c) Confirm that the DPL STATUS indicator on the Duplex Unit flashes green and then lights green. (See note.)

   d) Confirm that the ACTIVE indicator on the Active CPU Unit lights green. (See note.)

   Note Duplex CPU System only.

6. PLC Setup Settings

   With the PLC in PROGRAM mode, change the settings in the PLC Setup as necessary from the Programming Device (CX-Programmer or Programming Console). Set settings such as the Duplex Communications Unit settings. (Another method is to change the PLC Setup in CX-Programmer and transfer it to the CPU Unit.)

Refer to *SECTION 6 PLC Setup* for details.

7. Registering the I/O Tables

   Check the Units to verify that they are installed in the right slots. With the PLC in PROGRAM mode, register the I/O tables from the Programming Device (CX-Programmer or Programming Console). (Another method is to create the I/O tables in CX-Programmer and transfer them to the CPU Unit.)

   Refer to *7-1 I/O Allocations* for details.

8. Special I/O Unit, CPU Bus Unit, and Special I/O Unit DM Area Settings

   a) Use a Programming Device (CX-Programmer or Programming Console) to make any necessary settings in the parts of the DM Area that are allocated to Special I/O Units, CPU Bus Units, and Inner Boards.

   b) Reset the power (ON → OFF → ON) or turn ON the Restart Bit for each Unit or Board. See the Unit's or Board's Operation Manual for details.

9. Writing the Program

   Write the program with the CX-Programmer or a Programming Console.

10. Transferring the Program (CX-Programmer Only)

    With the PLC in PROGRAM mode, transfer the program from CX-Programmer to the CPU Unit.

    Note With a Duplex CPU System, transfer the program to the active CPU Unit.

11. Testing Operation

    a) Checking I/O Wiring

Output wiring	With the PLC in PROGRAM mode, force-set output bits and check the status of the corresponding outputs.
Input wiring	Activate sensors and switches and either check the status of the indicators on the Input Unit or check the status of the corresponding input bits with the Programming Device's Bit/Word Monitor operation.

    b) Auxiliary Area Settings (as Required)
    Check operation of special Auxiliary Area Settings such as the following:

Output OFF Bit	When necessary, turn ON the Output OFF Bit (A50015) from the program and test operation with the outputs forced OFF.
Hot Start Settings	When you want to start operation (switch to RUN mode) without changing the contents of I/O memory, turn ON the IOM Hold Bit (A50012).

    c) Trial Operation
    Test PLC operation by switching the PLC to MONITOR mode.

    d) Monitoring and Debugging
    Monitor operation from the Programming Device. Use functions such as force-setting/force-resetting bits, tracing, and online editing to debug the program.
    See *SECTION 7 Program Transfer, Trial Operation, and Debugging* of *CS/CJ Series Programmable Controllers* (W394) for details.
    Perform switching of CPU Units of the CS1D Duplex-CPU System
    Refer to *Appendix H Method of Switching the Operation of a Duplex System by a Program*.

12. Save and print the program.

13. Running the Program
    Switch the PLC to RUN mode to run the program.

4-2 Basic Procedures

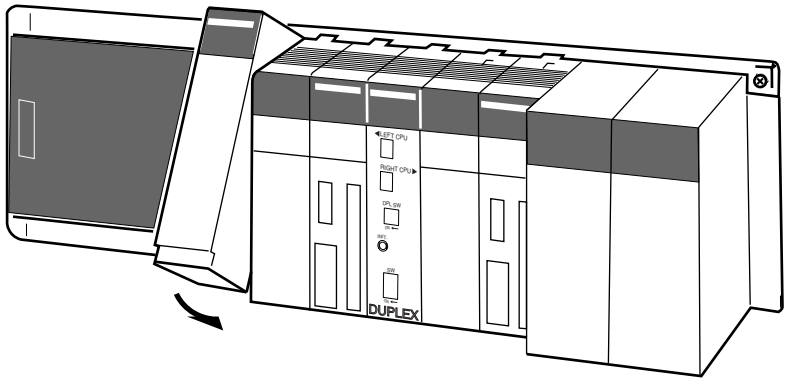
1. Installation

1,2,3...

1. As necessary, set the DIP switches on the fronts of the Units.
2. Mount the two Duplex CPU Units, Duplex Unit, two Power Supply Units, and other Units to the Backplane. Use the same model of CPU Unit for both CPU Units.

   Note a) For a Single CPU System, only one CPU Unit is required and no Duplex Unit is required.

   b) Only one Power Supply Unit is required. Two Power Supply Units are mounted for duplex power supply operation.



3. For a Single CPU System, install an Inner Board in the CPU Unit if required.

2. Wiring

1,2,3...

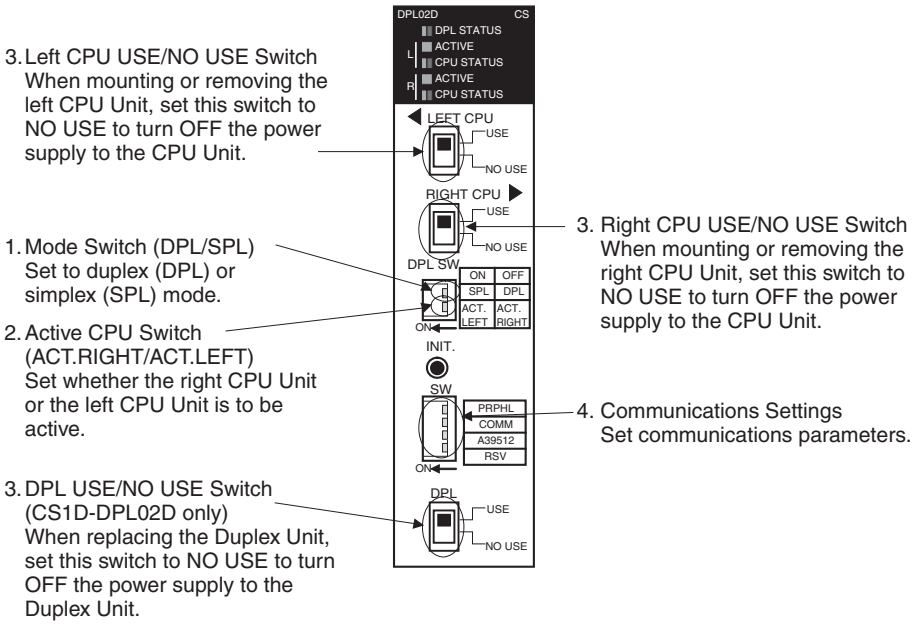
1. Connect the power supply and I/O wiring.
2. Connect communications lines if required.

⚠ **Caution** When 200 to 240 V AC power is being supplied, be sure to remove the jumper bar that shorts the voltage selector terminals. The Power Supply Unit will be damaged if 200 to 240 V AC is supplied with the jumper bar connected.

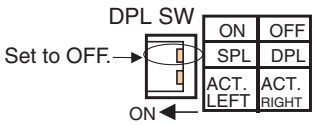
3. Initial Hardware Settings

Settings for Duplex CPU Systems

1,2,3... 1. Duplex Unit Settings

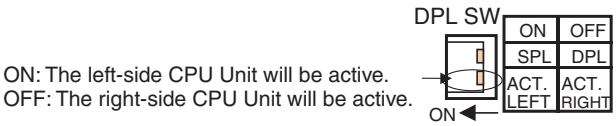


a) Set the mode switch on the Duplex Unit to DPL (duplex).



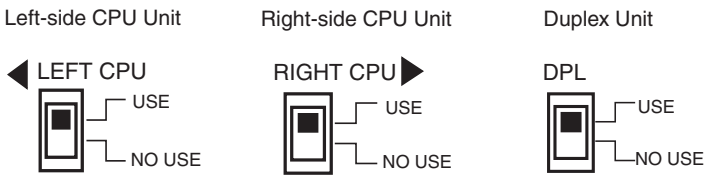
Note For simplex operation, set the mode switch to SPL.

b) Set the active-CPU Unit switch to ACT.RIGHT or ACT.LEFT depending on which CPU Unit is to be used as the active CPU Unit.



Note For simplex operation, set the active-CPU switch to the side where the CPU Unit is mounted.

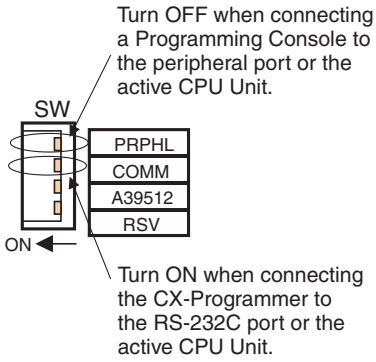
c) Set the Duplex Unit's left and right CPU USE/NO USE switches and DPL USE/NO USE switch to USE. Power will be supplied to the CPU Units and Duplex Unit only when the corresponding switch is set to USE.



Note For simplex operation, set the CPU USE/NO USE switch to USE only for the side where the CPU Unit is mounted.

d) Set the communications switch on the Duplex Unit. When connecting a Programming Console to the peripheral port, set the PRPHL switch to OFF. When connecting the CX-Programmer to the RS-232C port, set the COMM switch to ON.

Note When connecting anything other than a Programming Console to the peripheral port, set the PRPHL switch to ON. When connecting anything other than the CX-Programmer to the RS-232C port, set the COMM switch to OFF.

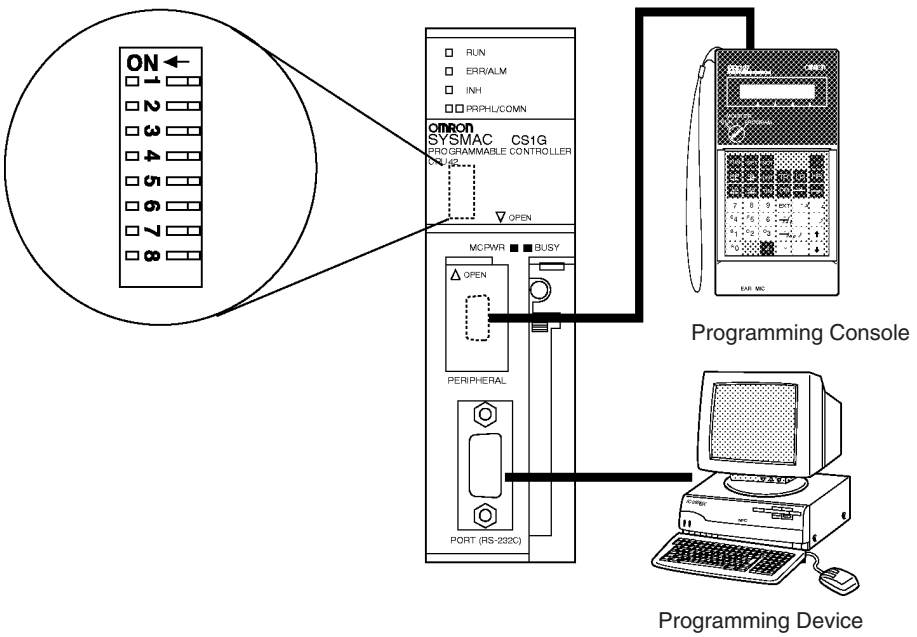


Note In a Duplex CPU System, pin 4 (peripheral port communications settings) on the DIP switches on the fronts of the CPU Units are disabled and the PRPHL setting on the Duplex Unit is used instead. Also, pin 5 (RS-232C port communications settings) on the DIP switches on the fronts of the CPU Units are disabled and the COMM setting on the Duplex Unit is used instead.

2. CPU Unit Settings
   a) Set the DIP switches on the fronts of the two CPU Units to the same settings.
   b) Confirm that both CPU Units are the same model.

Settings for Single CPU Systems

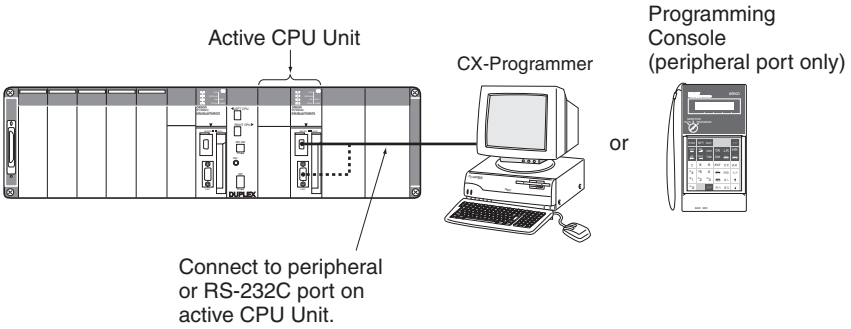
The DIP switch on the front of the CPU Unit must be set, along with other settings. Be particularly careful when setting the peripheral port and RS-232C port settings.



- Turn OFF pin 4 on the DIP switch when connecting a Programming Device to the peripheral port. Turn pin 4 ON when connecting any other device.
- Turn ON pin 5 on the DIP switch when connected a Programming Device other than a Programming Console to the RS-232C port. Turn pin 5 OFF when connecting any other device.

4. Connecting a Programming Device

Connect the CX-Programmer or Programming Console to the active CPU Unit's peripheral port (the upper port) or connect the CX-Programmer to the RS-232C port. (See note.)



Note With a Duplex CPU System, operations, such as generating I/O tables and transferring the program, will not be possible if the Programming Device is connected to the standby CPU Unit.

5. Checking Initial Operation

⚠ **Caution** When 200 to 240 V AC power is being supplied, be sure to remove the jumper bar that shorts the voltage selector terminals. The Power Supply Unit will be damaged if 200 to 240 V AC is supplied with the jumper bar connected.

1,2,3...

1. Check the power supply wiring and voltage and turn ON the power supply to the CS1D Power Supply Units. Confirm that the POWER indicator on the Power Supply Unit when power is turned ON.
2. With a Duplex CPU System, confirm that the DPL STATUS indicator on the front of the Duplex Unit flashes green indicating that duplex operation is being initialized. If initialization is completed normally, the DPL STATUS indicator will stop flashing and remain lit green.

Note If an inconsistency is detected between the two CS1D CPU Units, a duplex verification error will occur and the DPL STATUS indicator will flash red. If this happens, press the initialization switch. Unless there is a hardware error causing the inconsistency, the error should be cleared.

3. With a Duplex CPU System, confirm that the ACTIVE indicator on the active CPU Unit lights green and be sure that the Programming Device is connected to the active CPU Unit.

Note If the PLC Setup's Startup Mode Setting is set to PRCN (Startup Mode determined by the Programming Console's mode switch, the default setting), but a Programming Console isn't connected when the power is turned ON, the CPU Unit will enter RUN Mode and start operating.

6. PLC Setup Settings

These settings are the CPU Unit's software configuration. Refer to *SECTION 6 PLC Setup* for details on the settings.

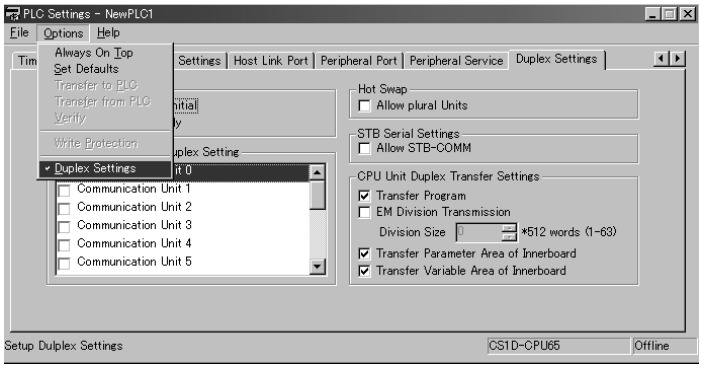
Note The PLC Setup settings are arranged by word addresses when a Programming Console is used to make PLC Setup settings. Refer to *Appendix D PLC Setup Coding Sheets for Programming Console* for details.

Examples:

- For Duplex CPU Systems, setting automatic recovery to duplex mode when an error causes a switch from duplex to simplex mode
- Settings for Duplex Communications Units (CS1W-CLK12-V1 and CS1W-CLK52-V1)
- For Duplex CPU Systems, settings to connect a Programming Device to the RS-232C port on the standby CPU Unit to monitor PLC operation (write operations will not be possible)

Using the CX-Programmer

1,2,3... 1. When setting the device type to "CS1H-H" for a Duplex CPU System, select ***Duplex Settings*** from the Options Menu on the PLC Settings Window to enable setting the PLC Setup for a CS1D from the CX-Programmer.



Note The device type setting on the CX-Programmer depends on the version of CX-Programmer being used. When setting the device type to "CS1H-H" for a Duplex CPU System, select ***Duplex Settings*** from the Options Menu on the PLC Settings Window to enable setting the PLC Setup for a CS1D from the CX-Programmer. For other device type settings, the duplex settings can be made without selecting this option.

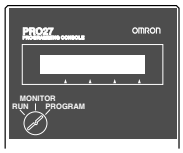
Model	CX-Programmer Ver. 3.□	CX-Programmer Ver. 4.0 or later
CS1D-CPU□□HA	Cannot be selected	CS1D-H *
CS1D-CPU□□H	CS1H-H	CS1H-H or CS1D-H
CS1D-CPU□□SA	Cannot be selected	CS1D-S
CS1D-CPU□□S	Cannot be selected	CS1D-S

* CS1D-CPU□□HA requires CX-Programmer Ver. 9.7 or later.

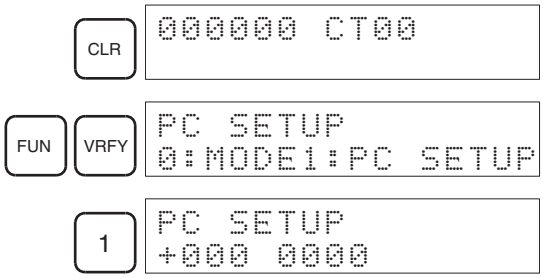
2. Edit the PLC Setup and transfer it to the CPU Unit. (It can be transferred separately or the CXP project can be saved and the PLC Setup can be transferred together with the program.)

Note In a Duplex CPU System, transfer to PLC Setup to the active CPU Unit. (It cannot be transferred to the standby CPU Unit.)

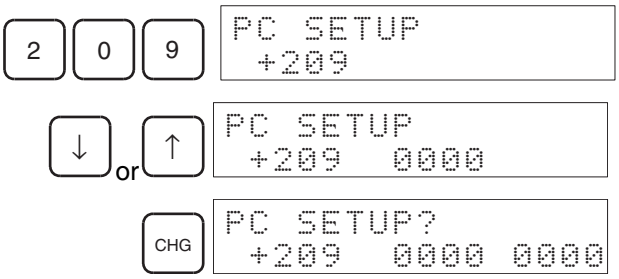
Using a Programming Console



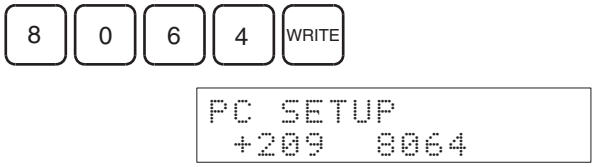
Procedure



Specifying a word address in the PLC Setup.
(Example: 209)



Example: Input 8064.



Address	Bits	Setting	Description
95	00 to 14	Communications Unit Duplex Settings for primary/secondary communications (See note.)	ON: Enable OFF: Disable
121	00 to 15	Communications Unit Duplex Settings for active/standby communications	ON: Enable OFF: Disable
123	15	Automatic Duplex Operation Recovery	ON: Automatic recovery OFF: No automatic recovery
127	00 to 15	Standby CPU Unit RS-232C Port Setting	0000 hex: Do not use independently. 5AA5 hex: Enable independent monitoring.

Note Supported for CPU Unit Ver. 1.1 or later.

7. Registering the I/O Tables in the CPU Unit

Registering the I/O tables allocates I/O memory to the Units actually installed in the PLC. This operation is required in CS-series PLCs.

Note The I/O tables, user program, and PLC Setup data in CS1D CPU Units is backed up in the built-in flash memory. The BKUP indicator will light on the front of the CPU Unit when the backup operation is in progress. Do not turn OFF the power supply to the CPU Unit when the BKUP indicator is lit. The data will not be backed up if power is turned OFF.

Using the CX-Programmer Online

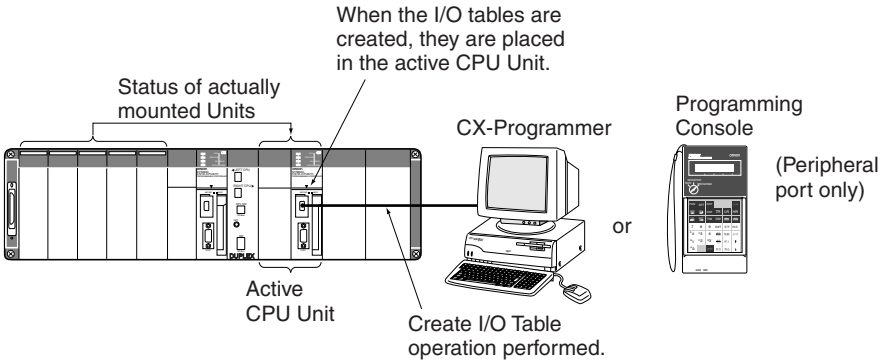
Use the following procedure to register the I/O tables with the CX-Programmer connected to the CPU Unit and all of the Units mounted to the system.

1,2,3... 1. Set the device type in the CX-Programmer as shown in the following table.

Model	CX-Programmer Ver. 3.□	CX-Programmer Ver. 4.0 or later
CS1D-CPU□□HA	Cannot be selected	CS1D-H *
CS1D-CPU□□H	CS1H-H	CS1H-H or CS1D-H
CS1D-CPU□□SA	Cannot be selected	CS1D-S
CS1D-CPU□□S	Cannot be selected	CS1D-S

* CS1D-CPU□□HA requires CX-Programmer Ver. 9.7 or later.

2. Place the CX-Programmer online to the PLC.
3. Create the I/O tables.
   a) With the CPU Unit in PROGRAM mode, double-click ***IO Table*** on the project tree in the main window. The I/O Table Window will be displayed.
   b) Select ***Options*** and then ***Create***. The models and positions of Units mounted to the Racks will be written to the registered I/O tables in the CPU Unit. With a Duplex CPU System running in Duplex Mode, the I/O tables will automatically be created in both the active and standby CPU Units.



Note With a Duplex CPU System, the I/O tables cannot be created directly in the standby CPU Unit.

4. With a Duplex CPU System, confirm that the DPL STATUS indicator on the Duplex Unit flashes green after the I/O tables have been created in the active CPU Unit. This indicates that the duplex system is being initialized, e.g., the I/O tables that were written to the active CPU Unit are also being written to the standby CPU Unit.

Note If an inconsistency is detected between the two CS1D CPU Units, a duplex verification error will occur and the DPL STATUS indicator will flash red. If this happens, press the initialization switch. Unless there is a hardware error causing the inconsistency, the error should be cleared.

Using the CX-Programmer Offline

Use the following procedure to create the I/O tables offline with the CX-Programmer and later transfer the I/O tables to the CPU Unit.

1,2,3... 1. Set the device type in the CX-Programmer as shown in the following table.

Model	CX-Programmer Ver. 3.□	CX-Programmer Ver. 4.0 or later
CS1D-CPU□□HA	Cannot be selected	CS1D-H *
CS1D-CPU□□H	CS1H-H	CS1H-H or CS1D-H
CS1D-CPU□□SA	Cannot be selected	CS1D-S
CS1D-CPU□□S	Cannot be selected	CS1D-S

* CS1D-CPU□□HA requires CX-Programmer Ver. 9.7 or later.

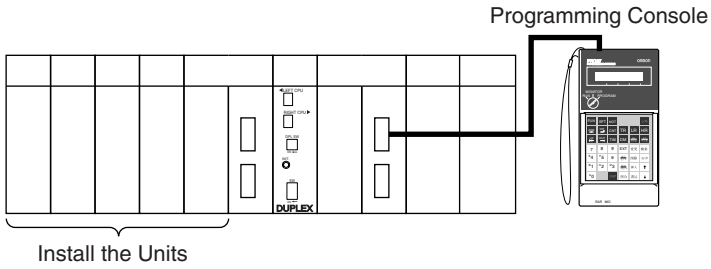
2. Create the I/O tables offline.
   a) Double-click ***IO Table*** on the project tree in the main window. The I/O Table Window will be displayed.
   b) Select ***PLC - PLC Information - I/O Table***, and then double-click the Rack to be edited. The slots for that Rack will be displayed.
   c) Right-click the slots to be edited and select the desired Units from the pull-down menu.
3. Select ***Options*** and then ***Transfer to PLC*** to transfer the I/O tables to the active CPU Unit. The I/O tables will automatically be copied to the standby CPU Unit as well.

Note The first word allocated to each Rack can be set in the PLC Setup under the Options menu.

Using a Programming Console

Use the following procedure to register the I/O table with a Programming Console.

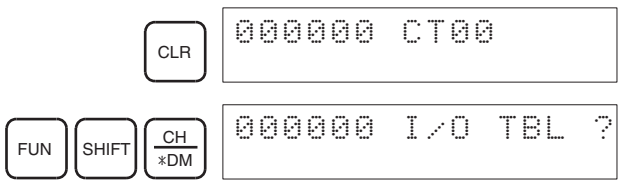
1,2,3... 1. Install all of the Units in the PLC.

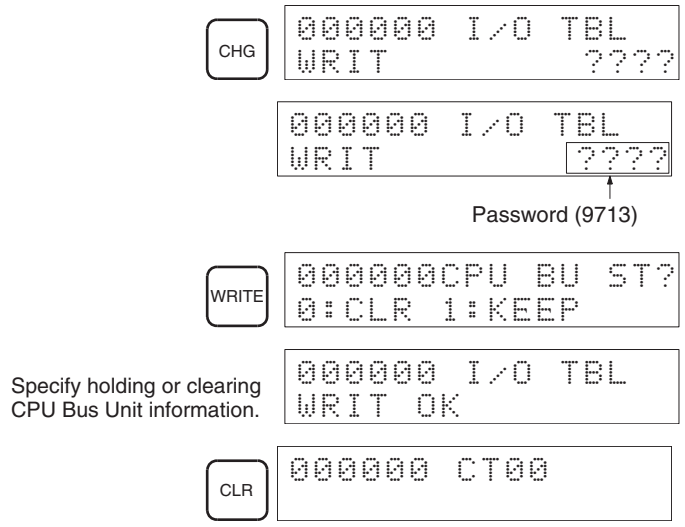


2. Connect the Programming Console to the peripheral port. (See note.) (It can be connected with the power ON.)

   Note With a Duplex CPU System, connect the Programming Console to the active CPU Unit.

3. Register the I/O tables.





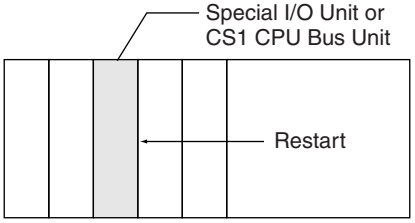
Note If an error occurs when creating the I/O tales, detailed I/O table error information is stored in A261 whenever the I/O tables. This information can be used to identify the Unit causing the error.

8. Special I/O Unit, CPU Bus Unit, and Inner Board Settings

The following table shows the parts of the DM Area are allocated to Special I/O Units, CPU Bus Units, and Inner Boards for initial settings. The actual settings depend on the model of Unit or Inner Board being used.

Unit/Board	Allocated words
Special I/O Units	D20000 to D29599 (100 words × 96 Units)
CPU Bus Units	D30000 to D31599 (100 words × 16 Units)
Inner Board	D32000 to D32099 (100 words × 1 Board)

After writing the initial settings to the DM Area, be sure to restart the Units by turning the PLC OFF and then ON again or turning ON the Restart Bits for the affected Units.



9. Writing the Program

Write the program with the CX-Programmer or a Programming Console.

10. Transferring the User Program, PLC Setup, and DM Area Settings to the CPU Unit

1,2,3... 1. When the user program, PLC Setup, and DM Area Settings have been created in a Programming Device other than a Programming Console, they must be transferred to the CPU Unit. If a Duplex CPU System is being used in Duplex Mode, the data is automatically transferred to both the active and standby CPU Units.

Note The user program and other data cannot be translated directly to the standby CPU Unit.

2. With Duplex CPU Systems, confirm that the DPL STATUS indicator on the Duplex Unit flashes green after the data has been transferred to the active CPU Unit. This indicates that the duplex system is being initialized, e.g., the data that was transferred to the active CPU Unit is also being transferred to the standby CPU Unit.

   Note If an inconsistency is detected between the two CS1D CPU Units, a duplex verification error will occur and the DPL STATUS indicator will flash red. If this happens, press the initialization switch. Unless there is a hardware error causing the inconsistency, the error should be cleared.

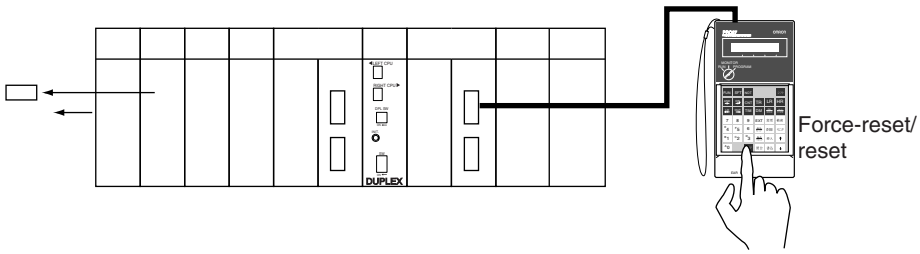
11. Testing Operation

Checking I/O Wiring

Before performing a trial operation in MONITOR mode, check the I/O wiring.

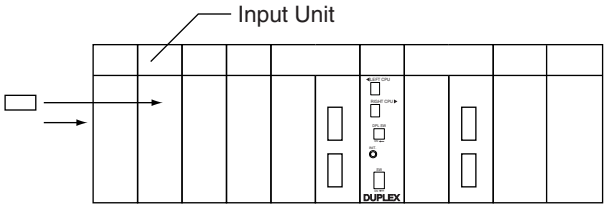
Output Wiring

With the PLC in PROGRAM mode, force-set and force-reset output bits and verify that the corresponding outputs operate properly.



Input Wiring

Activate input devices such as sensors and switches and verify that the corresponding indicators on the Input Units light. Also, use the Bit/Word Monitor operation in the Programming Device to verify the operation of the corresponding input bits.

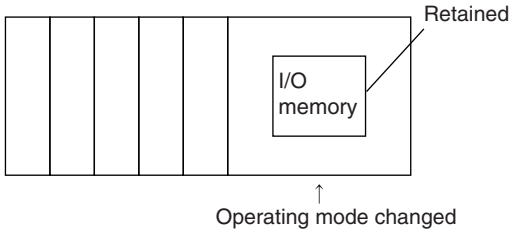


Auxiliary Area Settings

Make any required Auxiliary Area settings, such as the ones shown below. These settings can be made from a Programming Device (including a Programming Console) or instructions in the program.

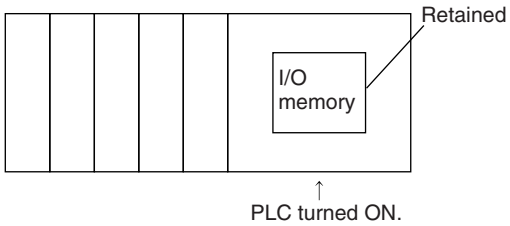
IOM Hold Bit (A50012)

Turning ON the IOM Hold Bit protects the contents of I/O memory (the CIO Area, Work Area, Timer Completion Flags and PVs, Index Registers, and Data Registers) that would otherwise be cleared when the operating mode is switched from PROGRAM mode to RUN/MONITOR mode or vice-versa.



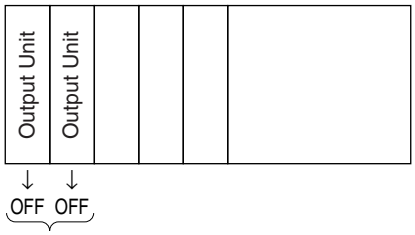
IOM Hold Bit Status at Startup

When the IOM Hold Bit has been turned ON and the PLC Setup is set to protect the status of the IOM Hold Bit at startup (PLC Setup address 80 bit 15 turned ON), the contents of I/O memory that would otherwise be cleared will be retained when the PLC is turned ON.



Output OFF Bit (A50015)

Turning ON the Output OFF Bit causes all outputs on Basic I/O Units and Special I/O Units to be turned OFF. The outputs will be turned OFF regardless of the PLC's operating mode.

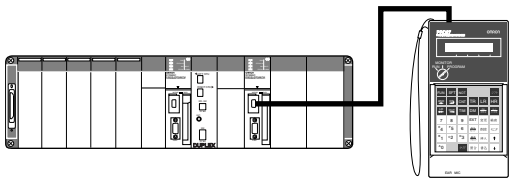


Trial Operation

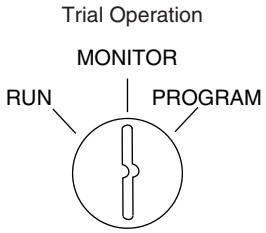
Use the Programming Console or Programming Device (CX-Programmer) to switch the CPU Unit to MONITOR mode.

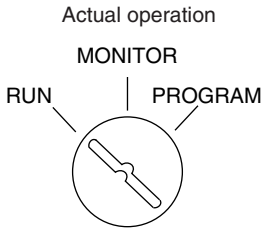
Using a Programming Console

Turn the Mode Switch to MONITOR for the trial operation. (Turn the switch to RUN for full-scale PLC operation.)



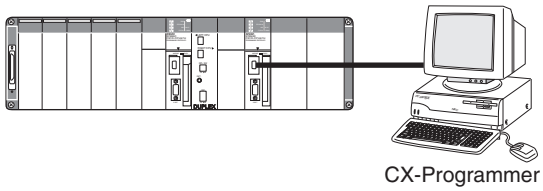
Programming Console





Using the CX-Programmer

The PLC can be put into MONITOR mode with a host computer running CX-Programmer.



CX-Programmer

Trial Operation

Select ***PLC, Mode, MONITOR.***

Actual operation

Select ***PLC, Mode, RUN.***

Monitoring and Debugging

There are several ways to monitor and debug PLC operation, including the force-set and force-reset operations, differentiation monitoring, time chart monitoring, data tracing, and online editing.

Force-Set and Force-Reset

When necessary, the force-set and force-reset operations can be used to force the status of bits and check program execution.

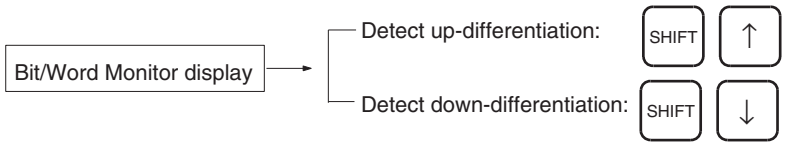
When a Programming Console is being used, monitor the bits with Bit/Word Monitor or 3-word Monitor. Press the SHIFT+SET Keys to force-set a bit or press the SHIFT+RESET Keys to force-reset a bit. The forced status can be cleared by pressing the NOT Key.

CX-Programmer	Programming Console
1. Click the bit to be force-set or force-reset. 2. Select ***Force On*** or ***Off*** from the PLC menu.	Bit/Word Monitor display 3-word Monitor display Force-set: SHIFT SET Force-reset: SHIFT SET Clear: NOT

Differentiation Monitor

The differentiation monitor operation can be used to monitor the up or down differentiation of particular bits.

When a Programming Console is being used, monitor the bit with Bit/Word Monitor. Press the SHIFT+Up Arrow Keys to specify up differentiation or press the SHIFT+Down Arrow Keys to specify down differentiation.

CX-Programmer	Programming Console
1. Click the bit for differential monitoring. 2. Click ***Differential Monitor*** from the PLC Menu. The Differential Monitor Dialog Box will be displayed. 3. Click ***Rising*** or ***Falling.*** 4. Click the **Start** Button. The buzzer will sound when the specified change is detected and the count will be incremented. 5. Click the **Stop** Button. Differential monitoring will stop.	

Time Chart Monitoring

The CX-Programmer's time chart monitor operation can be used to check and debug program execution.

Data Tracing

The CX-Programmer's data trace operation can be used to check and debug program execution.

Online Editing

When a few lines of the program in the CPU Unit have to be modified, they can be edited online with the PLC in MONITOR mode or PROGRAM mode. When more extensive modifications are needed, upload the program from the CPU Unit to the host computer, make the necessary changes, and transfer the edited program back to the CPU Unit.

12. Save and Print the Program

To save the program, select ***File*** and then ***Save*** (or ***Save As***) from the CX-Programmer menus.

To print the program, select ***File*** and then ***Print*** from the CX-Programmer menus.

13. Run the Program

SECTION 5
Installation and Wiring

This section describes how to install a PLC System, including mounting the various Units and wiring the System. Be sure to follow the instructions carefully. Improper installation can cause the PLC to malfunction, resulting in very dangerous situations.

5-1 Fail-safe Circuits

Be sure to set up safety circuits outside of the PLC to prevent dangerous conditions in the event of errors in the PLC or external power supply.

Order of Supplying Power

If the PLC's power supply is turned ON after the controlled system's power supply, outputs in Units such as DC Output Units may malfunction momentarily. To prevent any malfunction, add an external circuit that prevents the power supply to the controlled system from going ON before the power supply to the PLC itself.

Managing PLC Errors

With a Single CPU System or a Duplex CPU System in Simplex Mode, PLC operation will stop and all outputs from Output Units will be turned OFF when any of the following errors occurs.

- Operation of the Power Supply Unit's overcurrent protection circuit
- A CPU error (watchdog timer error) or CPU on standby
- Any of the following fatal errors: Memory error, I/O bus error, duplicate number error, fatal Inner Board error, too many I/O points error, I/O setting error, program error, cycle time overrun error, or FALS(007) error

With a Duplex CPU System in Duplex Mode, PLC operation will stop and all outputs from Output Units will be turned OFF when any of the following errors occurs in the active CPU Unit.

- CPU on standby
- Any of the following fatal errors: I/O bus error, duplicate number error, too many I/O points error, or I/O setting error.

Be sure to add any circuits necessary outside of the PLC to ensure the safety of the system in the event of an error that stops PLC operation.

Note When a fatal error occurs, all outputs from Output Units will be turned OFF even if the IOM Hold Bit has been turned ON to protect the contents of I/O memory. (When the IOM Hold Bit is ON, the outputs will retain their previous status after the PLC has been switched from RUN/MONITOR mode to PROGRAM mode.)

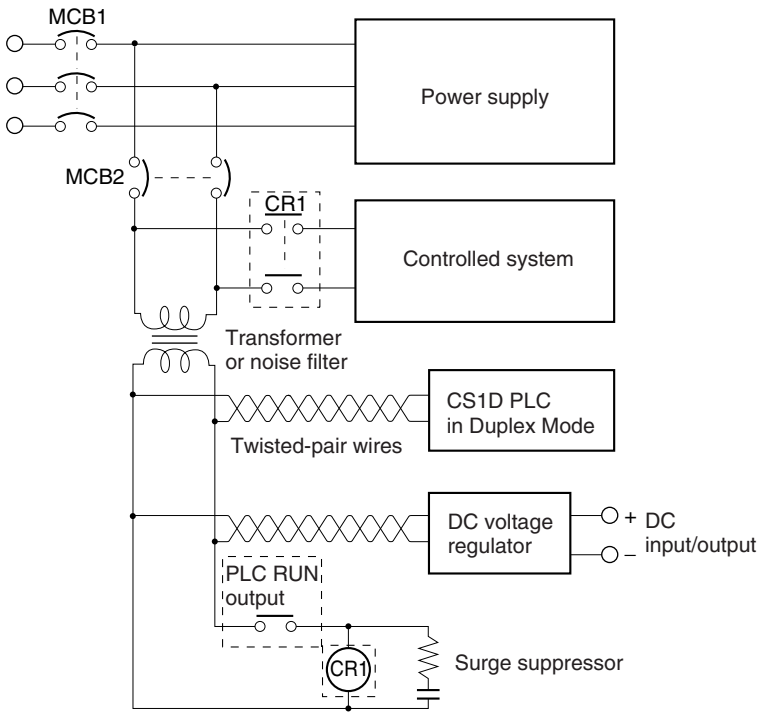
Managing Output Malfunctions

It is possible for an output to remain ON due to a malfunction in the internal circuitry of the Output Unit, such as a relay or transistor malfunction. Be sure to add any circuits necessary outside of the PLC to ensure the safety of the system in the event that an output fails to go OFF.

Emergency Stop Circuit

The following emergency stop circuit controls the power supply to the controlled system so that power is supplied to the controlled system only when the PLC is operating and the RUN output is ON.

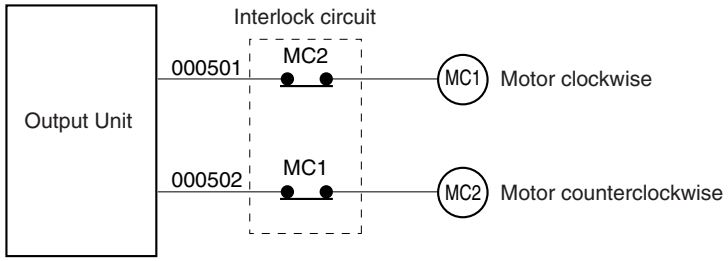
An external relay (CR1) is connected to the RUN output from the Power Supply Unit as shown in the following diagram.



Note Do not latch the RUN output and use it in a circuit to stop a controlled object. Chattering of the relay contacts used in the output may cause incorrect operation.

Interlock Circuits

When the PLC controls an operation such as the clockwise and counterclockwise operation of a motor, provide an external interlock such as the one shown below to prevent both the forward and reverse outputs from turning ON at the same time.



This circuit prevents outputs MC1 and MC2 from both being ON at the same time even if both CIO 000501 and CIO 000502 are both ON, so the motor is protected even if the PLC is programmed improperly or malfunctions.

5-2 Installation

5-2-1 Installation and Wiring Precautions

Be sure to consider the following factors when installing and wiring the PLC to improve the reliability of the system and make the most of the PLC's functions.

Ambient Conditions

Do not install the PLC in any of the following locations.

- Locations subject to ambient temperatures lower than 0°C or higher than 55°C.
- Locations subject to drastic temperature changes or condensation.
- Locations subject to ambient humidity lower than 10% or higher than 90%.
- Locations subject to corrosive or flammable gases.
- Locations subject to excessive dust, salt, or metal filings.
- Locations that would subject the PLC to direct shock or vibration.
- Locations exposed to direct sunlight.
- Locations that would subject the PLC to water, oil, or chemical reagents.

Be sure to enclose or protect the PLC sufficiently in the following locations.

- Locations subject to static electricity or other forms of noise.
- Locations subject to strong electromagnetic fields.
- Locations subject to possible exposure to radioactivity.
- Locations close to power lines.

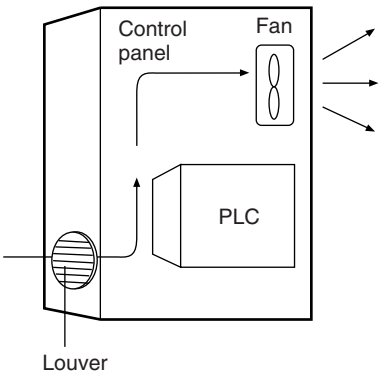
Installation in Cabinets or Control Panels

When the PLC is being installed in a cabinet or control panel, be sure to provide proper ambient conditions as well as access for operation and maintenance.

Temperature Control

The ambient temperature within the enclosure must be within the operating range of 0°C to 55°C. When necessary, take the following steps to maintain the proper temperature.

- Provide enough space for good air flow.
- Do not install the PLC above equipment that generates a large amount of heat such as heaters, transformers, or high-capacity resistors.
- If the ambient temperature exceeds 55°C, install a cooling fan or air conditioner.



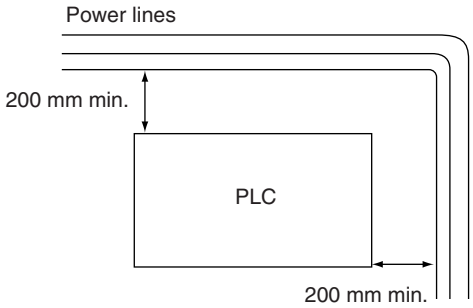
- If a Programming Console will be left on the PLC, the ambient temperature must be within the Programming Console's operating range of 0°C to 45°C.

Accessibility for Operation and Maintenance

- To ensure safe access for operation and maintenance, separate the PLC as much as possible from high-voltage equipment and moving machinery.
- The PLC will be easiest to install and operate if it is mounted at a height of about 1.0 to 1.6 m.

Improving Noise Resistance

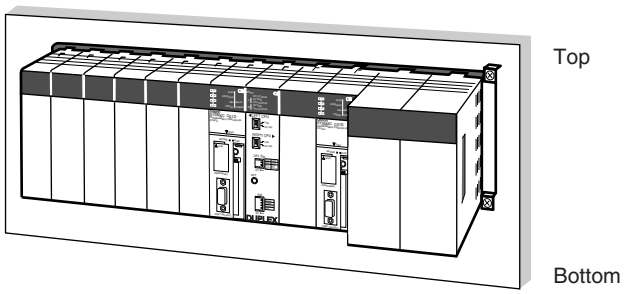
- Do not mount the PLC in a control panel containing high-voltage equipment.
- Install the PLC at least 200 mm (6.5 feet) from power lines.



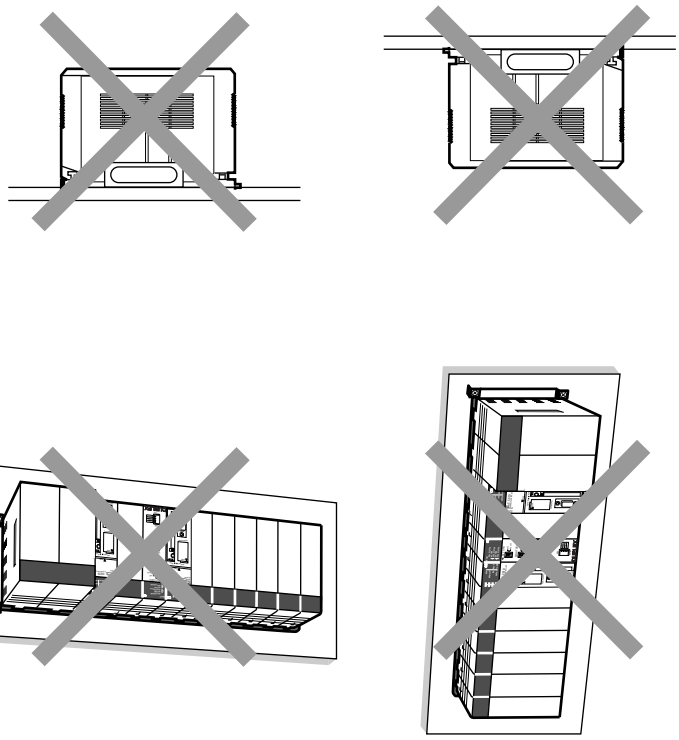
- Ground the mounting plate between the PLC and the mounting surface.
- When I/O Connecting Cables are 10 m or longer, connect the control panels in which Racks are mounted with heavier power wires (3 wires at least 2 mm^2 in cross-sectional area).

PLC Orientation

- Each Rack must be mounted in an upright position to provide proper cooling.



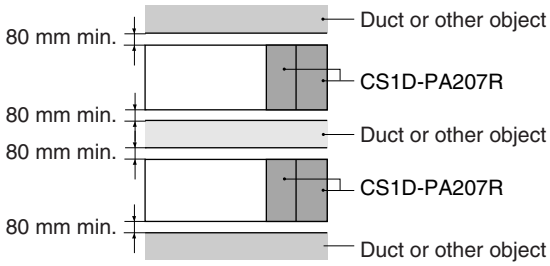
- Do not install a Rack in any of the following positions.



5-2-2 Installation in a Control Panel

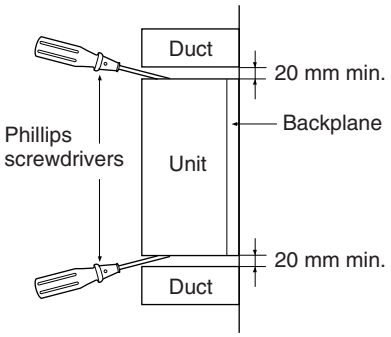
- A typical installation is a CPU Rack mounted above an Expansion Rack on a mounting plate in the control panel.
- The spacing between the CPU Rack and Expansion Rack (or between two Expansion Racks) should be sufficient to allow space for a wiring duct, wiring, air circulation, and replacement of Units in the Racks.

Note If the CS1D-PA207R Power Supply Unit is to be used at an ambient temperature of 50°C or higher, provide a minimum space of 80 mm between the top of the Unit and any other objects, e.g., ceiling, wiring ducts, structural supports, devices, etc.



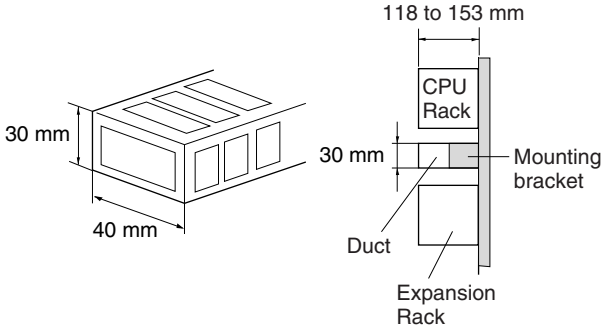
- Up to 7 Expansion Racks can be connected.
  Each I/O Connecting Cable can be up to 12 m long, but the sum total of all cables between the CPU Rack and Expansion Racks must be 12 m or less.
- The mounting plate should be grounded completely and we recommend using a mounting plate that has been plated with a good conductor to improve noise resistance.
- If all of the Racks cannot be mounted to the same mounting plate, the individual plates should be securely connected together using 3 wires of at least 2 mm^2 in cross-sectional area.

- The Backplanes are mounted to the plate(s) with four M4 screws each.
- Whenever possible, route I/O wiring through wiring ducts or raceways. Install the duct so that it is easy to fish wire from the I/O Units through the duct. It is handy to have the duct at the same height as the Racks.



Wiring Ducts

The following example shows the proper installation of wiring duct.

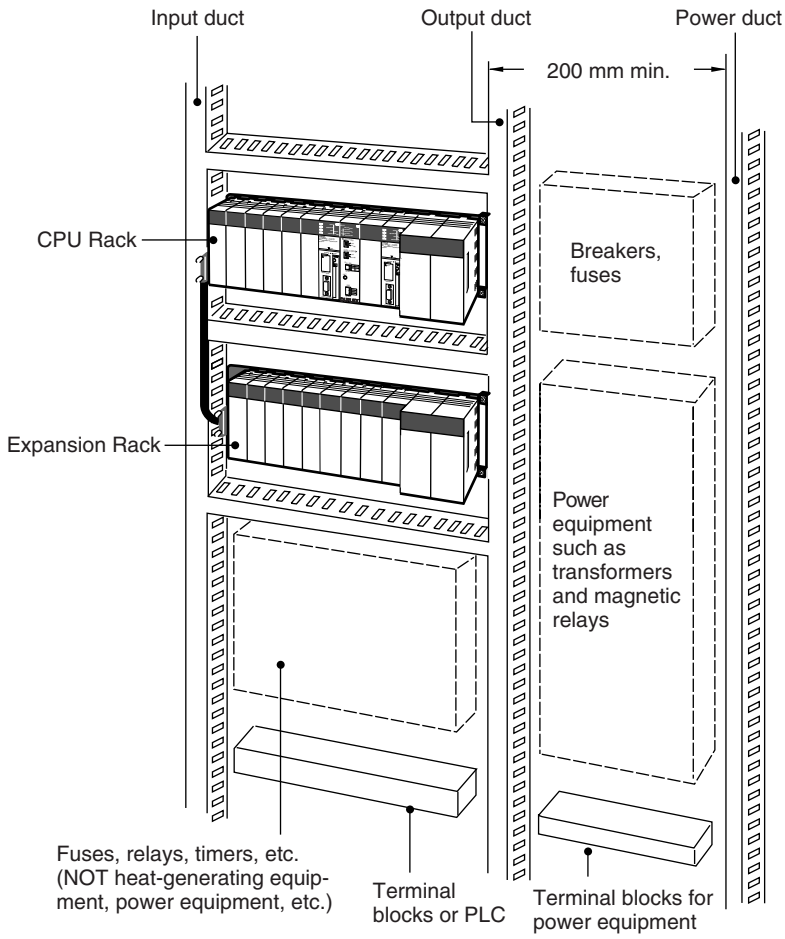


Note Tighten the Unit mounting screws, PLC Rack mounting screws, terminal block screws, and cable screws to the following torques.

Screws	Unit/screw size	Torque
Unit mounting screws	CPU Units	0.9 N·m
	Power Supply Units	0.9 N·m
	Duplex Unit	0.4 N·m
	I/O Units	0.4 N·m
Backplane mounting screws		0.9 N·m
Terminal screws	M3.5	0.8 N·m
	M3	0.5 N·m
Cable connector screws	M2.6	0.2 N·m

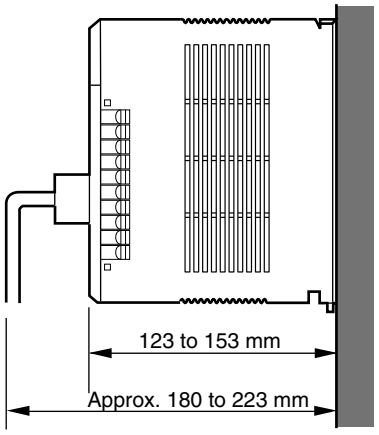
Routing Wiring Ducts

Install the wiring ducts at least 20 mm between the tops of the Racks and any other objects, (e.g., ceiling, wiring ducts, structural supports, devices, etc.) to provide enough space for air circulation and replacement of Units. If the ambient temperature is 50 °C or higher, provide a minimum space of 80 mm.

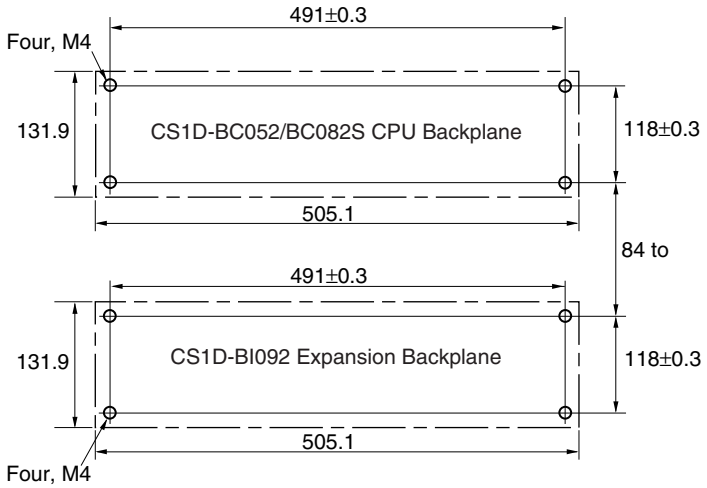


5-2-3 Mounting Height

The mounting height of CPU Racks and Expansion Racks is 123 to 153 mm, depending on I/O Units mounted. If Programming Devices or connecting cables are attached, the additional dimensions must be taken into account. Allow sufficient clearance in the control panel in which the PLC is mounted.



5-2-4 Backplane Mounting Dimensions

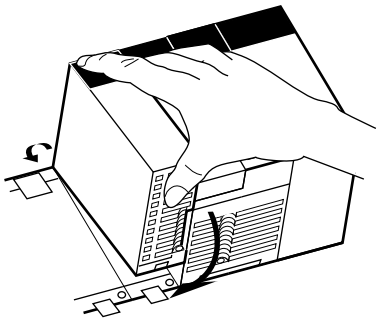


5-2-5 Mounting Units to the Backplane

The following table shows the mounting method.

Installation method	Removal method
Hook the top of the Unit into the slot on the Backplane and tighten the screw on the bottom of Unit.	Loosen the screw on the bottom of the Unit and rotate the Unit upward.

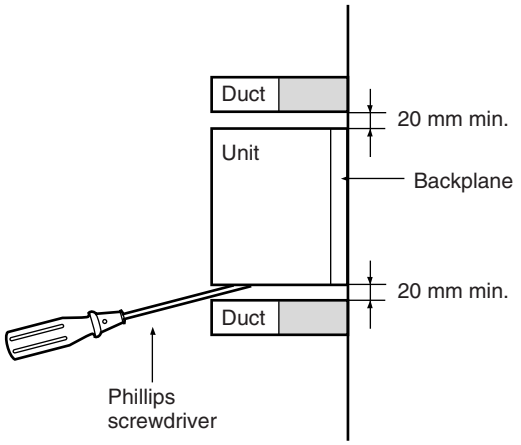
1,2,3... 1. Mount the Unit to the Backplane by hooking the top of the Unit into the slot on the Backplane and rotating the I/O Unit downwards.

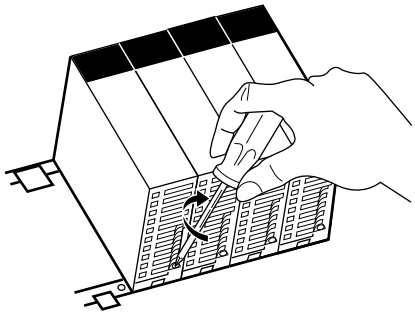


2. Make sure that the connector on the back of the Unit is properly inserted into the connector in the Backplane.
3. Use a Phillips-head screwdriver to tighten the screw on the bottom of Unit. The screwdriver must be held at a slight angle, so be sure to leave enough space below each Rack.

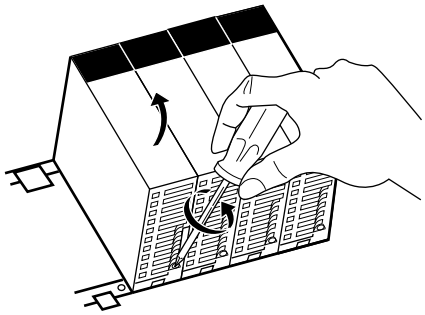
Note The screws at the bottoms of the Units must be tightened to the following torques.

CPU Units:	0.9 N·m
Power Supply Units:	0.9 N·m
Duplex Unit:	0.4 N·m
I/O Units:	0.4 N·m





4. To remove a Unit, use a phillips-head screwdriver to loosen the screw at the bottom of the Unit, rotate the Unit upward, and remove it.



5-2-6 I/O Connecting Cables

I/O Connecting Cables are used to connect the CPU Rack and Expansion Racks. There are two types of I/O Connecting Cables.

Type	Model number	Connectors		Usage
		CPU Rack	Expansion Rack	
CS-series I/O Connecting Cables	CS1D-CN□□3	Simple lock connector	Simple lock connector	CPU Rack → Expansion Rack
				Expansion Rack → Expansion Rack
CV-series Long-distance Expansion Rack I/O Connecting Cables	CV500-CN□□2	Simple lock connector		CPU Rack or Expansion Rack → Long-distance Expansion Rack

Model Numbers

CS-series I/O Connecting Cables

Model number	Cable length
CS1W-CN313 (See note.)	0.3 m
CS1W-CN713 (See note.)	0.7 m
CS1W-CN223	2 m
CS1W-CN323	3 m
CS1W-CN523	5 m
CS1W-CN133	10 m
CS1W-CN133B2	12 m

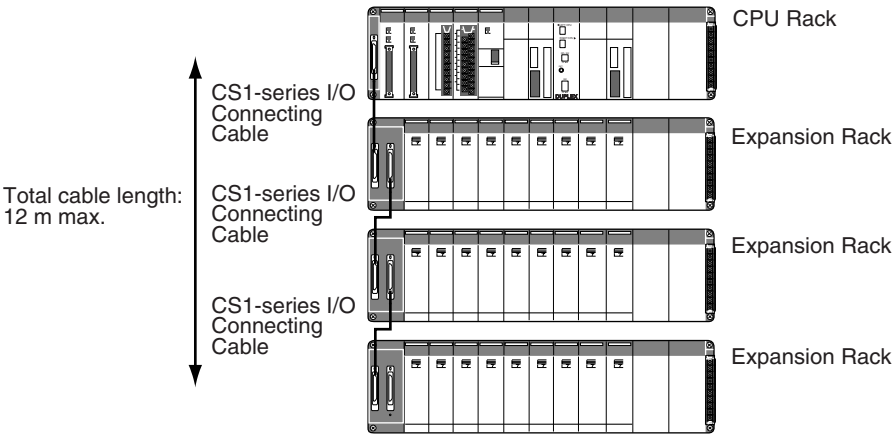
Note Not all CS1W-CN313/CN713 Cables can be used. Refer to *CS-series Connecting Cables* on page 45 for details.

Long-distance Expansion Rack I/O Connecting Cables

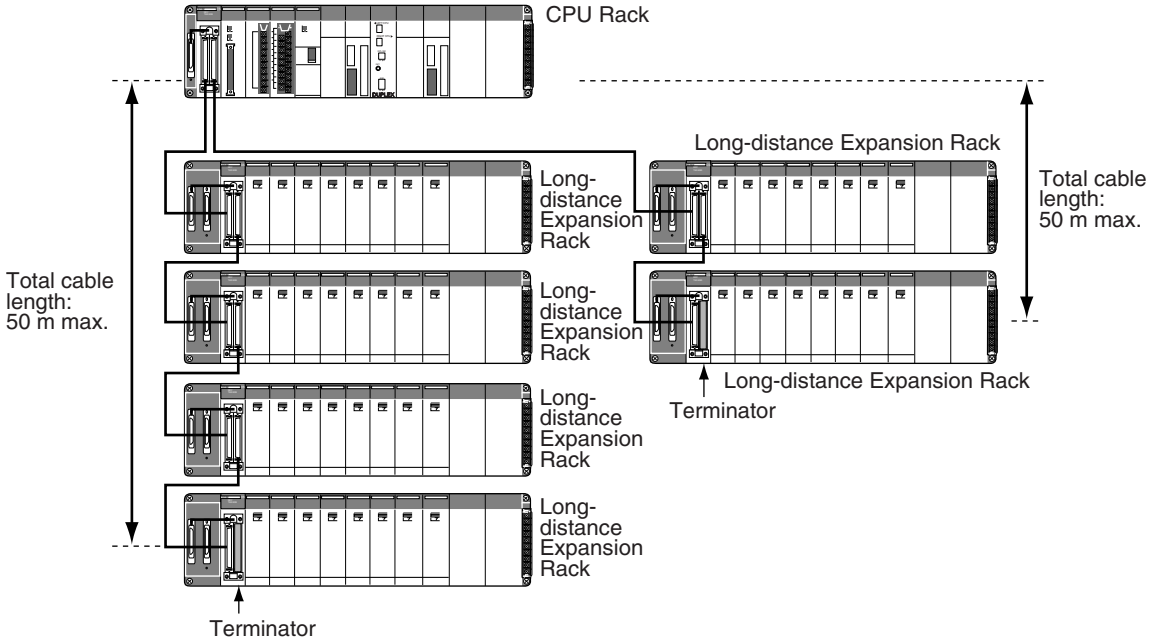
Model number	Cable length
CV500-CN312	0.3 m
CV500-CN612	0.6 m
CV500-CN122	1 m
CV500-CN222	2 m
CV500-CN322	3 m
CV500-CN522	5 m
CV500-CN132	10 m
CV500-CN232	20 m
CV500-CN332	30 m
CV500-CN432	40 m
CV500-CN532	50 m

- When connecting Expansion Racks with CS-series I/O Connecting Cables, install the Racks and select I/O Connecting Cables so that the total length of all I/O Connecting Cables does not exceed 12 m.
- When connecting Expansion Racks with Long-distance Expansion Rack I/O Connecting Cables, install the Racks and select I/O Connecting Cables so that the total length of all I/O Connecting Cables in one system does not exceed 50 m.

Example 1: CS-series I/O Connecting Cables



Example 2: Long-distance Expansion Rack I/O Connecting Cables



Note

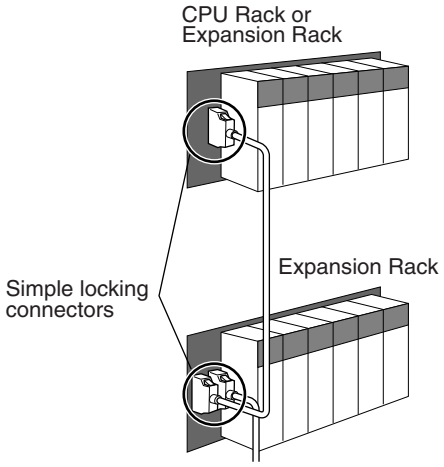
1. Up to two series of Long-distance Expansion Racks can be connected.
2. A maximum of seven Long-distance Expansion Racks can be connected (including all Racks in both series).
3. Each series of Long-distance Expansion Racks must be 50 m max. with a total of 100 m max. for both series.
4. Expansion Racks and Long-distance Expansion Racks cannot be connected at the same time.
5. In a Duplex CPU, Dual I/O Expansion System, use only the CS1D-BC042D CPU Backplane and CS1D-BIO082D Expansion Backplanes. No other Backplanes can be used.
6. In a Duplex CPU, Single I/O Expansion System, use only the CS1D-BC052 CPU Backplane and CS1D-BIO092 Expansion Backplanes. No other Backplanes can be used.
7. In a CS1D Single CPU System, use only the CS1D-BC082S CPU Backplane and CS1D-BIO092 Expansion Backplanes. No other Backplanes can be used.

Connecting Cables

There are two connection methods that are used, depending on the type of cable.

CS-series I/O Connecting Cables

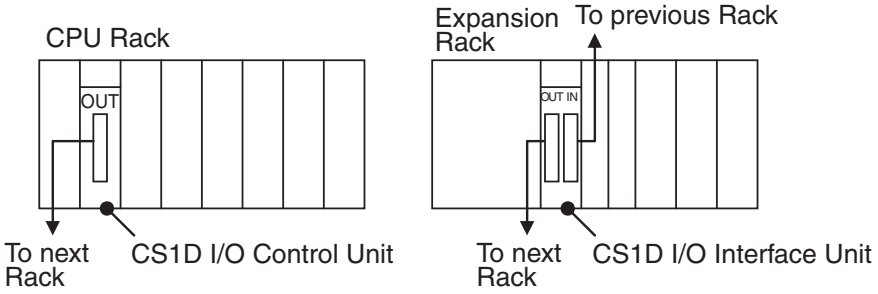
With CS-series I/O Connecting Cables, simple locking connectors are used on both the CPU Rack and Expansion Racks.



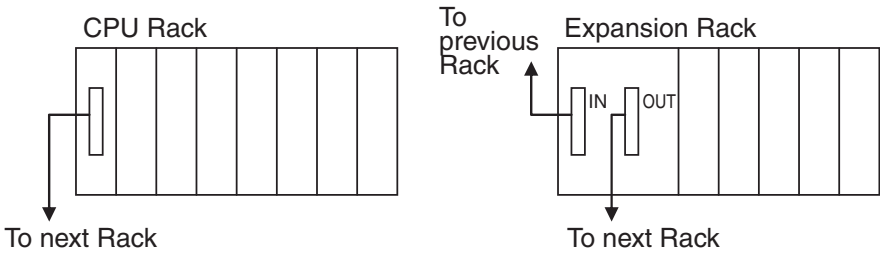
The connectors can be inserted only one way; they cannot be inserted upside down. Be sure that the connectors fit properly as they are inserted.

The connecting port for each CS-series I/O Connecting Cable depends on the system configuration and the Rack being connected, as shown in the following diagrams. The PLC will not operate properly if the Racks are not connected as shown in the following diagrams.

Duplex CPU, Dual I/O Expansion System

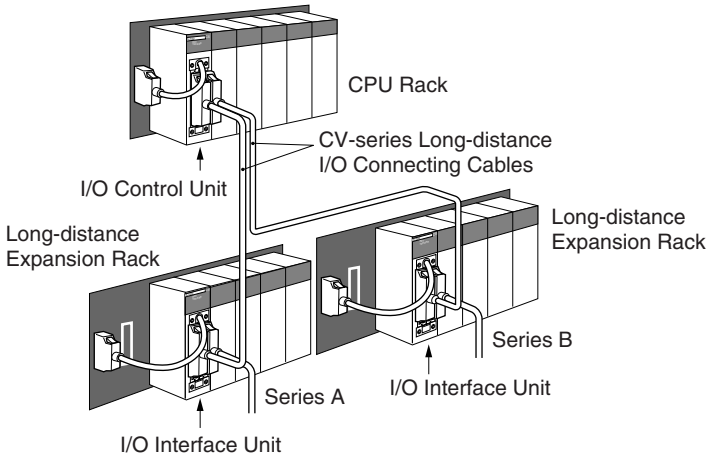


Duplex CPU, Single I/O Expansion System



CV-series Long-distance I/O Connecting Cables: Connecting Long-distance Expansion Racks

The following connections are used when an I/O Control Unit is mounted to the CPU Rack. With the CS1D PLCs, an I/O Control Unit cannot be mounted to an Expansion Rack.

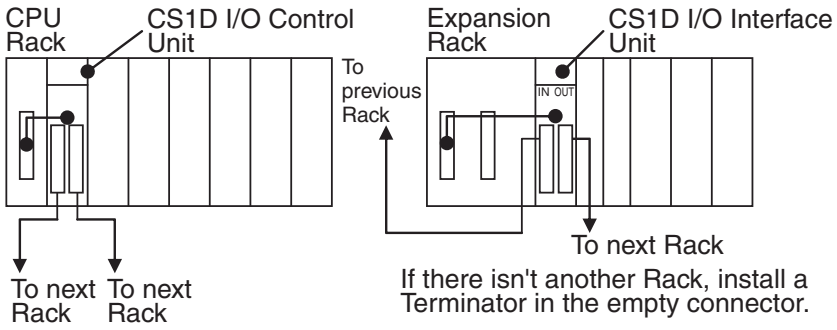


The connecting port for each CV-series Long-distance I/O Connecting Cable depends on the system configuration and the Rack being connected, as shown in the following diagrams. The PLC will not operate properly if the Racks are not connected as shown in the following diagrams.

Duplex CPU, Dual I/O Expansion System

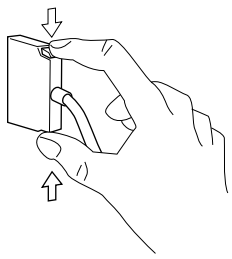
Long-distance Expansion Racks cannot be connected.

Duplex CPU, Single I/O Expansion System



Connecting the Simple Locking Connectors

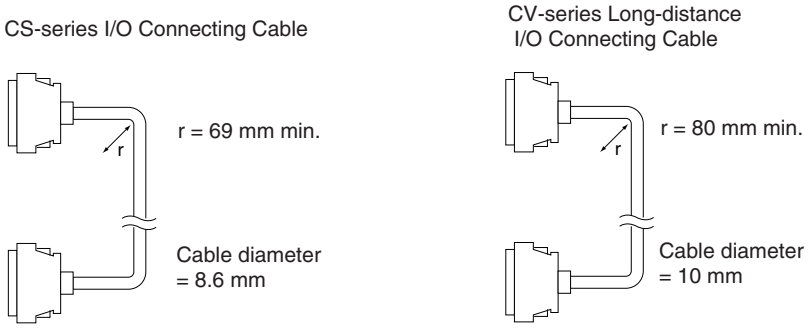
Press the tabs on the end of the connector and insert the connector until it locks in place. The PLC will not operate properly if the connector isn't inserted completely. To remove the connector, press the tabs and then pull the connector out.



Note

1. Do not route the I/O Connecting Cables through ducts that contain the I/O or power wiring.
2. Always turn OFF the power supply to the PLC before connecting Cables.
3. An I/O bus error will occur and the PLC will stop if an I/O Connecting Cable's connector separates from the Rack. Be sure that the connectors are secure.

4. A 75-mm hole will be required if the I/O Connecting Cable must pass through a hole when connecting a Long-distance Expansion Rack and a 63-mm hole will be required for Cables connecting other Racks.
5. I/O Connecting Cables cannot be cut or rejoined. Be sure to use I/O Connecting Cables of the proper length, particularly when wiring inside panels or wiring ducts.
6. Do not pull on the I/O Connecting Cables with excessive force.
7. The I/O Connecting Cables mustn't be bent too severely. The minimum bending radii are shown in the following diagram.

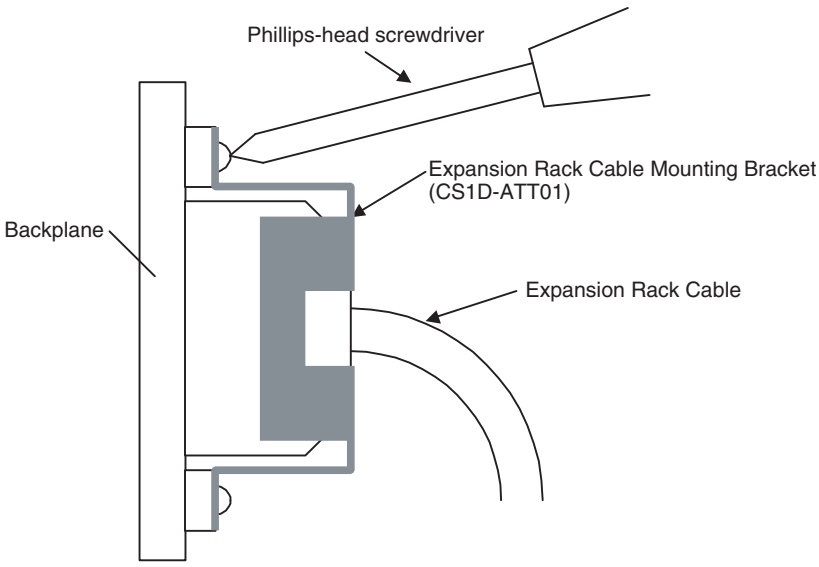


Installing the Expansion Rack Cable Mounting Bracket

Expansion Rack Cable Mounting Brackets can be used to prevent the Expansion Cables from being disconnected unintentionally.

Note The Expansion Rack Cable Mounting Bracket is an accessory, which is sold separately from the Connecting Cables and Backplanes.

1,2,3... 1. Connect the Cable as described in *5-2-6 I/O Connecting Cables*.
2. Put on the Expansion Rack Cable Mounting Bracket from above and attach it at the top and bottom with the provided Phillips-head screws.



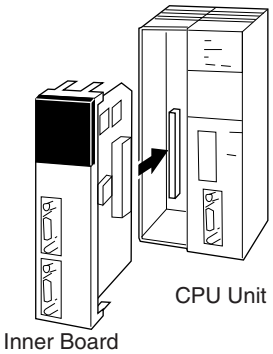
5-2-7 Inner Board Installation

An Inner Board can be mounted only to CPU Units for Single CPU Systems. You cannot mount one to CPU Units for Duplex CPU Systems. The only Inner Boards that can be used for Duplex CPU Systems is the CS1D-LCP05D built

into the CS1D-CPU□□PProcess-control CPU Units. The CS1D-CPU□□P Process-control CPU Units are sold as a single product and the Board cannot be removed.

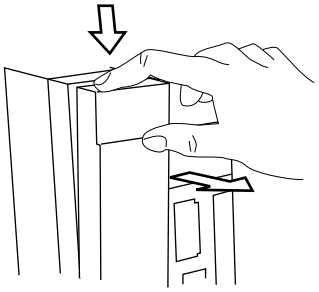
Note

1. Duplex operation that includes Inner Boards can be used with CPU Units from lot number 030422 onwards (i.e., CPU Units manufactured from April 22, 2003 onwards).
2. Always turn the power OFF before installing or removing the Inner Board. Installing or removing the Inner Board with the power turned ON can cause the CPU Unit to malfunction, damage internal components, or cause communications errors.
3. Before installing the Inner Board, be sure to first touch a grounded metallic object, such as a metal water pipe, in order to discharge any static build-up from your body.

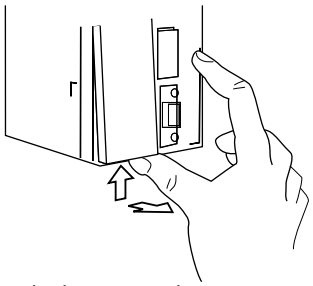


1,2,3...

1. Press the catches at the top and bottom of the Inner Board compartment cover and pull the cover forward.

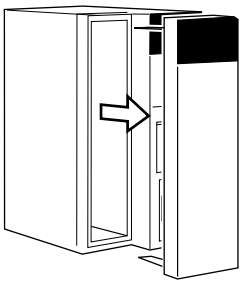


Press the top catch.

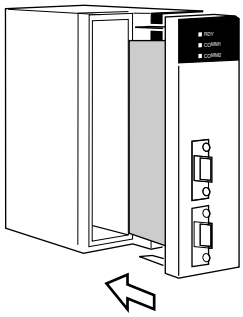


Press the bottom catch.

2. Remove the Inner Board compartment cover.



3. Align the Inner Board with the groove and slide it into the compartment.

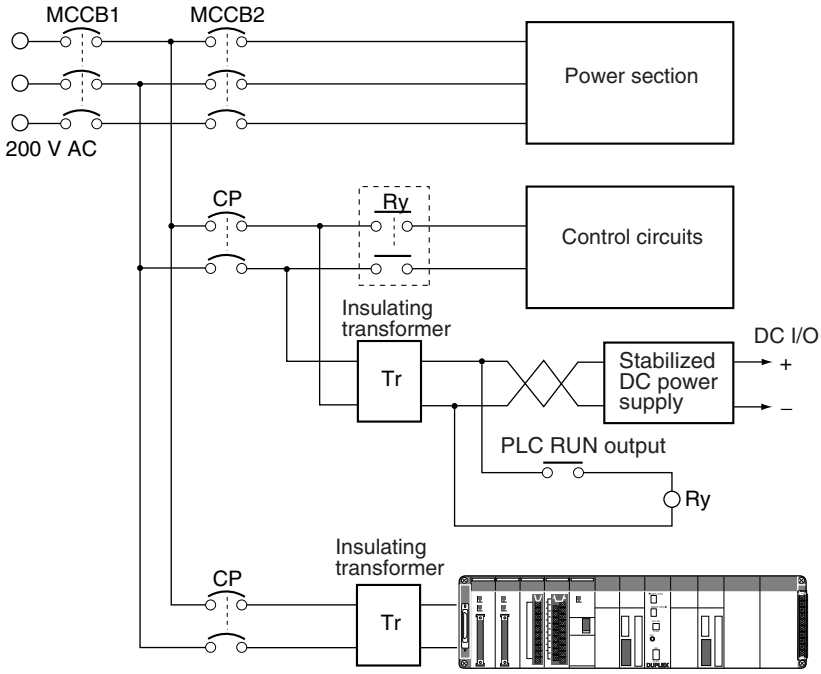


5-3 Power Supply Wiring

The power supply systems are divided as follows: Power section, control circuits, CS1D Racks, and DC I/O. Wire each of these separately.

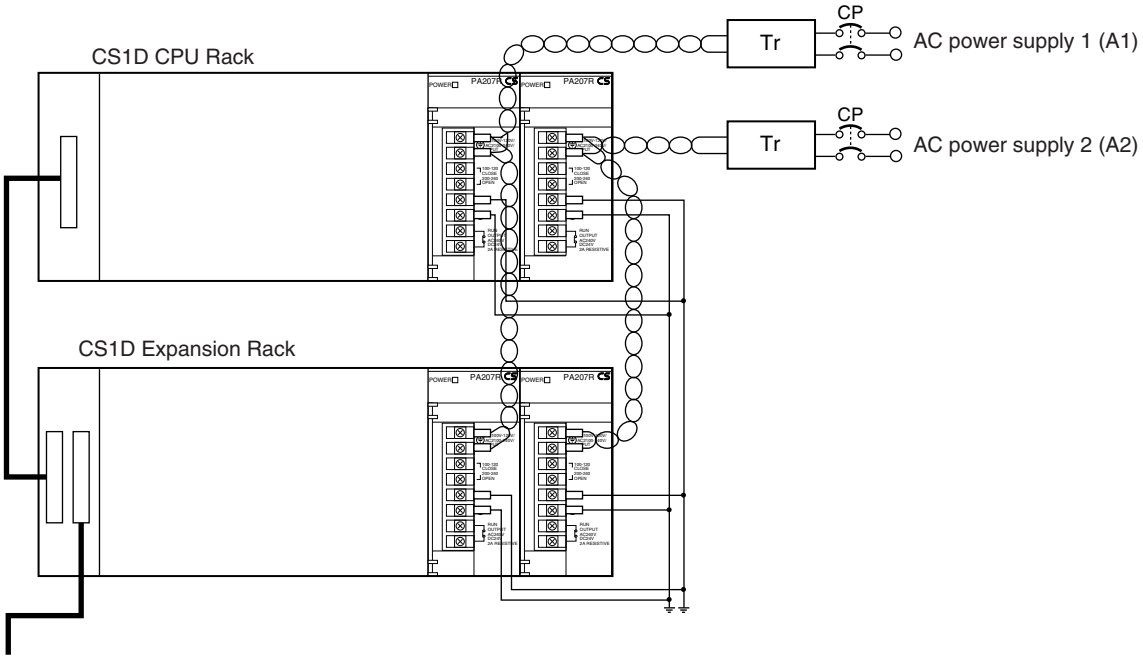
When using a duplex CS1D System, use a separate power source for each of the two Duplex Power Supply Units.

Provide an emergency stop circuit to control the power supply to the controlled system so that power is supplied to the controlled system only when the PLC is operating and the RUN output is ON. Connect an external relay to the RUN output from the Power Supply Unit.



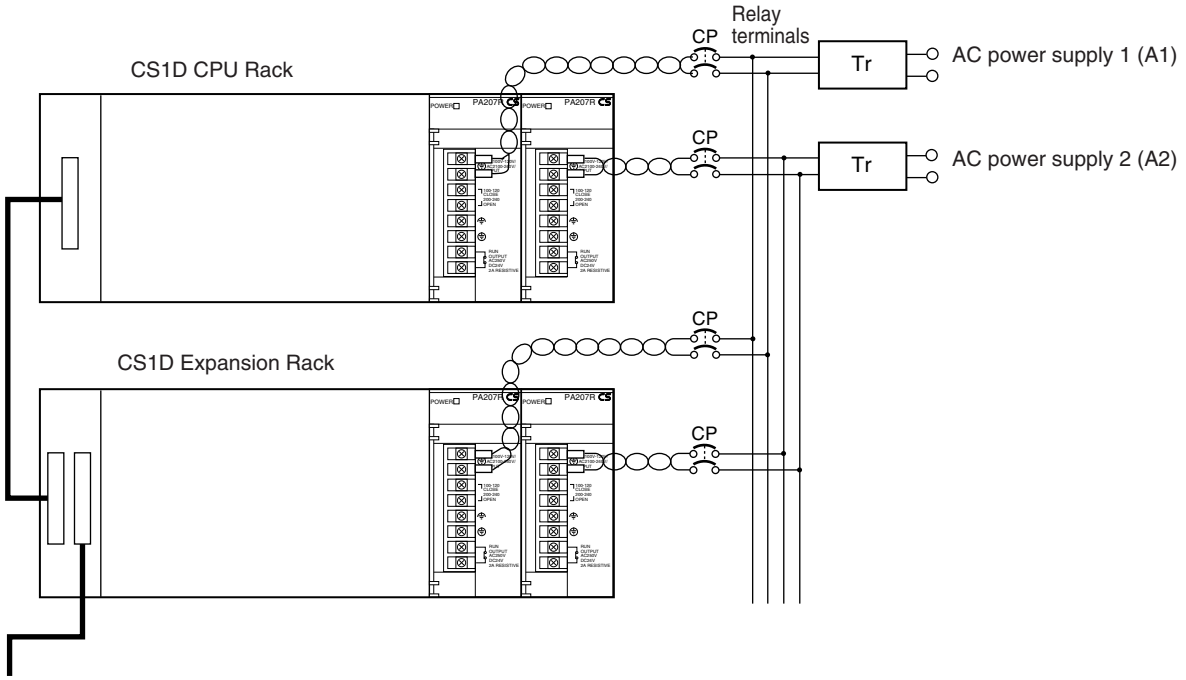
The Duplex CPU and Expansion Backplanes for a CS1D PLC support Duplex Power Supply Units. If anything happens to interrupt the power supply from one of the Power Supply Units, the other one will continue supplying power to the Unit on the Rack. To ensure that the PLC will continue operating even if the power supply to the Power Supply Unit is interrupts, always provide power to two Duplex Power Supply Units from different power sources.

Wiring Examples: Expansion Racks



Note

1. Wire the Power Supply Units so that they can be replaced safely and without interrupt the power supply to other Racks or devices in the event that a Power Supply Unit fails.
2. Branching wiring at a Power Supply Unit terminal block will create a dangerous situation if a Unit must be replaced. Use relay terminals to branch wiring and provide a circuit protector (CP) for each Power Supply Unit.

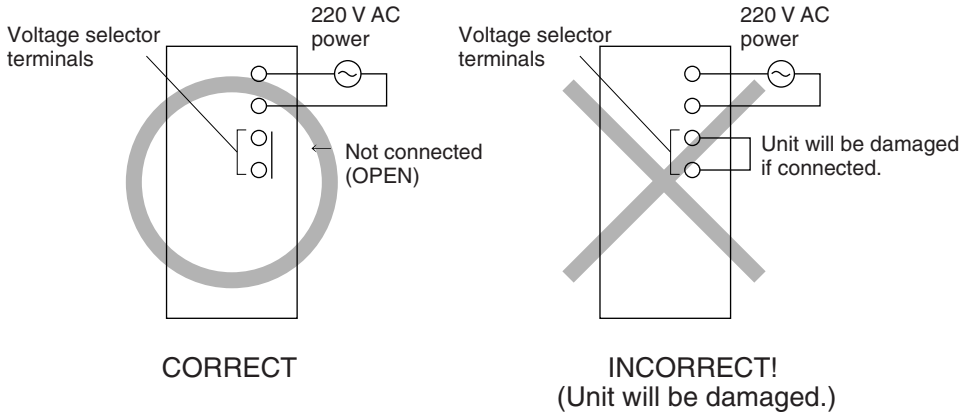


5-4 Wiring Methods

5-4-1 Wiring Power Supply Units

AC Power Supply Models

Note When 220 V AC power (200 to 240 V AC) is being supplied, be sure to remove the jumper bar that shorts the voltage selector terminals. The Unit will be damaged if 220 V AC is supplied with the jumper bar connected.

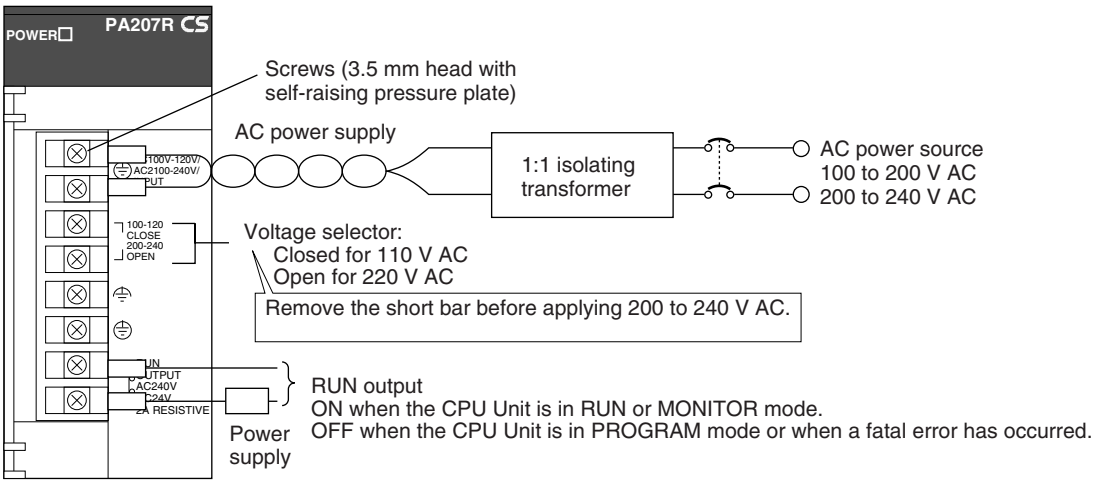


CORRECT

INCORRECT!
(Unit will be damaged.)

Note If 100 to 120 V AC power is supplied but the jumper bar has been removed to select 200 to 220 V AC, the Unit will not operate because the power supply voltage will be below the 85% minimum level.

- Cover the Unit while wiring to prevent wire clippings from entering the Unit. If there is a dustproof label on the top of the Unit, do not remote it before you wire the Unit. (Remove the label or other covering after wiring has been completed to allow air circulation needed for cooling.)



Note The RUN output can be used from either the Power Supply Units on the CPU Rack or the Expansion Racks.

To obtain an output contact equivalent to RUN output when using a Power Supply Unit without RUN output, use an output contact from the Power Supply Unit with a constant ON flag as the input condition.

AC Power Source

- Supply 100 to 120 V AC or 200 to 240 V AC.
- Keep voltage fluctuations within the specified range:

Supply voltage	Allowable voltage fluctuations
100 to 120 V AC	85 to 132 V AC
200 to 240 V AC	170 to 264 V AC

- If one power supply phase of the equipment is grounded, connect the grounded phase side to the L2/N (or L1/N if so indicated) terminal.

Voltage Selector

Shorted: 100 to 120 V AC
Open: 200 to 240 V AC

Short-circuit the voltage selector terminals with the jumper bar to select 100 to 120 V AC supply voltage. For 200 to 240 V AC leave them open.

⚠ **Caution** The Power Supply Unit will be damaged if 200 to 240 V AC power is supplied and the voltage selector terminals are connected with the jumper bar.

Isolating Transformer

The PLC's internal noise isolation circuits are sufficient to control typical noise in power supply lines, but noise between the PLC and ground can be significantly reduced by connecting a 1-to-1 isolating transformer. Do not ground the secondary coil of the transformer.

Power Consumption

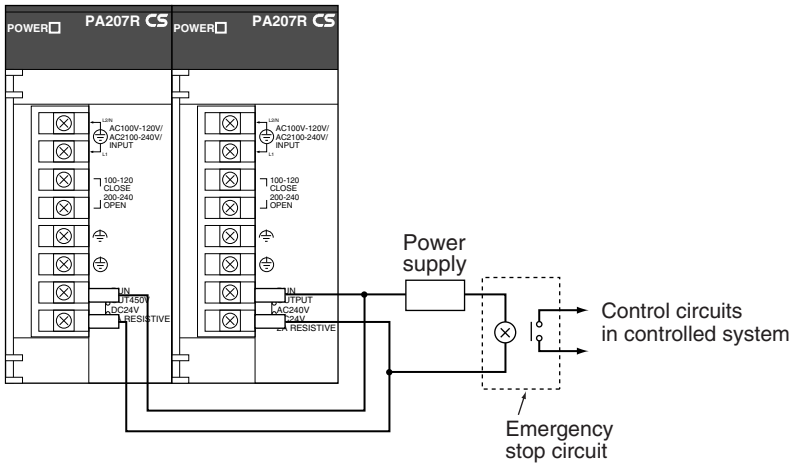
The power consumption will be 150 VA max. per Rack, but there will be a surge current determined by power supply specifications when power is turned ON.

RUN Output

This output is ON whenever the CPU Unit is operating in RUN or MONITOR mode; it is OFF when the CPU Unit is in PROGRAM mode or a fatal error has occurred.
The RUN output can be used to control external systems, such as in an emergency stop circuit that turns OFF the power supply to external systems when the PLC is not operating. (See *5-1 Fail-safe Circuits* for more details on the emergency stop circuit.)

CS1D-PA207R	
Contact form	SPST-NO
Maximum switching capacity	240 V AC: 2 A for resistive loads 120 V AC: 0.5 A for inductive loads 24 V DC: 2 A for resistive loads 2 A for inductive loads

Wiring Example: RUN Output



Wiring

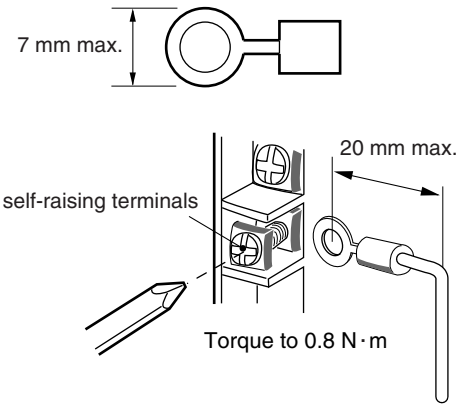
Terminal screws	M3.5 self-rising screws
Recommended wire size	AWG 20 to 14 (0.517 to 2.08 mm^2)
Recommended tightening torque	0.8 N·m

Recommended crimp terminals

Manufacturer	Models	Shape	Applicable wire range (stranded wire)
JST Mfg.	V1.25-YS3A	Y-shaped terminal with sleeve	0.25 to 1.65 mm^2 (AWG 22 to 16)
	V1.25-M3(RAV1.25-3.5)	Round terminal with sleeve	
	V2-YS3A	Y-shaped terminal with sleeve	1.04 to 2.63 mm^2 (AWG 16 to 14)
	V2-M3(RAV2-3.5)	Round terminal with sleeve	

Note

1. Use crimp terminals for wiring.
2. Do not connect bare stranded wires directly to terminals.



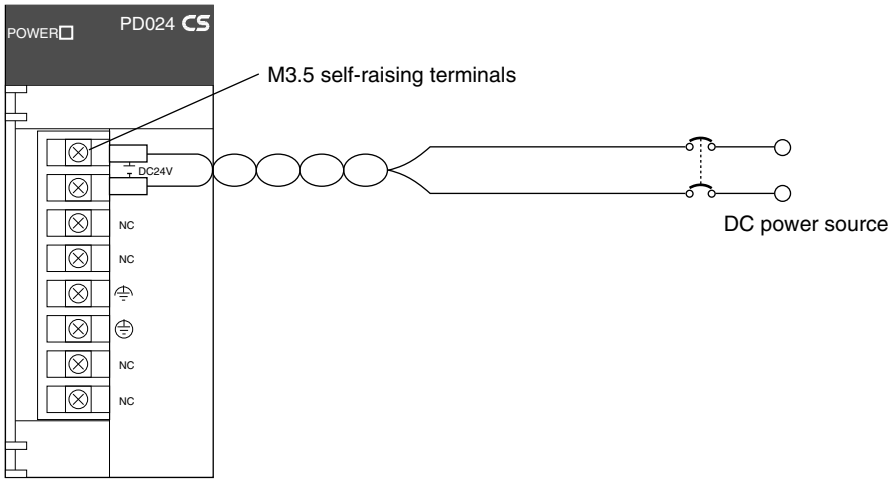
⚠ **Caution** Tighten the AC power supply terminal block screws to the torque of 0.8 N·m. Loose screws may result in short-circuit, malfunction, or fire.

Note
1. Be sure to check the setting of the voltage selector before supplying power.
2. Always remove any dustproof labels that are on the top of the Units when they are shipped before you tum ON the power supply. If the labels are not removed, heat will accumulate and malfunctions may occur.

DC Power Supply Models

Note Cover the Unit while wiring to prevent wire clippings from entering the Unit. If there is a dustproof label on the top of the Unit, do not remote it before you wire the Unit. (Remove the label or other covering after wiring has been completed to allow air circulation needed for cooling.)

CS1D-PD024/025 Power Supply Unit



DC Power Source

Supply 24 V DC. Keep voltage fluctuations within the specified range (19.2 to 28.8 V DC).

Power Supply Capacity

The maximum power consumption is 40 W per Rack for the CS1D-PD024 and 60 W per Rack for the CS1D-PD025, but there will be a surge current determined by power supply specifications when the power is turned ON.

Wiring

Terminal screws	M3.5 self-rising screws
Recommended wire size	AWG 20 to 14 (0.517 to 2.08 mm^2)
Recommended tightening torque	0.8 N·m

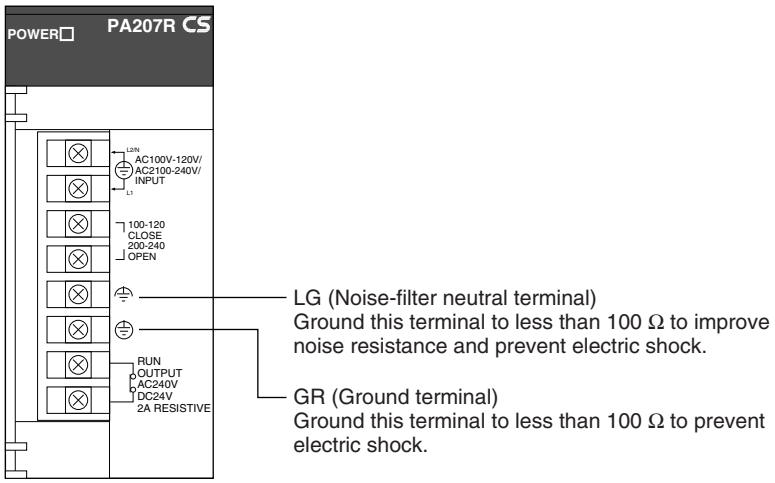
Recommended crimp terminals

Manufacturer	Models	Shape	Applicable wire range (stranded wire)
JST Mfg.	V1.25-YS3A	Y-shaped terminal with sleeve	0.25 to 1.65 mm^2 (AWG 22 to 16)
	V1.25-M3(RAV1.25-3.5)	Round terminal with sleeve	
	V2-YS3A	Y-shaped terminal with sleeve	1.04 to 2.63 mm^2 (AWG 16 to 14)
	V2-M3(RAV2-3.5)	Round terminal with sleeve	

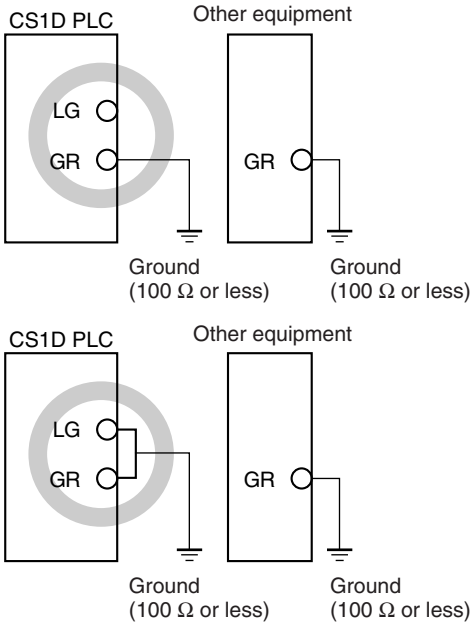
Note

1. Use crimp terminals for wiring.
2. Do not connect bare stranded wires directly to terminals.
3. Be sure not to reverse the positive and negative leads when wiring the power supply terminals.
   Supply power to all of the Power Supply Units from the same source.
4. To allow heat to dissipate, always remove any dustproof labels that are on the top of the Units before you turn ON the power supply.

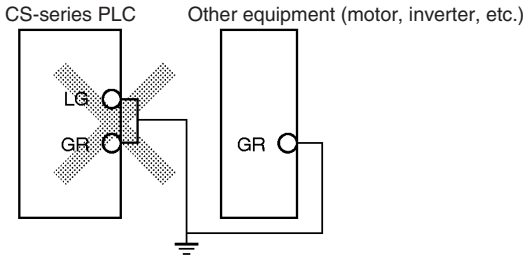
Grounding



- To help prevent electrical shock, ground the ground terminal (GR: ⏚) with a ground resistance of less than 100 Ω using a 14-gauge wire (minimum cross-sectional area of 2 mm^2).
- The line ground terminal (LG: ⏚) is a noise-filtered neutral terminal. If noise is a significant source of errors or electrical shocks are a problem, connect the line ground terminal to the ground terminal and ground both with a ground resistance of less than 100 Ω.
- To prevent electrical shock, always ground the LG-GR terminals to a ground resistance of less than 100 Ω if these are connected to each other.
- The ground wire should not be more than 20 m long.
- Using the same ground line is used together with other equipment, such as motors and inverters, or connecting the ground line to structural parts of buildings may actually increase noise and may have a negative affect on operation.



- Do not share the PLC's ground with other equipment or ground the PLC to the metal structure of a building. The configuration shown in the following diagram may worsen operation.

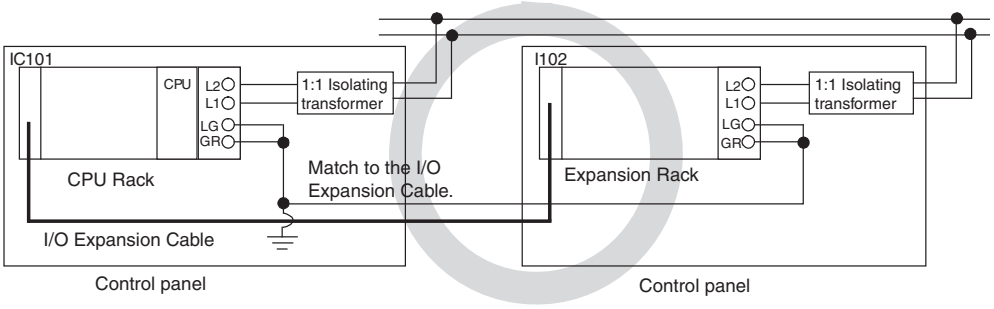


Grounding Long-distance Expansion Racks

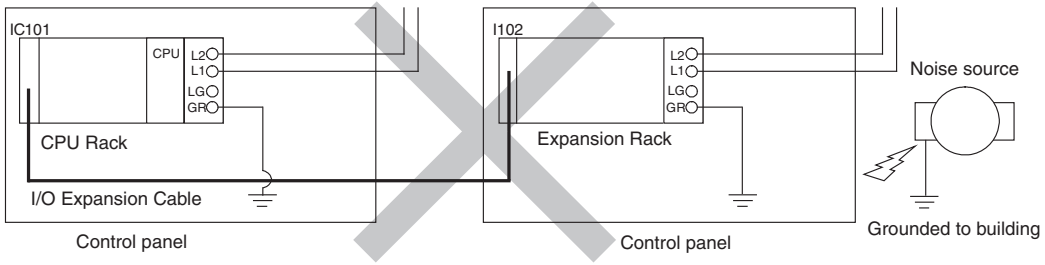
A difference in potential will occur between remote ground points if more than one point is grounded on the CPU Rack and Long-distance Expansion Racks in a CS1 Long-distance Expansion System. This is caused by high-frequency noise from power lines, potential and phase differences between power lines, and other factors. To prevent noise from entering on the GR (ground) terminal as a result of a difference in potential, wire the system as shown below.

- Connect all of the GR terminals on the Racks and ground them at one point only to 100 Ω or less.
- Short the LR terminals to the GR terminals.
- Use a ground wire of 2 mm^2 min.
- Insert 1:1 isolating transformers into the power supply lines and do not ground the secondary sides of the transformers.

Recommended Wiring



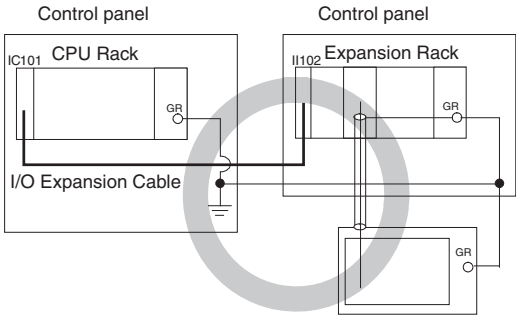
Wiring Susceptible to Noise



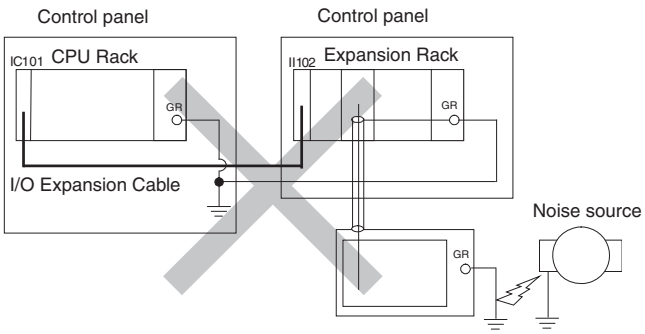
Wiring Communications Lines

When using communications from one or more Rack in the system, ground the entire system so that only one point is grounded. (Refer to user documentation for the devices connected.) For detailed connection methods, refer to the *Operation Manual* for the Communications Unit.

Recommended Wiring



Wiring Susceptible to Noise



Wiring

Terminal screws	M3.5 self-rising screws
Recommended wire size	AWG 14 min. (2 mm^2 min.)
Recommended tightening torque	0.8 N·m

Recommended crimp terminals

Manufacturer	Models	Shape	Applicable wire range (stranded wire)
JST Mfg.	V2-YS3A	Y-shaped terminal with sleeve	1.04 to 2.63 mm^2 (AWG 16 to 14)
	V2-M3(RAV2-3.5)	Round terminal with sleeve	

Note
1. Use crimp terminals for wiring.
2. Do not connect bare stranded wires directly to terminals.

5-4-2 Wiring CS-series Basic I/O Units with Terminal Blocks

I/O Unit Specifications

Double-check the specifications for the I/O Units. In particular, do not apply a voltage that exceeds the input voltage for Input Units or the maximum switching capacity for Output Units. Doing so may result in breakdown, damage, or fire.

When the power supply has positive and negative terminals, be sure to wire them correctly.

Wire Sizes

The following wire gauges are recommended.

Wire Size
AWG 22 (0.32 mm^2)

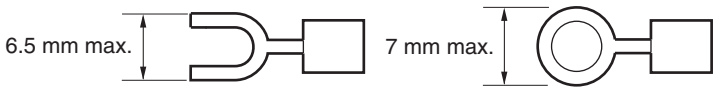
Note The current capacity of electric wire depends on factors such as the ambient temperature and insulation thickness as well as the gauge of the conductor.

Wiring

Terminal screws	M3.5 self-rising screws
Recommended wire size	AWG 22 to 18 (0.326 to 0.823 mm^2)
Recommended tightening torque	0.8 N·m

Recommended crimp terminals

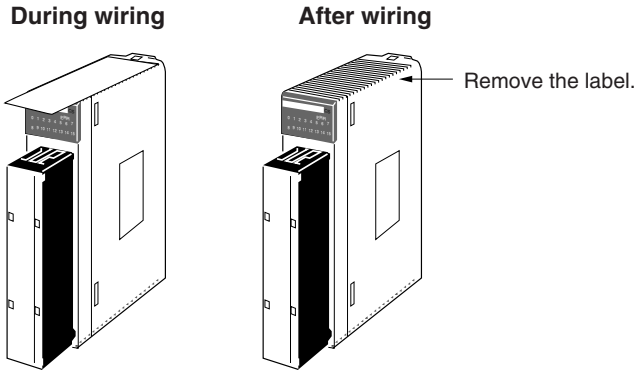
CS-series Basic I/O Units with 20-terminal Terminal Blocks



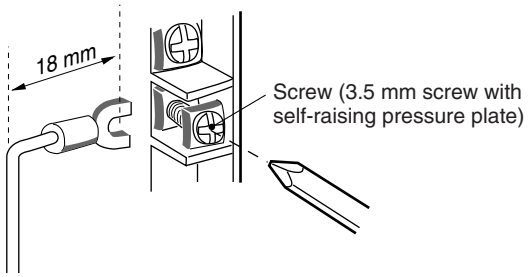
Manufacturer	Models	Shape	Applicable wire range (stranded wire)
JST Mfg.	V1.25-YS3A	Y-shaped terminal with sleeve	0.25 to 1.65 mm^2 (AWG 22 to 16)
	V1.25-M3(RAV1.25-3.5)	Round terminal with sleeve	

Note
1. Use crimp terminals for wiring.

2. Do not connect bare stranded wires directly to terminals.
   - Confirm that the Units have been mounted properly.
   - Cover the Unit while wiring to prevent wire clippings from entering the Unit. If there is a dustproof label on the top of the Unit, do not remote it before you wire the Unit. (Remove the label or other covering after wiring has been completed to allow air circulation needed for cooling.)

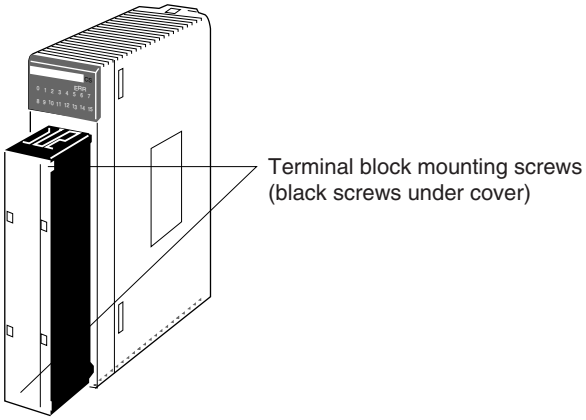


   - Wire the Units so that they can be easily replaced.
   - In addition, make sure that the I/O indicators are not covered by the wiring.
   - Do not place the wiring for I/O Units in the same duct or raceway as power lines. Inductive noise can cause errors in operation.
   - Tighten the terminal screws to the torque of 0.8 N·m.



Terminal Blocks

The I/O Units are equipped with removable terminal blocks. The lead wires do not have to be removed from the terminal block to remove it from an I/O Unit. The terminal block can be removed by taking out the terminal block mounting screws.



CS1-series Basic I/O Units

5-4-3 Wiring CS-series Basic I/O Units with Connectors

This section describes wiring CS-series Basic I/O Units with Connectors (32-, 64-, and 96-point Units). The user can combine a special connector with cable or use a preassembled OMRON cable to connect a High-density I/O Unit to a terminal block or I/O Terminal.

Note

1. Be sure not to apply a voltage that exceeds the input voltage for Input Units or the maximum switching capacity for Output Units.
2. When the power supply has positive and negative terminals, be sure to wire them correctly.
3. Use reinforced insulation or double insulation on the DC power supply connected to DC I/O Units when required by EU Directives (low voltage).
4. When connecting the connector to the I/O Unit, tighten the connector screws to a torque of 0.2 N·m.
5. Turn ON the power after checking the connector's wiring.
6. Do not pull the cable. Doing so will damage the cable.
7. Bending the cable too sharply can damage or break wiring in the cable.

Available Connectors

Use the following connectors when assembling a connector and cable.

CS-series 32- and 64-point I/O Units

The following connectors are recommended for attachment to CS-series 32- and 64-point I/O Units.

Connection	Pins	OMRON set	Fujitsu/Otax parts
Solder-type (included with Unit)	40	C500-CE404	Socket: Fujitsu FCN-361J040-AU Connector bar: Fujitsu FCN-360C040-J2 Otax N360C040J2
Crimp-type	40	C500-CE405	Socket: Fujitsu FCN-363J040 Otax N363J040 Connector bar: Fujitsu FCN-360C040-J2 Otax N360C040J2 Contacts: Fujitsu FCN-363J-AU Otax N363JAU
Crimp-type	40	C500-CE403	Fujitsu FCN-367J040-AU/F

Note Solder-type connectors are included with each Unit.

CS-series 96-point I/O Units

The following connectors are recommended for attachment to CS-series 96-point I/O Units.

Connection	Pins	OMRON set	Fujitsu/Otax parts
Solder-type (included with Unit)	56	CS1W-CE561	Socket: Fujitsu FCN-361J056-AU Connector bar: Fujitsu FCN-360C056-J3 Otax N360C056J3
Crimp-type	56	CS1W-CE562	Socket: Fujitsu FCN-363J056 Otax N363J056 Connector bar: Fujitsu FCN-360C056-J3 Otax N360C056J3 Contacts: Fujitsu FCN-363J-AU Otax N363JAU
Crimp-type	56	CS1W-CE563	Fujitsu FCN-367J056-AU/F Otax N367J056AUF

Note Solder-type connectors are included with each Unit.

Wire Sizes

We recommend using cable with wire gauges of AWG 28 to AWG 26 (0.2 mm^2 to 0.13 mm^2). Use cable with external wire diameters of 1.61 mm max.

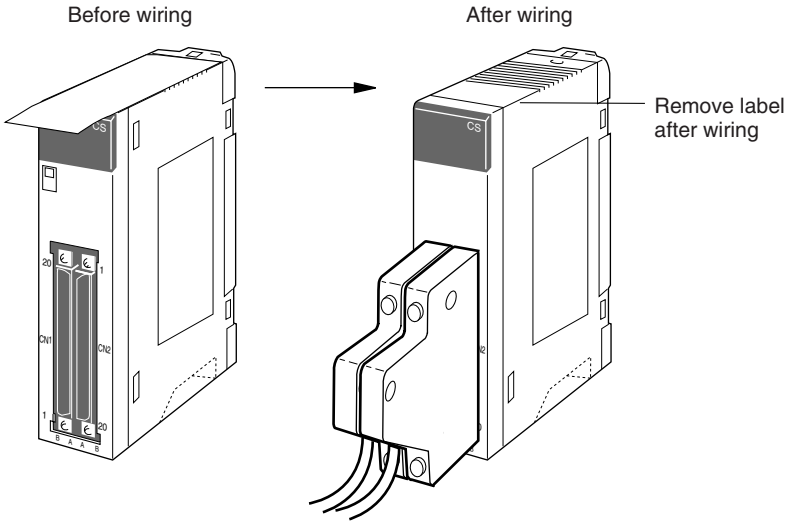
Wiring Procedure

1,2,3...

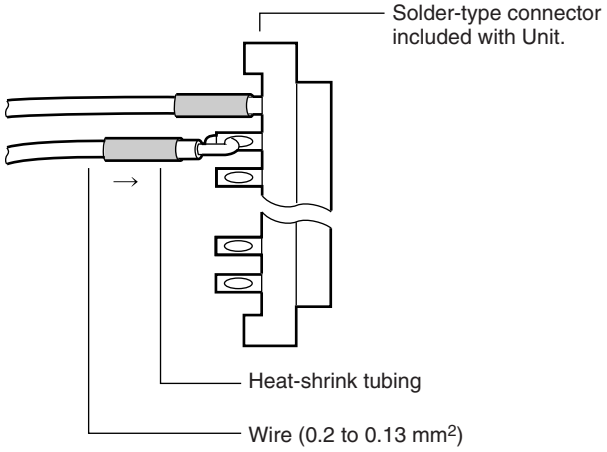
1. Check that each Unit is installed securely.

   Note Do not apply excessive force on the cables.

2. Cover the Unit while wiring to prevent wire clippings from entering the Unit. If there is a dustproof label on the top of the Unit, do not remote it before you wire the Unit. (Remove the label or other covering after wiring has been completed to allow air circulation needed for cooling.)

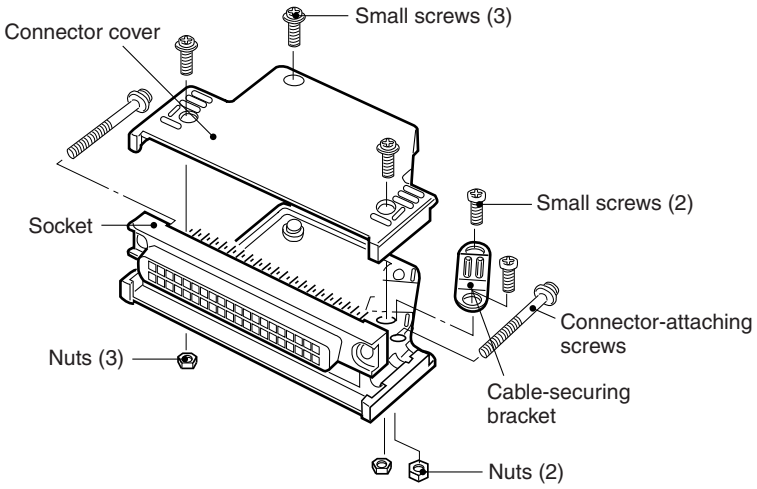


3. When solder-type connectors are being used, be sure not to accidentally short adjacent terminals. Cover the solder joint with heat-shrink tubing.

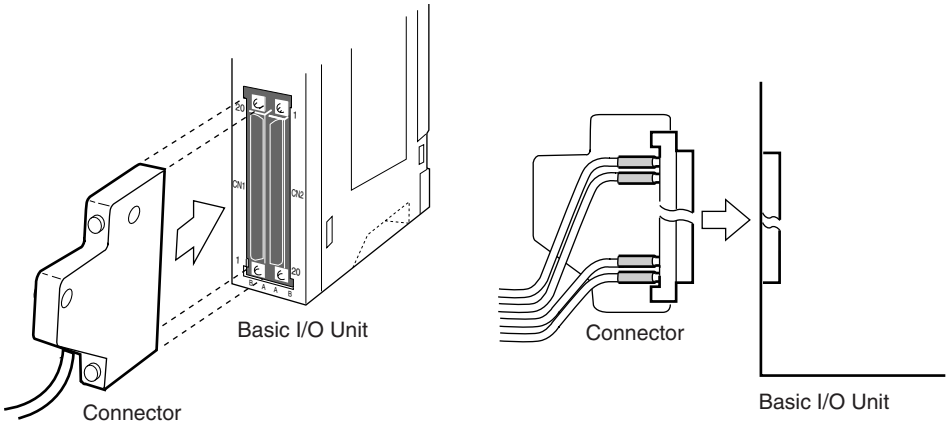


Note Double-check to make sure that the Output Unit's power supply leads haven't been reversed. If the leads are reversed, the Unit's internal fuse will blow and the Unit will not operate.

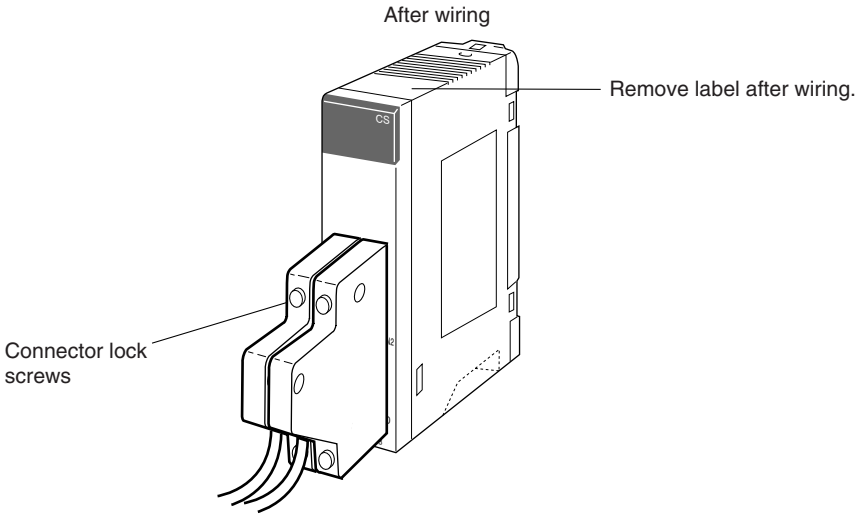
4. Assemble the connector (included or purchased separately) as shown in the following diagram. (The shape of the 56-pin connector is different.)



5. Insert the wired connector.



6. Remove the label or other covering after wiring has been completed to allow air circulation needed for cooling.

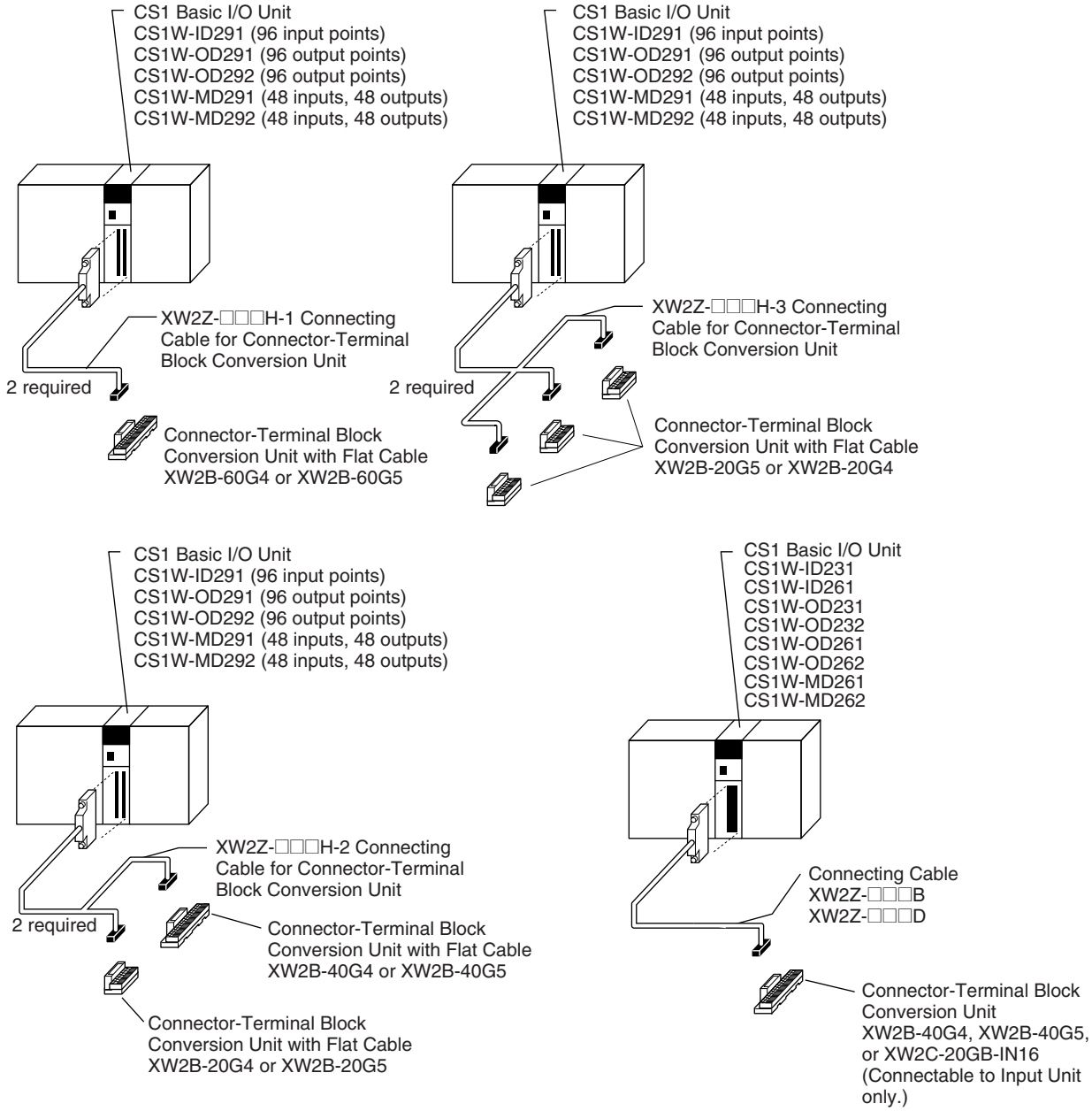


Tighten the connector-attaching screws to a torque of 0.2 N·m.

The following examples show applications for preassembled OMRON Cables. Contact your OMRON dealer for more details.

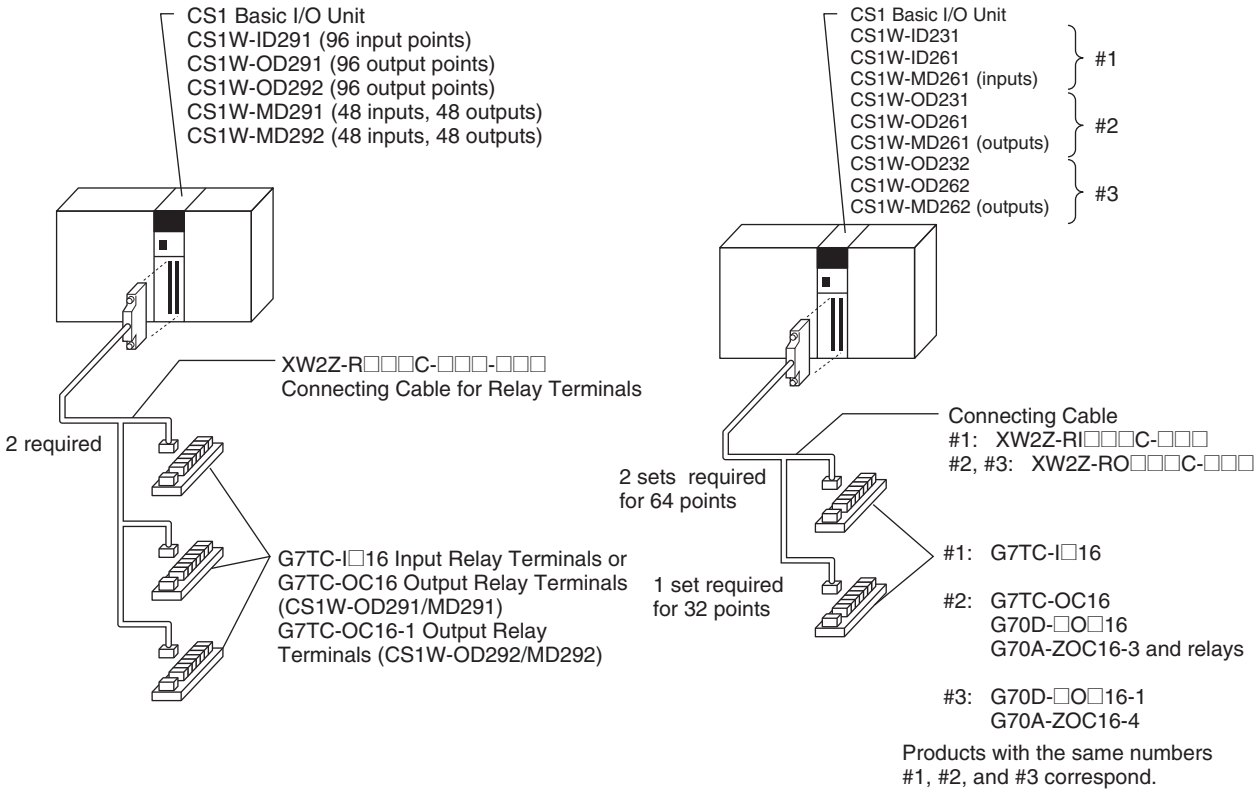
Connecting to a Terminal Block

Two sets of the following Cables and Conversion Units are required.


CS1 Basic I/O Unit
CS1W-ID291 (96 input points)
CS1W-OD291 (96 output points)
CS1W-OD292 (96 output points)
CS1W-MD291 (48 inputs, 48 outputs)
CS1W-MD292 (48 inputs, 48 outputs)
XW2Z-□□□H-1 Connecting Cable for Connector-Terminal Block Conversion Unit
2 required
Connector-Terminal Block Conversion Unit with Flat Cable
XW2B-60G4 or XW2B-60G5
CS1 Basic I/O Unit
CS1W-ID291 (96 input points)
CS1W-OD291 (96 output points)
CS1W-OD292 (96 output points)
CS1W-MD291 (48 inputs, 48 outputs)
CS1W-MD292 (48 inputs, 48 outputs)
XW2Z-□□□H-3 Connecting Cable for Connector-Terminal Block Conversion Unit
2 required
Connector-Terminal Block Conversion Unit with Flat Cable
XW2B-20G5 or XW2B-20G4
CS1 Basic I/O Unit
CS1W-ID291 (96 input points)
CS1W-OD291 (96 output points)
CS1W-OD292 (96 output points)
CS1W-MD291 (48 inputs, 48 outputs)
CS1W-MD292 (48 inputs, 48 outputs)
XW2Z-□□□H-2 Connecting Cable for Connector-Terminal Block Conversion Unit
2 required
Connector-Terminal Block Conversion Unit with Flat Cable
XW2B-40G4 or XW2B-40G5
Connector-Terminal Block Conversion Unit with Flat Cable
XW2B-20G4 or XW2B-20G5
CS1 Basic I/O Unit
CS1W-ID231
CS1W-ID261
CS1W-OD231
CS1W-OD232
CS1W-OD261
CS1W-OD262
CS1W-MD261
CS1W-MD262
Connecting Cable
XW2Z-□□□B
XW2Z-□□□D
Connector-Terminal Block Conversion Unit
XW2B-40G4, XW2B-40G5, or XW2C-20GB-IN16
(Connectable to Input Unit only.)

Connecting to a Relay Terminal

Two sets of the following Cables and Relay Terminals are required.



5-4-4 Connecting I/O Devices

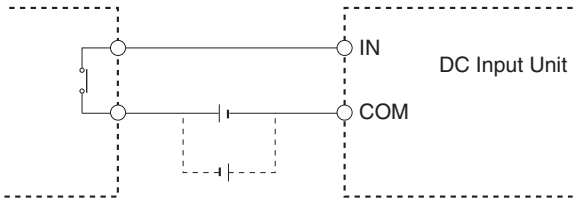
Input Devices

Use the following information for reference when selecting or connecting input devices.

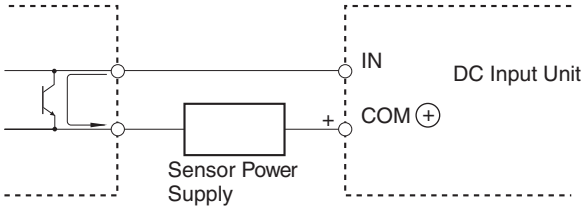
DC Input Units

The following types of DC input devices can be connected.

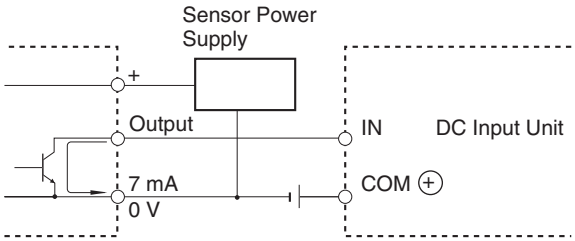
- Contact output



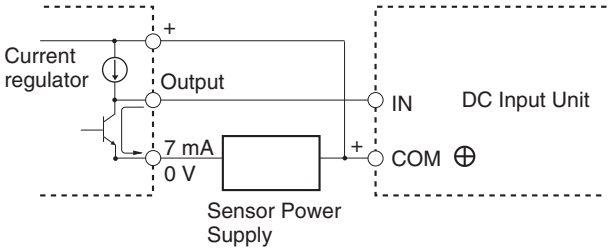
- Two-wire DC output



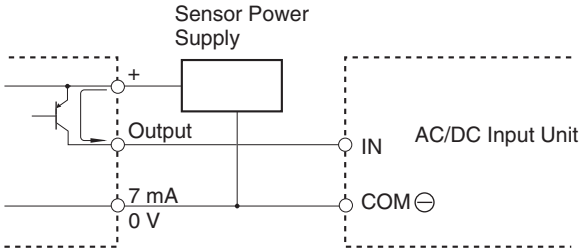
- NPN open-collector output



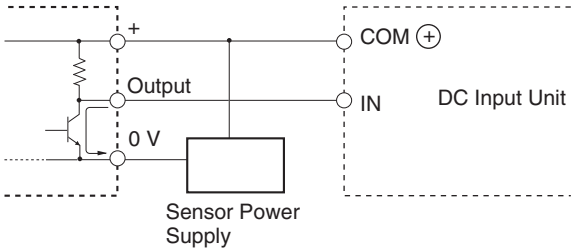
- NPN current output



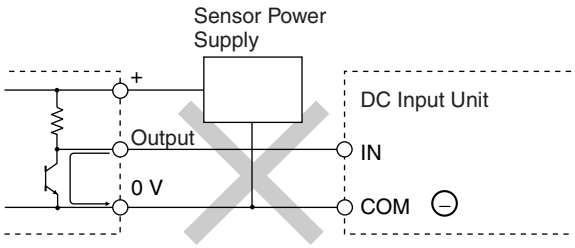
- PNP current output



- Voltage current output

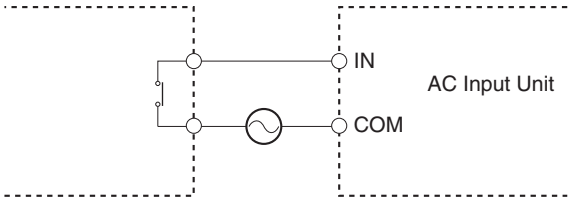


The circuit below should **NOT** be used for I/O devices having a voltage output.

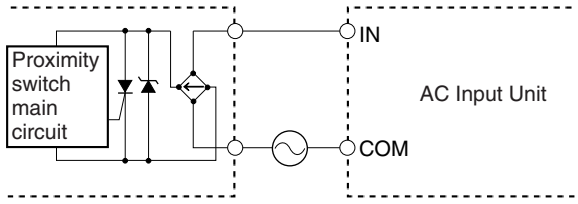


AC Input Units

- Contact output



- AC switching



Note When using a reed switch as the input contact for an AC Input Unit, use a switch with an allowable current of 1 A or greater. If Reed switches with smaller allowable currents are used, the contacts may fuse due to surge currents.

Precautions when Connecting a Two-wire DC Sensor

When using a two-wire sensor with a 12-V DC or 24-V DC input device, check that the following conditions have been met. Failure to meet these conditions may result in operating errors.

1,2,3...

1. Relation between voltage when the PLC is ON and the sensor residual voltage:

   $V_{ON} \leq V_{CC} - V_R$

2. Relation between voltage when the PLC is ON and sensor control output (load current):

   I_{OUT} (min) $\leq I_{ON} \leq I_{OUT}$ (max.)

   $I_{ON} = (V_{CC} - V_R - 1.5$ [PLC internal residual voltage]$)/R_{IN}$

   When I_{ON} is smaller than I_{OUT} (min), connect a bleeder resistor R. The bleeder resistor constant can be calculated as follows:

   $R \leq (V_{CC} - V_R)/(I_{OUT}$ (min.) $- I_{ON})$

   Power $W \geq (V_{CC} - V_R)^2/R \times 4$ [allowable margin]

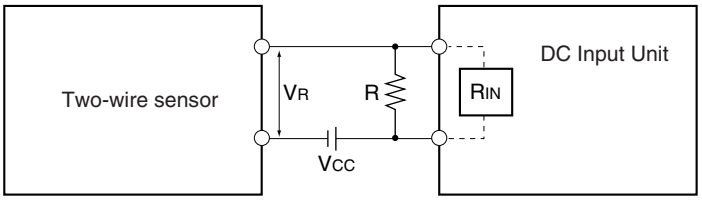
3. Relation between current when the PLC is OFF and sensor leakage current:

   $I_{OFF} \geq I_{leak}$

   If I_{leak} is larger than I_{OFF}, connect a breeder resistor. The breeder resistor constant can be calculated as follows:

   $R \leq R_{IN} \times V_{OFF}/(I_{leak} \times R_{IN} - V_{OFF})$

   Power $W \geq (V_{CC} - V_R)^2/R \times 4$ [allowable margin]



VCC: Power voltage
VON: PLC ON voltage
VOFF: PLC OFF voltage
ION: PLC ON current
IOFF: PLC OFF current
RIN: PLC input impedance

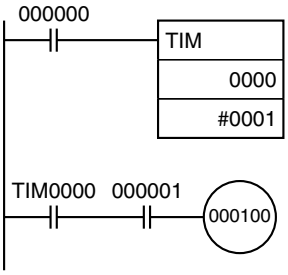
VR: Sensor output residual current
IOUT: Sensor control current (load current)
Ileak: Sensor leakage current
R: Bleeder resistance

4. Precautions on Sensor Surge Current

An incorrect input may occur if a sensor is turned ON after the PLC has started up to the point where inputs are possible. Determine the time required for sensor operation to stabilize after the sensor is turned ON and take appropriate measures, such as inserting into the program a timer delay after turning ON the sensor.

Example

In this example, the sensor's power supply voltage is used as the input to CIO 000000 and a 100-ms timer delay (the time required for an OMRON Proximity Sensor to stabilize) is created in the program. After the Completion Flag for the timer turns ON, the sensor input on CIO 000001 will cause output bit CIO 000100 to turn ON.



Output Wiring Precautions

Output Short-circuit Protection

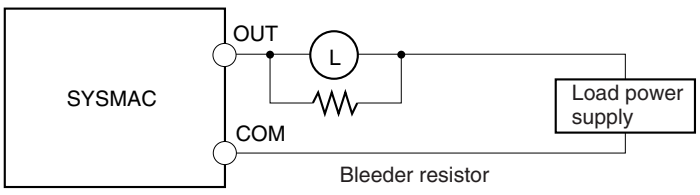
If a load connected to the output terminals is short-circuited, output components and the and printed circuit boards may be damaged. To guard against this, incorporate a fuse in the external circuit. Use a fuse with a capacity of about twice the rated output.

Transistor Output Residual Voltage

A TTL circuit cannot be connected directly to a transistor output because of the transistor's residual voltage. It is necessary to connect a pull-up resistor and a CMOS IC between the two.

Output Leakage Current

If a Triac Output Unit is used to drive a low-current load, the leakage current may prevent the output device from turning OFF. To prevent this, connect a bleeder resistor in parallel with the load as shown in the following diagram.



Use the following formula to determine the resistance and rating for the bleeder resistor.

$$R < \frac{V_{ON}}{I}$$

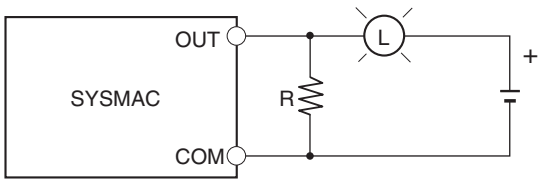
V_{ON}: ON voltage of the load (V)
I: Leakage current (mA)
R: Bleeder resistance (KΩ)

Output Surge Current

When connecting a transistor or triac output to an output device having a high surge current (such as an incandescent lamp), steps must be taken to avoid damage to the transistor or triac. Use either of the following methods to reduce the surge current.

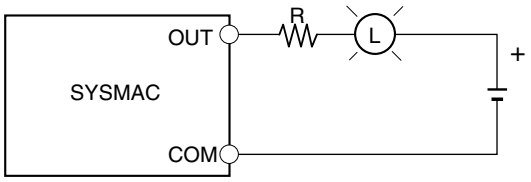
Method 1

Add a resistor that draws about 1/3 of the current consumed by the bulb.



Method 2

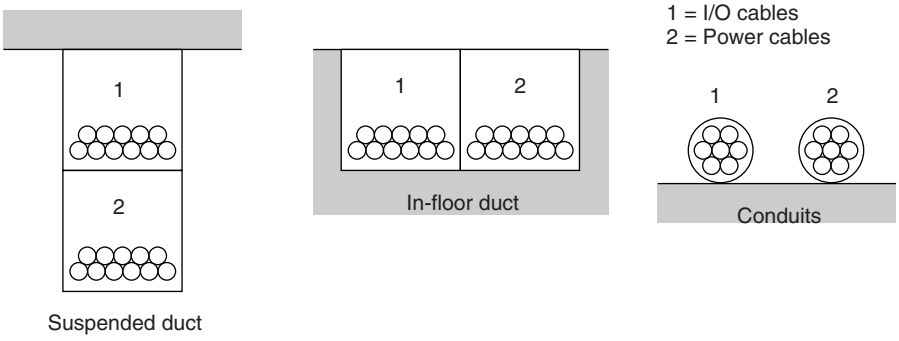
Add a control resistor as shown in the following diagram.



5-4-5 Reducing Electrical Noise

I/O Signal Wiring

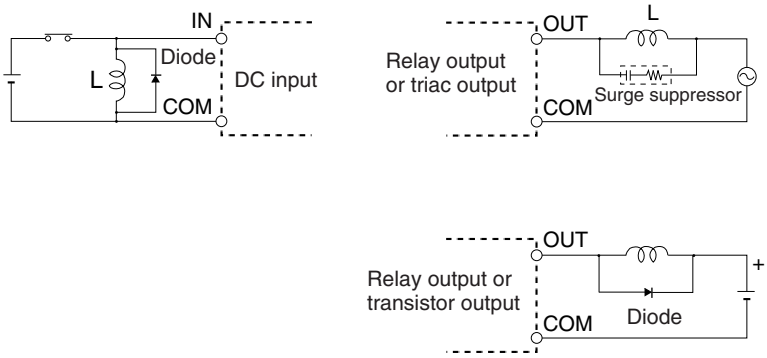
Whenever possible, place I/O signal lines and power lines in separate ducts or raceways both inside and outside of the control panel.



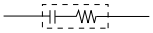
If the I/O wiring and power wiring must be routed in the same duct, use shielded cable and connect the shield to the GR terminal to reduce noise.

Inductive Loads

When an inductive load is connected to an I/O Unit, connect a surge suppressor or diode in parallel with the load as shown below.



Note Use surge suppressors and diodes with the following specifications.



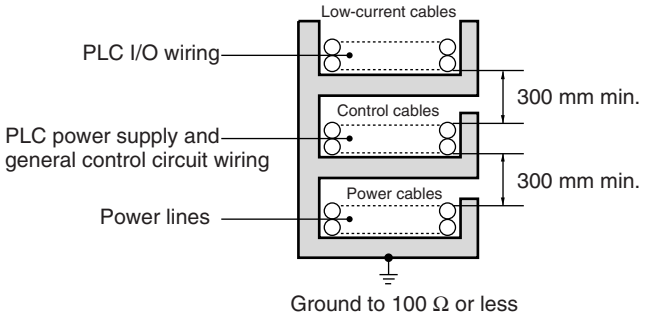
Resistance: 50 Ω
Capacitor: 0.47 μF
Voltage: 200 V

Breakdown voltage: 3 times load voltage min.
Mean rectification current: 1 A

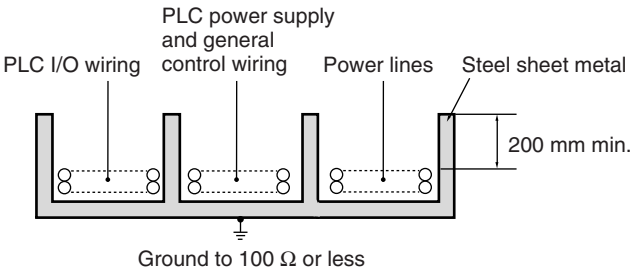
External Wiring

Observe the following precautions for external wiring.

- When multi-conductor signal cable is being used, avoid combining I/O wires and other control wires in the same cable.
- If wiring racks are parallel, allow at least 300 mm (12 inches) between the racks.



If the I/O wiring and power cables must be placed in the same duct, they must be shielded from each other using grounded steel sheet metal.



SECTION 6
PLC Setup

This section describes the settings in the PLC Setup and how they are used to control CPU Unit operation.

6-1 Overview of PLC Setup

The PLC Setup contains basic CPU Unit software settings that the user can change to customize PLC operation. These settings can be changed from a Programming Console or other Programming Device. The various settings for the CPU Unit are made in the PLC Setup.

6-1-1 Duplex System Settings

The following table lists cases in which the PLC Setup must be changed for Duplex Systems.

<table>
<tr><th colspan="2">Cases when settings must be changed</th><th colspan="2">PLC Setting(s) to be changed</th></tr>
<tr><td colspan="2">Reducing startup time when power is turned ON</td><td rowspan="3">CPU Duplex Tab Page
(See note 1.)</td><td>Run under Duplex Initial (under Operation Settings)</td></tr>
<tr><td colspan="2">Automatically returning to Duplex Mode after switching to Simplex Mode (continuing operation in Duplex Mode with a CPU Unit in which an operation switching error has occurred)</td><td>Return Automatically (under Operation Settings)</td></tr>
<tr><td colspan="2">Starting operation if either of the CPU Units is normal when the power is turned ON.</td><td>• Run under Duplex Initial (under Operation Settings)
• When an operation switching error occurs in the Active CPU Unit, the Standby CPU Unit will become the Active CPU Unit and start operating (See note 5.)</td></tr>
<tr><td colspan="2">Using the RS-232C port on the standby CPU Unit to independently (i.e., independent from the active CPU Unit's serial port) monitor operation via an RS-232C cable (write operations not allowed)</td><td>CPU Duplex Tab Page,
STB Serial Settings
(See note 1.)</td><td>Allow STB-COMM</td></tr>
<tr><td rowspan="2">Reducing the increase in the cycle time when initializing duplex operation</td><td>Using CPU Units containing the same program</td><td rowspan="2">CPU Duplex Tab Page,
CPU Unit Duplex Transfer Settings
(See note 1.)</td><td>Transfer Program</td></tr>
<tr><td>Not using the EM Area in the user program, data links, etc.</td><td>• Transfer EM
• Division Size</td></tr>
<tr><td colspan="2">Setting duplex operation for Memory Cards (See note 3.)</td><td>CPU Duplex Tab Page,
Memory Card Setting
(See note 1.)</td><td>Enable Memory Card Duplex Setting</td></tr>
<tr><td colspan="2">Removing a Unit that is operating without using the CPU Unit's Programming Device
Making I/O bus errors due to Unit failure non-fatal errors</td><td>CPU Duplex Tab Page,
Online Replacement
(See note 4.)</td><td>Allow removing Units without support software</td></tr>
<tr><td colspan="2">Replacing a Unit during operation without using the CPU Unit's Programming Device
Setting I/O bus errors as non-fatal errors when they are caused by a Unit failure</td><td>CPU Duplex Tab Page,
Online Replacement
(See notes 5 and 6.)</td><td>Enable removal/addition of units without support software</td></tr>
<tr><td colspan="2">Turning ON the following Special I/O Unit Error, Unit Number Flags and when a Special I/O Unit or CPU Bus Unit Error, Unit Number Flags during online Unit replacement.
Special I/O Units: A41800 to 42315
CPU Bus Units: A41700 to 41715</td><td>CPU Duplex Tab Page,
Online Replacement
(See notes 5 and 6.)</td><td>When removing any special unit, turn ON the error unit flag</td></tr>
</table>

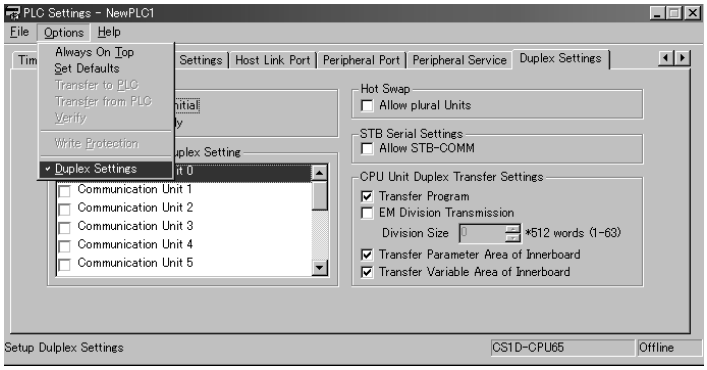
Note
1. Duplex CPU Systems only.
2. CS1D CPU Unit Ver. 1.1 or later and CX-Programmer version 4.0 or later only.
3. CX-Programmer version 3.1 or higher.
4. This function is supported only by Duplex CPU Units with Unit Ver. 1.2 or later and CX-Programmer version 6.1 or higher.

5. This function is supported only by Duplex CPU Units with Unit Ver. 1.3 or later.
6. Can be set in CX-Programmer Ver. 8.0 or later. The settings will be added to CX-Programmer version 7.0 when its functions are expanded by auto-update.

Making Settings from the CX-Programmer

When using CX-Programmer version 3.0 or higher, set the device type to "CS1H-H" in the PLC Setup and select ***Duplex Settings*** from the Options Menu on the PLC Settings Window to enable setting the PLC Setup for a CS1D.

When using CX-Programmer version 4.0 or higher and the device type is set to "CS1S-H" or "CS1D-S," is it not necessary to select ***Duplex Settings*** from the Options Menu on the PLC Settings Window to enable setting the PLC Setup for a CS1D.



6-1-2 Settings Other Than Those for Duplex Systems

The following table lists cases in which the PLC Setup must be changed for aspects of operation not directly related to duplex operation.

Cases when settings must be changed	Setting(s) to be changed
The input response time settings for Basic I/O Units must be changed in the following cases: • Chattering or noise occur in CS-series Basic I/O Units. • Short pulse inputs are being received for intervals longer than the cycle time.	Basic I/O Unit Input Response Time
Data in all regions of I/O Memory (including the CIO Area, Work Areas, Timer Flags and PVs, Task Flags, Index Registers, and Data Registers) must be retained when the PLC's power is turned ON.	IOM Hold Bit Status at Startup
The status of bits force-set or force-reset from a Programming Device (including Programming Consoles) must be retained when the PLC's power is turned on.	Forced Status Hold Bit Status at Startup
• You do not want the operating mode to be determined by the Programming Console's mode switch setting at startup. • You want the PLC to go into RUN mode or MONITOR mode and start operating immediately after startup. • You want the operating mode to be other than PROGRAM mode when the power is turned ON.	Startup Mode
Disabling detection of low-battery errors when it is not required.	Detect Low Battery
Detecting interrupt-task errors is not required.	Detect Interrupt Task Error (See note.)
Data files are required but a Memory Card cannot be used or the files are written frequently. (Part of the EM Area will be used as file memory.)	EM File Memory

Cases when settings must be changed	Setting(s) to be changed
The peripheral port will not be used with the Programming Console or CX-Programmer (peripheral bus) communications speed auto-detection and will not used the default host link communications settings such as 9,600 bps. **Note** With a Duplex CPU System, the PRPHL setting on the DIP switch on the front of the Duplex Unit must be ON to change the PLC Setup settings. With a Single CPU System, pin 4 the DIP switch on the front of the CPU Unit must be ON.	Peripheral Port Settings
The RS-232C port will not be used with the Programming Console or CX-Programmer (peripheral bus) communications speed auto-detection and will not use the default host link communications settings such as 9,600 bps. **Note** With a Duplex CPU System, the COMM setting on the DIP switch on the front of the CPU Unit must be OFF to change the PLC Setup settings. With a Single CPU System, pin 5 the DIP switch on the front of the CPU Unit must be OFF.	RS-232C Port Settings
You want to speed up communications with a PT via an NT Link.	Set the peripheral port or the RS-232C port communications port baud rate to "high-speed NT Link."
You want the intervals for scheduled interrupts to be set in units of 1 ms rather than 10 ms.	Schedules Interrupt Time Units (See note.)
You want CPU Unit operation to be stopped for instruction errors, i.e., when the ER Flag or AER Flag is turned ON. (You want instruction errors to be fatal errors.) You want to find the instructions where instruction errors are occurring (where the ER Flag is turning ON).	Instruction Error Operation
You want a minimum cycle time setting to create a consistent I/O refresh cycle.	Minimum Cycle Time
You want to set a maximum cycle time other than 1 second (10 ms to 40,000 ms).	Watch Cycle Time
You want to delay peripheral servicing so that it is executed over several cycles.	Fixed Peripheral Servicing Time (See note.)
You want to give priority to servicing peripherals over program execution. Here, "peripherals" include CPU Bus Units, Special I/O Units, Inner Boards, the built-in RS-232C port, and the peripheral port.	Peripheral Servicing Priority Mode (See note.)
A power OFF interrupt task will be used.	Power OFF Interrupt Task
You want to extend the detection of a power interruption.	Power OFF Detection Delay Time
IORF is executed in an interrupt task. (See note.) You want to shorten the average cycle time when a lot of Special I/O Units are being used. You want to extend the I/O refreshing interval for Special I/O Units.	Special I/O Unit Cyclic Refreshing
You want to improve both program execution and peripheral servicing response.	CPU Processing Mode (See note.)
You do not want to wait for Units and Boards to complete startup processing to start CPU Unit operation.	Startup Condition
You do not want to record user-defined errors for FAL(006) and FPD(269) in the error log.	FAL Error Log Registration
You want to reduce fluctuation in the cycle time caused by text string processing.	Background Execution for Table Data, Text String, and Data Shift Instructions (See note.)

Note Single CPU Systems only.

6-1-3 Tab Pages for Duplex Settings in the PLC Setup

The location of duplex settings and the tab labels in CX-Programmer are different between version 3.□ and version 4.0 or higher.

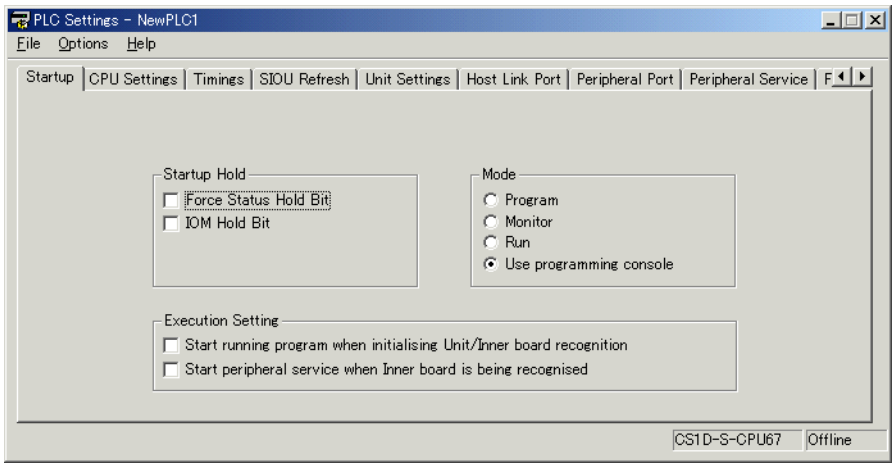
Settings	CX-Programmer Ver. 3.□	CX-Programmer Ver. 4.0 or higher
CPU Unit duplex settings	*Duplex* Tab Page	*Comms Unit Duplex* Tab Page
Communications duplex settings		*CPU Duplex* Tab Page

The CX-Programmer version 4.0 tab labels are used in this manual.

6-2 Specific PLC Setup Settings

The Programming Console addresses given in this section are used to access and change settings in the PLC Setup when using a Programming Console or the Programming Console function of an NS-series Programming Terminal. The PLC Setup is stored in the Parameter Area, which can be accessed only from a Programming Device. Do not use the Programming Console addresses as operands in programming instructions. They will be interpreted as addresses in the CIO Area of I/O memory.

6-2-1 Startup Tab Page



Startup Hold Settings

Forced Status Hold Bit

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
80	14	0: Cleared 1: Retained Default: 0	This setting determines whether or not the status of the Forced Status Hold Bit (A50013) is retained at startup. When you want all of the bits that have been force-set or force-reset to retain their forced status when the power is turned on, turn ON the Forced Status Hold Bit and set this setting to 1 (ON).	A50013 (Forced Status Hold Bit)	At startup

IOM Hold Bit

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
80	15	0: Cleared 1: Retained Default: 0	This setting determines whether or not the status of the IOM Hold Bit (A50012) is retained at startup. When you want all of the data in I/O Memory to be retained when the power is turned on, turn ON the IOM Hold Bit and set this setting to 1 (ON).	A50012 (IOM Hold Bit)	At startup

Mode Setting

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
81	---	Program: PROGRAM mode Monitor: MONITOR mode Run: RUN mode Use programming console: Programming Console's mode switch Default: Program	This setting determines whether the Startup Mode will be the mode set on the Programming Console's mode switch or the mode set here in the PLC Setup. If this setting is PRCN and a Programming Console isn't connected, startup mode will be RUN mode.	---	At startup

Execution Settings (Single CPU Systems Only)

Setting to Start Program without Waiting for Specific Units/Inner Board (Single CPU Systems Only)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
83	15	0: Wait for Units and Boards. 1: Don't wait. Default: 0	To start the CPU Unit in MONITOR or PROGRAM mode even if there is one or more Boards or Units that has not completed startup processing, set this setting to 1 (Don't wait for Units and Boards). (The operation for Inner Boards, however, also depends on the next setting.) To wait for all Units and Boards to finish startup processing, set this setting to 0 (Wait for Units and Boards).	---	At startup

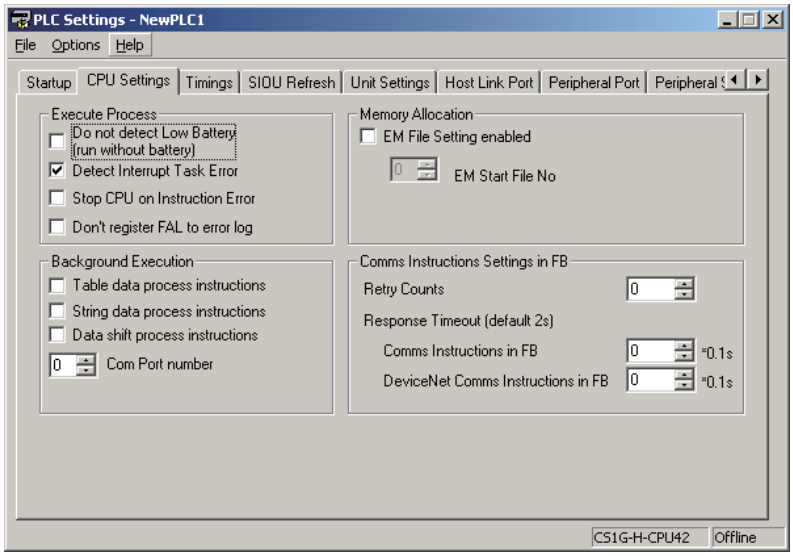
Note This setting cannot be used with Duplex CPU Systems.

Enable Setting in Word 83 for Inner Boards (Single CPU Systems Only)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
84	15	0: Wait for Boards. 1: Don't wait. Default: 0	To start the CPU Unit in MONITOR or PROGRAM mode even if there is one or more of Boards that has not completed startup processing, set this setting to 1 (Don't wait for Boards). To wait for all Boards to finish startup processing, set this setting to 0 (Wait for Boards). This setting is valid only if the Startup Condition is set to 1 (Don't wait for Units and Boards).	---	At startup

Note This setting cannot be used with Duplex CPU Systems.

6-2-2 CPU Unit Tab Page



Execute Process

Detect Low Battery

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
128	15	0: Detect 1: Do not detect Default: 0	This setting determines whether CPU Unit battery errors are detected. If this setting is set to 0 and a battery error is detected, the ERR/ALM indicator on the CPU Unit will flash and the Battery Error Flag (A40204) will be turned ON, but CPU Unit operation will continue.	A40204 (Battery Error Flag)	Takes effect the next cycle

Detect Interrupt Task Error (Single CPU Systems Only)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
128	14	0: Detect 1: Do not detect Default: 0	This setting determines whether interrupt task errors are detected. If this setting is set to 0 and an interrupt task error is detected, the ERR/ALM indicator on the CPU Unit will flash and the Interrupt Task Error Flag (A40213) will be turned ON, but CPU Unit operation will continue.	A40213 (Interrupt Task Error Flag)	Takes effect the next cycle

Note This setting cannot be used with Duplex CPU Systems.

Stop CPU on Instruction Error (Instruction Error Operation)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
197	15	0: Continue 1: Stop Default: 0	This setting determines whether instruction errors (instruction processing errors (ER) and illegal access errors (AER)) are treated as non-fatal or fatal errors. When this setting is set to 1, CPU Unit operation will be stopped if the ER or AER Flags is turned ON (even when the AER Flag is turned ON for an indirect DM/EM BCD error). Related Flags: A29508 (Instruction Processing Error Flag) A29509 (Indirect DM/EM BCD Error Flag) A29510 (Illegal Access Error Flag)	A29508, A29509, A29510 (If this setting is set to 0, these flags won't be turned ON even if an instruction error occurs.)	Takes effect at the start of operation

Don't Register FAL to Error Log (User-defined FAL Error Storage)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
129	15	0: Record user-defined FAL errors in error log. 1: Don't record user-defined FAL errors in error log. Default: 0	This setting determines if user-defined FAL errors created with FAL(006) and time monitoring for FPD(269) will be recorded in the error log (A100 to A199). Set it to 1 so prevent these errors from being recorded.	---	Whenever FAL(006) is executed (every cycle)

Memory Allocation Settings

EM File Setting Enabled

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
136	7	0: None 1: EM File Memory Enabled Default: 0	This setting determines whether part of the EM Area will be used for file memory.	---	After initialization from Programming Device or via FINS command.

EM Start File No. (Starting Memory Starting Bank)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
136	0 to 4	0 to 18 hex (0 to 24) Default: 0	If bit 7 (above) is set to 1, the setting here specifies the EM bank where file memory begins. The specified EM bank and all subsequent banks will be used as file memory. This setting will be disabled if bit 7 is set to 0.	A344 (EM File Memory Starting Bank)	After initialization from Programming Device or via FINS command.

Background Execution Settings (Single CPU Systems Only)

Table Data Process Instructions

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
198	15	0: Not executed in background 1: Executed in background Default: 0	This setting determines if Table Data Instructions will be processed over multiple cycle times (i.e., processed in the background).	---	Start of operation

Note This setting cannot be used with Duplex CPU Systems.

String Data Process Instructions

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
198	14	0: Not executed in background 1: Executed in background Default: 0	This setting determines if Text String Data Instructions will be processed over multiple cycle times (i.e., processed in the background).	---	Start of operation

Note This setting cannot be used with Duplex CPU Systems.

Data Shift Process Instructions

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
198	13	0: Not executed in background 1: Executed in background Default: 0	This setting determines if Data Shift Instructions will be processed over multiple cycle times (i.e., processed in the background).	---	Start of operation

Note This setting cannot be used with Duplex CPU Systems.

Communications Port Number for Background Execution

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
198	0 to 3	0 to 7: Communications ports 0 to 7 (internal logical ports)	The communications port number (internal logical port) that will be used for background execution.	---	Start of operation

Note This setting cannot be used with Duplex CPU Systems.

FB Communications Instruction Settings (CS1D-CPU□□HA/SA only)

The following PLC Setup settings are used only when using the OMRON FB Library.

■ Number of Resends

Programming Console address		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
+ 200	0 to 3	0 to F: 0 to 15 Default: 0	Set the number of retries for sending commands when executing DeviceNet explicit messages or FINS messages within function blocks.	A58000 to A58003	Start of operation

■ FB Communications Instruction Response Monitoring Time

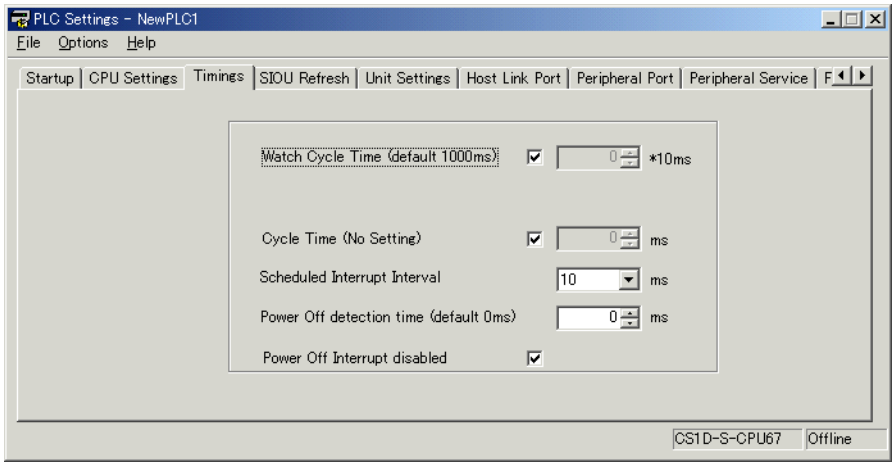
Programming Console address		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
+ 201	0 to 15	0001 to FFFF (Unit: 0.1 s, 0.1 to 6553.5) 0000: 2 s	A response timeout occurs when no response is returned within the time set here for FINS commands executed within a function block.	A581	Start of operation

■ DeviceNet Communications Instruction Response Monitoring Time

Programming Console address		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
+ 202	0 to 15	0001 to FFFF (Unit: 0.1 s, 0.1 to 6553.5) 0000: 2 s	A response timeout occurs when no response is returned within the time set here for explicit messages commands executed within a function block.	A582	Start of operation

Note The number of resends and response monitoring time must be set by the user in the FB communications instructions settings in the PLC Setup, particularly when using function blocks from the OMRON FB Library to execute FINS messages or DeviceNet explicit messages communications. The values set in this PLC Setup for OMRON FB Library will be automatically stored in the related Auxiliary Area words A580 to A582 and used by the function blocks from the OMRON FB Library.

6-2-3 Timings Tab Page



Watch Cycle Time

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
209	0 to 14	001 to FA0 hex: 10 to 40,000 ms (10-ms units) Default: 001 (1 s)	This setting is valid only when bit 15 of 209 is set to 1. The Cycle Time Overrun Flag (A40108) will be turned ON if the cycle time exceeds this setting.	A264 and A265 (Present Cycle Time)	At the start of operation (Can't be changed during operation.)

Enable Watch Cycle Time Setting

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
209	15	0: Default 1: Bits 0 to 14 Default: 0	Set to 1 to enable the Watch Cycle Time Setting in bits 0 to 14. Leave this setting at 0 for a maximum cycle time of 1 s.	A40108 (Cycle Time Overrun Flag)	At the start of operation (Can't be changed during operation.)

Cycle Time (Minimum Cycle Time)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
208	0 to 15	0001 to 7D00 hex: 1 to 32,000 ms (1-ms units) Default: 0000 hex (No minimum)	Set to 0001 to 7D00 to specify a minimum cycle time (in parallel processing mode, the cycle time for instruction execution, see note). If the cycle time is less than this setting, it will be extended until this time passes. Leave this setting at 0000 for a variable cycle time. (Can't be changed during operation.)	---	At the start of operation (Can't be changed during operation.)

Note Single CPU Systems only.

Schedule Interrupt Interval (Single CPU Systems Only)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
195	0 to 3	0 hex: 10 ms 1 hex: 1.0 ms Default: 0 hex	Sets the time interval for the scheduled interrupt task.	---	Takes effect at the start of operation. (Can't be changed during operation.)

Note This setting cannot be used with Duplex CPU Systems.

Power OFF Detection Time (Power OFF Detection Delay Time)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
225	0 to 7	00 to 0A hex: 0 to 10 ms (1-ms units) Default: 00 hex	This setting determines how much of a delay there will be from the detection of a power interruption (approximately 10 to 25 ms for AC power and 2 to 5 ms for DC power after the power supply voltage drops below 85% of the rated value) to the confirmation of a power interruption. The default setting is 0 ms. If enabled, the power OFF interrupt will be executed after a power interruption is confirmed (see note). If the power OFF interrupt is not enabled, the CPU Unit will be reset and operation will stop.	---	At startup or at the start of operation. (Can't be changed during operation.)

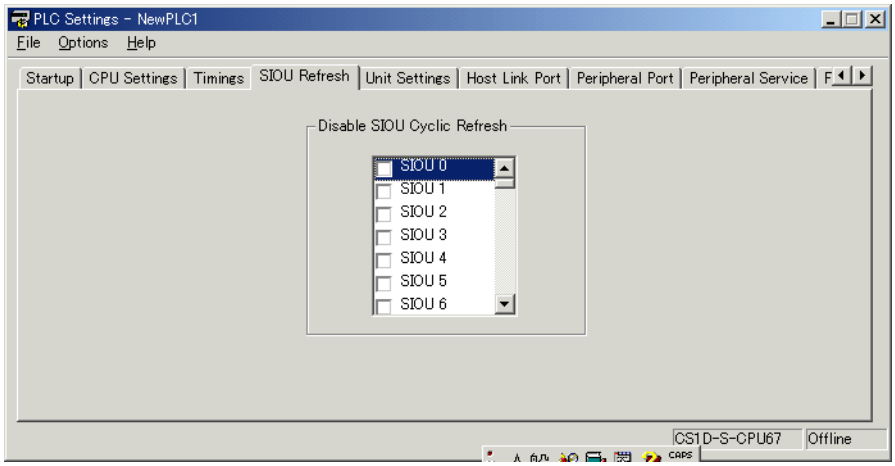
Note Single CPU Systems only.

Power OFF Interrupt Disable (Single CPU Systems Only)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
225	15	0: Disabled 1: Enabled Default: 0	When this setting is set to 1, the power OFF interrupt task will be executed when power is interrupted.	---	Takes effect at startup or at the start of operation. (Can't be changed during operation.)

Note This setting cannot be used with Duplex CPU Systems.

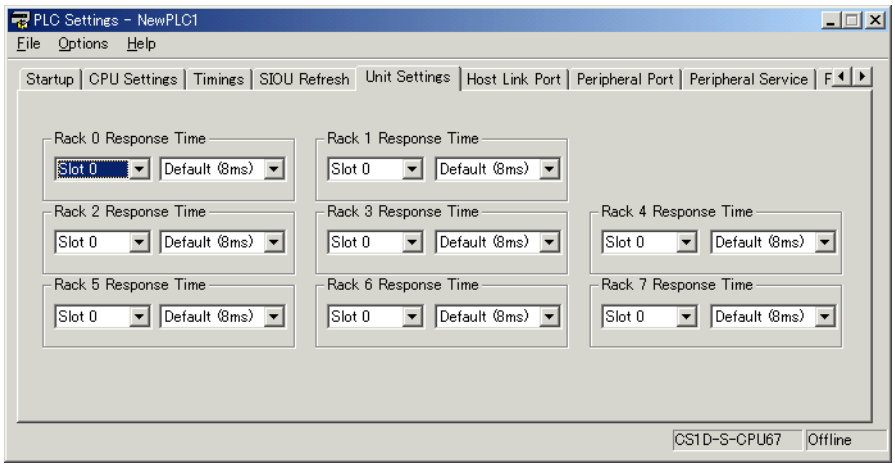
6-2-4 SIOU Refresh Tab Page



Special I/O Unit Cyclic Refreshing

Item	Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
	Word	Bit(s)				
Cyclic Refreshing of Units 0 to 15	226	0 to 15	0: Enabled 1: Disabled Default: 0	These settings determine whether data will be exchanged between the specified Unit and the Special I/O Unit's allocated words (10 words/Unit) during cyclic refreshing for Special I/O Units. Turn ON the corresponding bit to disable cyclic refreshing when several Special I/O Units are being used and you don't want to extend the cycle time or the cycle time is so short that the Special I/O Unit's internal processing can't keep up. (Special I/O Units can be refreshed from the program with IORF(097).)	---	At the start of operation
Cyclic Refreshing of Units 16 to 31	227	0 to 15	0: Enabled 1: Disabled Default: 0			
Cyclic Refreshing of Units 32 to 47	228	0 to 15	0: Enabled 1: Disabled Default: 0			
Cyclic Refreshing of Units 48 to 63	229	0 to 15	0: Enabled 1: Disabled Default: 0			
Cyclic Refreshing of Units 64 to 79	230	0 to 15	0: Enabled 1: Disabled Default: 0			
Cyclic Refreshing of Units 80 to 95	231	0 to 15	0: Enabled 1: Disabled Default: 0			

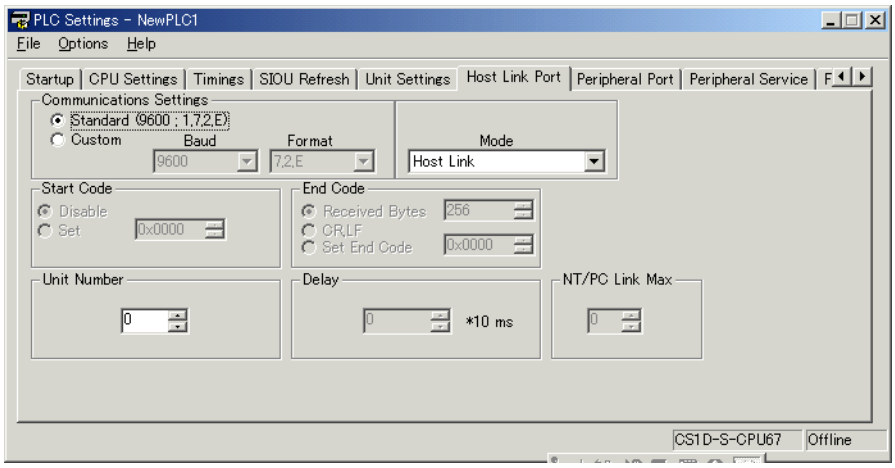
6-2-5 Unit Settings Tab Page



Basic I/O Unit Input (Rack) Response Times

Item	Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
	Word	Bit(s)				
Rack 0, Slot 0	10	0 to 7	00 hex: 8 ms 10 hex: 0 ms 11 hex: 0.5 ms 12 hex: 1 ms 13 hex: 2 ms 14 hex: 4 ms 15 hex: 8 ms 16 hex: 16 ms 17 hex: 32 ms Default: 00 hex (8 ms)	Sets the input response time (ON response time = OFF response time) for CS-series Basic I/O Units. The default setting is 8 ms and the setting range is 0.5 ms to 32 ms. This value can be increased to reduce the effects of chattering and noise, or it can be reduced to allow reception of shorter input pulses.	A220 to A259: Actual input response times for Basic I/O Units	At startup
Rack 0, Slot 1		8 to 15				
Rack 0, Slot 2	11	0 to 7				
Rack 0, Slot 3		8 to 15				
Rack 0, Slot 4	12	0 to 7				
Rack 0, Slot 5		8 to 15				
Rack 0, Slot 6	13	0 to 7				
Rack 0, Slot 7		8 to 15				
Rack 0, Slot 8	14	0 to 7				
Rack 0, Slot 9		8 to 15				
Rack 1, Slots 0 to 9	15 to 19	See Rack 0.				
Rack 2, Slots 0 to 9	20 to 24					
Rack 3, Slots 0 to 9	25 to 29					
Rack 4, Slots 0 to 9	30 to 34					
Rack 5, Slots 0 to 9	35 to 39					
Rack 6, Slots 0 to 9	40 to 44					
Rack 7, Slots 0 to 9	45 to 49					

6-2-6 Host Link Port Tab Page



With a Duplex CPU System, these settings are valid when the COMM pin on the DIP switch on the Duplex Unit is turned OFF.

With a Single CPU System, these settings are valid when the pin 5 on the DIP switch on the CPU Unit is turned OFF.

Host Link Settings

Communications Settings

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	15	0: Default (standard)* 1: PLC Setup (custom) Default: 0	*The default settings are for 1 start bit, 7 data bits, even parity, 2 stop bits, and a baud rate of 9,600 bps.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	8 to 11	00 hex: Host link 05 hex: Host link Default: 0	This setting determines whether the RS-232C port will operate in host link mode or another serial communications mode. (Host link can be specified with 00 or 05.) The Peripheral bus mode is for communications with Programming Devices other than the Programming Console.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Data Bits

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	3	0: 7 bits 1: 8 bits Default: 0	These settings are valid only when the communications mode is set to host link or no-protocol. These settings are also valid only when the RS-232C Port Settings Selection is set to 1: PLC Setup.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Stop Bits

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	2	0: 2 bits 1: 1 bit Default: 0	These settings are valid only when the communications mode is set to host link or no-protocol. These settings are also valid only when the RS-232C Port Settings Selection is set to 1: PLC Setup.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Parity

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	0 to 1	00: Even 01: Odd 10: None Default: 00	These settings are valid only when the communications mode is set to host link or no-protocol. These settings are also valid only when the RS-232C Port Settings Selection is set to 1: PLC Setup.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
161	0 to 7	00 hex: 9,600 01 hex: 300 02 hex: 600 03 hex: 1,200 04 hex: 2,400 05 hex: 4,800 06 hex: 9,600 07 hex: 19,200 08 hex: 38,400 09 hex: 57,600 0A hex: 115,200 (Unit: bps) Default: 00 hex	These settings are valid only when the communications mode is set to host link or no-protocol. These settings are also valid only when the RS-232C Port Settings Selection is set to 1: PLC Setup.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Unit Number (for CPU Unit in Host Link Mode)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
163	0 to 7	00 to 1F hex: (0 to 31) Default: 00 hex	This setting determines the CPU Unit's unit number when it is connected in a 1-to-N (N=2 to 32) Host Link.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

NT Link Settings

Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	8 to 11	02 hex: 1:N NT Link Default: 0	This setting determines whether the RS-232C port will operate in host link mode or another serial communications mode. **Note** Communications will not be possible with PTs set for 1:1 NT Links.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
161	0 to 7	00 hex: Standard 0A hex: High-speed NT Link* Default: 00 hex	* Set to 115,200 when setting this value from the CX-Programmer. To return to the standard setting, leave the setting set to "PLC Setup" and set the baud rate to 9,600 bps.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

NT Link Max. (Maximum Unit Number in NT Link Mode)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
166	0 to 3	0 to 7 Default: 0	This setting determines the highest unit number of PT that can be connected to the PLC.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Peripheral Bus Settings

Communications Settings

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	15	0: Default (standard)* 1: PLC Setup (custom) Default: 0	*The default settings are for a baud rate of 9,600 bps.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
160	8 to 11	04 hex: Peripheral bus Default: 0 hex	This setting determines whether the RS-232C port will operate in host link mode or another serial communications mode. (Host link can be specified with 00 or 05.) The Peripheral Bus mode is for communications with Programming Devices other than the Programming Console.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
161	0 to 7	00 hex: 9,600 06 hex: 9,600 07 hex: 19,200 08 hex: 38,400 09 hex: 57,600 0A hex: 115,200 (Unit: bps) Default: 00 hex	Settings 00 hex and 06 hex through 0A hex are valid when the communications mode is set to peripheral bus.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

No-protocol Settings

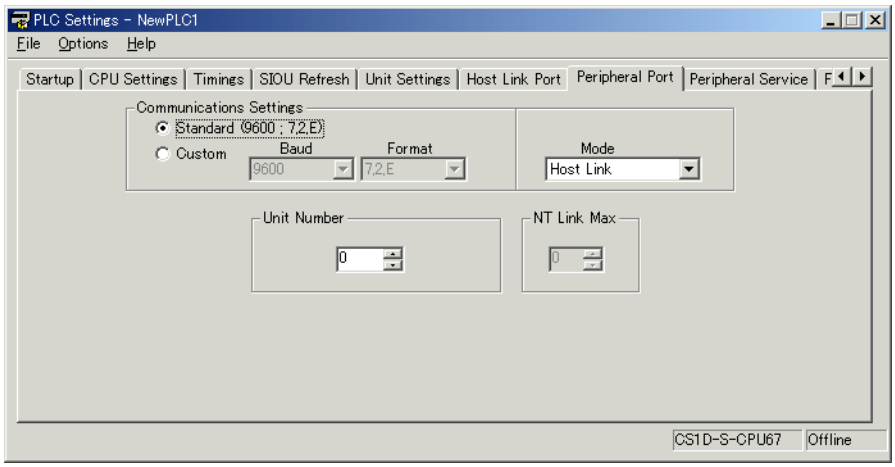
Delay

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
162	0 to 15	0000 to 270F hex: 0 to 99990 ms (10-ms units) Default: 0000 hex	This setting determines the delay from execution of TXD(236) until the data is actually transmitted from the specified port.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Start Code/End Code

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
164	8 to 15	00 to FF hex Default: 00 hex	Start code: Set this start code only when the start code is enabled (1) in bits 12 of 165.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)
	0 to 7	00 to FF hex Default: 00 hex	End code: Set this end code only when the end code is enabled (1) in bits 8 and 9 of 165.		
165	12	0: None 1: Code in 164 Default: 0	Start code setting: A setting of 1 enables the start code in 164 bits 8 to 15.		
	8 and 9	0 hex: None 1 hex: Code in 164 2 hex: CR+LF Default: 0 hex	End code setting: With a setting of 0, the amount of data being received must be specified. A setting of 1 enables the end code in bits 0 to 7 of 164. A setting of 2 enables an end code of CR+LF.		
	0 to 7	00 hex: 256 bytes 01 to FF hex: 1 to 255 bytes Default: 00 hex	Set the data length to be sent and received with no-protocol communications. The end code and start code are not included in the data length. Set this value only when the end code setting in bits 8 and of 165 is "0 hex: None." This setting can be used to change the amount of data that can be transferred at one time by TXD(236) or RXD(235). The default setting is the maximum value of 256 bytes.		

6-2-7 Peripheral Port Tab Page



With a Duplex CPU System, these settings are valid when the PRPHL pin on the DIP switch on the Duplex Unit is turned ON.

With a Single CPU System, these settings are valid when the pin 4 on the DIP switch on the CPU Unit is turned ON.

Host Link Settings

Communications Settings

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	15	0: Default (standard)* 1: PLC Setup (Custom) Default: 0	*The default settings are for 1 start bit, 7 data bits, even parity, 2 stop bits, and a baud rate of 9,600 bps.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	8 to 11	00 hex: Host Link 05 hex: Host link Default: 00 hex	This setting determines whether the peripheral port will operate in host link mode or another serial communications mode. (Host link can be specified with 00 or 05 hex.) The peripheral bus mode is for communications with Programming Devices other than the Programming Console.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Data Bits

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	3	0: 7 bits 1: 8 bits Default: 0	These settings are valid only when the communications mode is set to Host link. These settings are also valid only when the Peripheral Port Settings Selection is set to 1: PLC Setup.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Stop Bits

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	2	0: 2 bits 1: 1 bit Default: 0	These settings are valid only when the communications mode is set to Host link. These settings are also valid only when the Peripheral Port Settings Selection is set to 1: PLC Setup.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Format: Parity

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	0 and 1	00: Even 01: Odd 10: None Default: 00	These setting is valid only when the communications mode is set to Host link. These settings are also valid only when the Peripheral Port Settings Selection is set to 1: PLC Setup.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
145	0 to 7	00 hex: 9,600 01 hex: 300 02 hex: 600 03 hex: 1,200 04 hex: 2,400 05 hex: 4,800 06 hex: 9,600 07 hex: 19,200 08 hex: 38,400 09 hex: 57,600 0A hex: 115,200 (Unit: bps) Default: 00 hex	This setting is valid only when the communications mode is set to the Host Link mode. These settings are also valid only when the Peripheral Port Settings Selection is set to 1: PLC Setup.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Unit Number (for CPU Unit in Host Link Mode)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
147	0 to 7	00 to 1F hex (0 to 31) Default: 00 hex	This setting determines the CPU Unit's unit number when it is connected in a 1-to-N (N=2 to 32) Host Link.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

NT Link Settings

Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	8 to 11	02 hex:1: N NT Link Default: 00 hex	This setting determines whether the RS-232C port will operate in host link mode or another serial communications mode. **Note** Communications will not be possible with PTs set for 1:1 NT Links.	A61902 (RS-232C Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
145	0 to 7	00 hex: Standard 0A hex: High-speed NT Link* Default: 00 hex	* Set to 115,200 when setting this value from the CX-Programmer.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

NT Link Max. (Maximum Unit Number in NT Link Mode)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
150	0 to 3	0 to 7 hex Default: 0 hex	This setting determines the highest unit number of PT that can be connected to the PLC in NT Link mode.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Peripheral Bus Settings

Communications Setting

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	15	0: Default (standard)* 1: PLC Setup (custom) Default: 0	*The default settings are for a baud rate of 9,600 bps	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

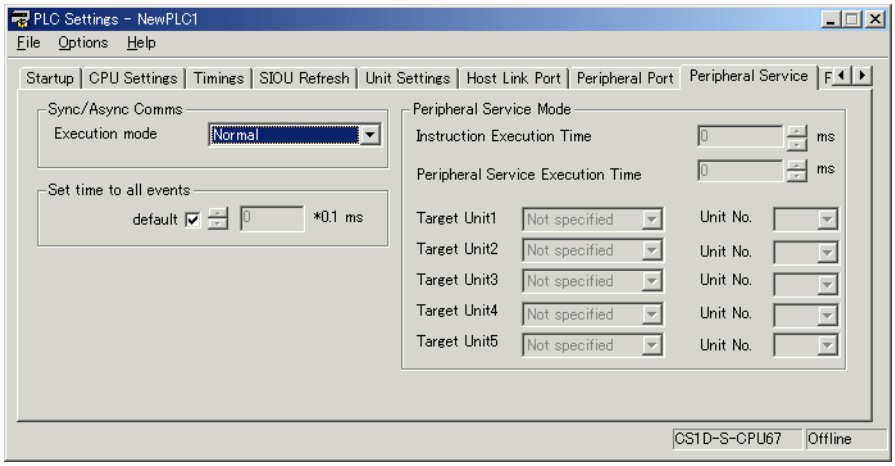
Mode: Communications Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	8 to 11	4 hex: Peripheral bus Default: 0 hex	This setting determines whether the communications mode for the peripheral port. The peripheral bus mode is used for all Programming Devices except for Programming Consoles.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

Baud Rate (bps)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
144	0 to 7	00 hex: 9,600 06 hex: 9,600 07 hex: 19,200 08 hex: 38,400 09 hex: 57,600 0A hex: 115,200 (Unit: bps) Default: 00 hex	The following settings are valid for the peripheral bus mode: 00 and 06 to 0A hex.	A61901 (Peripheral Port Settings Changing Flag)	Takes effect the next cycle. (Also can be changed with STUP (237).)

6-2-8 Peripheral Service Tab Page



CPU Execution Mode Setting (Sync/Async Comms) (Single CPU Systems Only)

Execution Mode

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
219	00 to 15	00 01 02 Default: 00	00: Not specified (disable parallel processing) 01: Synchronous (Synchronous Memory Access 02: Asynchronous (Asynchronous Memory Access)	---	Takes effect at the start of operation (Can't be changed during operation.)

Note
1. This setting cannot be used with Duplex CPU Systems. The default setting will be used even if the setting is changed.
2. A PLC Setup error will occur if any non-specified value is set.

Set Time to All Events (Fixed Peripheral Servicing Time)

Enable Fixed Servicing Time

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
218	15	0: Default* 1: Bits 0 to 7 Default: 0	Set to 1 to enable the fixed peripheral servicing time in bits 0 to 7. *Default: 4% of the cycle time	---	Takes effect at the start of operation (Can't be changed during operation.)

Fixed Servicing Time

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
218	0 to 7	00 to FF hex: 0.0 to 25.5 ms (0.1-ms units) Default: 00 hex	Set the peripheral servicing time. This setting is valid only when bit 15 of 218 is set to 1.	---	Takes effect at the start of operation (Can't be changed during operation.)

Peripheral Service Mode (Priority Mode) (Single CPU Systems Only)

Instruction Execution Time

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
219	08 to 15	00 05 to FF (hex) Default: 00 (hex)	00: Disable priority servicing 05 to FF: Time slice for instruction execution (5 to 255 ms in 1-ms increments)	A266 and A267	Takes effect at the start of operation (Can't be changed during operation.)

Note This setting cannot be used with Duplex CPU Systems.

Peripheral Service Execution Time

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
219	00 to 07	00 to FF (hex) Default: 00 (hex)	00: Disable priority servicing 01 to FF: Time slice for peripheral servicing (0.1 to 25.5 ms in 0.1-ms increments)	A266 and A267	Takes effect at the start of operation (Can't be changed during operation.)

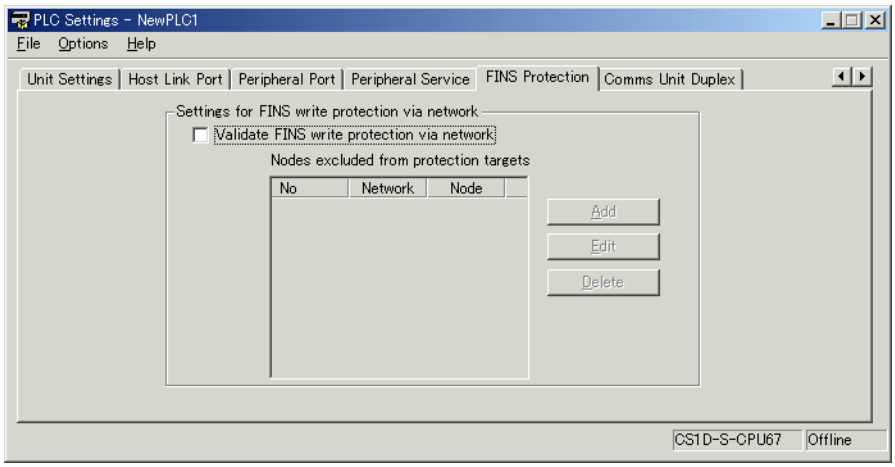
Note This setting cannot be used with Duplex CPU Systems.

Target Units (Units/Boards for Priority Servicing)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
220	08 to 15	00 10 to 1F 20 to 2F E1 FC FD Default: 00	Up to five Units and/or Boards can be specified for priority servicing. 00: Disable priority servicing 10 to 1F: CPU Bus Unit unit number + 10 (hex) 20 to 2F: CS-series Special I/O Unit unit number + 20 (hex) E1: Inner Boards FC: RS-232C port FD: Peripheral port	---	Takes effect at the start of operation (Can't be changed during operation.)
	00 to 07				
221	08 to 15				
	00 to 07				
222	08 to 15				

Note This setting cannot be used with Duplex CPU Systems.

6-2-9 FINS Protection Tab Page (Single CPU Systems Only)



Enabling FINS Write Protection (Use FINS Write Protection)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
448	15	0: Disable FINS write protection 1: Enable FINS write protection Default: 0	Enables or disables write protection for the CPU Unit from FINS command sent over a network (i.e., all connections except for serial connections).	---	At any time

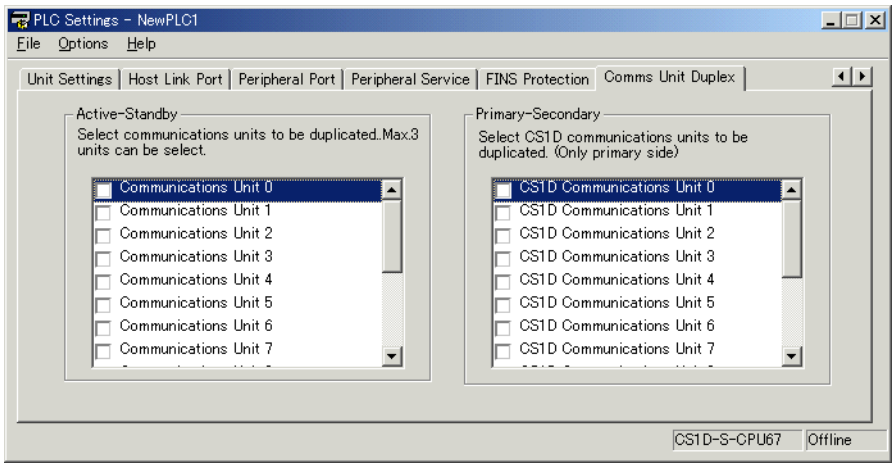
Note This setting cannot be used with Duplex CPU Systems.

Nodes Excluded from Write Protection (Protection Releasing Addresses)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
Set the nodes and networks from which FINS write operations will be enabled. The total number of nodes set to be excluded from write protection will be automatically set. A maximum of 32 nodes can be set. If these settings are not made (i.e., if the total number of nodes is 0), write operations will be disabled for all nodes but the local node. Note: This setting is valid only when FINS write protection has been enabled.					
449 to 480	8 to 15	0 to 127 (00 to 7F hex)	FINS command source network address	---	At any time
	0 to 7	1 to 255 (01 to FE hex) Note: 255 (FF hex) can be set to include all nodes in the specified network.	FINS command source node address	---	
448	0 to 7	0 to 32 (00 to 20 hex)	Number of nodes excluded from protection (Automatically calculated by the CX-Programmer; do not set.)	---	

Note This setting cannot be used with Duplex CPU Systems.

6-2-10 Comms Unit Duplex Tab Page



There are two methods that can be used for duplex communications: Active-standby and primary-secondary. There are options available for both in the PLC Setup. The methods that are used depends on the Communications Units. Refer to the operation manuals for the Communications Units for details.

Note CX-Programmer version 3.□ supports active-standby duplex communications, but it does not support primary-secondary communications for CS1D Communications Units.

Active-Standby Settings (Check Boxes for Communications Units 0 to 15)

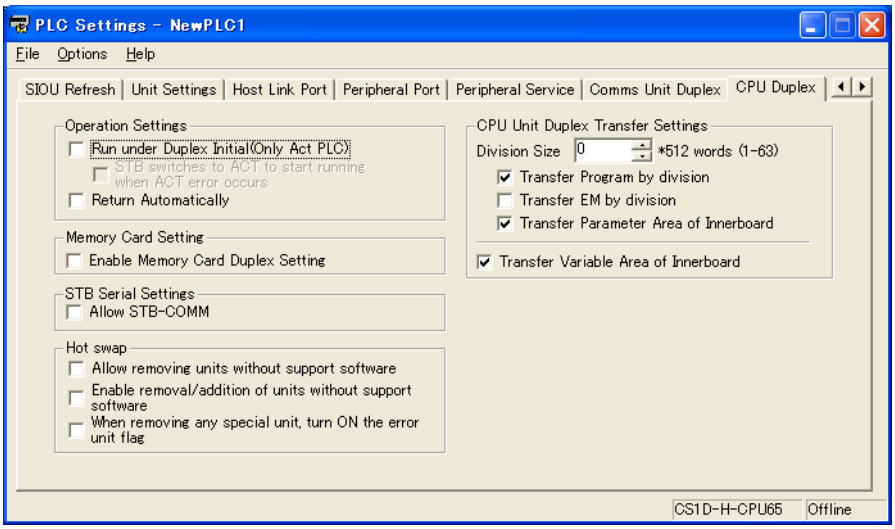
Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
121	0 to 15	0: Disable duplex settings for Communications Units 1: Enable duplex settings for Communications Units Default: 0	These settings (individual bits) enable or disable duplex settings for individual Communications Units. Bits 00 to 15 correspond to unit numbers 0 to F. To use Duplex Communications Units, setting them must be enabled here, and then either the I/O tables must be created automatically, or they must be edited to specify active and standby modes for the Communications Units and then transferred to the active CPU Unit. If necessary, the I/O table editing operations of the CX-Programmer can be used to specify the slot in which the standby Communications Unit is mounted.	---	At startup

Primary-Secondary Settings (Check Boxes for CS1D Communications Units 0 to 15)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
95	0 to 15	0: Disable duplex settings for Communications Units 1: Enable duplex settings for Communications Units Default: 0	These settings (individual bits) enable or disable duplex settings for individual Communications Units. Bits 00 to 15 correspond to unit numbers 0 to F. The secondary Communications Unit will be allocated the unit number one higher than the number assigned to the primary Communications Unit. Set only the unit number for the primary Communications Unit. To use Duplex Communications Units, setting them must be enabled here, and then either the I/O tables must be created automatically, or they must be edited to specify primary and secondary Units for the Communications Units and then transferred to the CPU Unit. If necessary, the I/O table editing operations of the CX-Programmer can be used to specify the slot in which the secondary Communications Unit is mounted.	---	At startup

Note This setting is supported only for CS1D CPU Units Ver. 1.1 or later. CX-Programmer version 4.0 or higher must be used to make the setting.

6-2-11 CPU Duplex Tab Page



Duplex Settings

Operation Settings, Run under Duplex Initial

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
123	14	0: Do not run during initialization (start running after initialization 1: Start running during initialization Default: 0	This setting determines where operation is started while the duplex system is being initialized. In Duplex Mode, duplex initialization starts after the power supply is turned ON. Normally, operation will begin only after initialization has been completed. This setting can be used to start operation before initialization has been completed. Use this setting to reduce startup time when the power is turned ON.	---	At startup

When an operation switching error occurs in the Active CPU Unit, the Standby CPU Unit will become the Active CPU Unit and start operating.

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
125	13	0: No check (When there is an error in the Active CPU Unit at startup, the Standby CPU Unit stays in standby status.) 1: Check performed (When there is an error in the Active CPU Unit at startup, the Standby CPU Unit becomes the Active CPU Unit and starts operating.) Default: 0	This setting determines whether the Standby CPU Unit will become the Active CPU Unit and starts operating if an error is detected in the Duplex CPU Unit set as the Active Unit when the power is turned ON. This setting is enabled when the Duplex system is set to *Start under Duplex Initial*.	---	At startup

Note
1. This setting can be used in all of the Duplex CPU Unit versions.
2. This setting can be selected with CX-Programmer version 6.1 or higher.

Operation Settings, Return Automatically

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
123	15	0: Do not automatically return to duplex operation 1: Automatically return to duplex operation Default: 0	When an error has caused operation to switch from Duplex Mode to Simplex Mode, this setting determines whether the PLC will attempt to return automatically to Duplex Mode or will stay in Simplex Mode. An automatic return to Duplex Mode will be attempted only if the same error does not reoccur in self-diagnosis. Automatic recovery can be set to give Duplex Mode priority for intermittent errors (e.g., WTD errors) or to eliminate the need to press the initialization button after replacing a CPU Unit online.	---	Every cycle

Memory Card Duplex Settings

Enable Memory Card Duplex Setting

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
130	15	0: Disable duplex operation for Memory Cards. 1: Enable duplex operation for Memory Cards. Default: 0	When data is written to Memory Cards, this setting determines whether it is written to the Memory Cards mounted in both CPU Units or to just the Memory Card in the active CPU Unit. **Note** No processing, however, is executed during duplex initialization to match the data on the Memory Cards mounted in the active and standby CPU Units. Therefore, before enabling duplex operation for Memory Cards, make sure that the contents and capacities are the same for both of the Memory Cards. **Note** Data read from the Memory Card mounted in the active CPU Unit is used by both the active and standby CPU Units.	---	Every cycle

Note Memory Card duplex operation can be selected with CX-Programmer Ver. 3.1 or higher.

STB Serial Settings

Allow STB-COMM

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
127	0 to 15	0000 hex: Disable independent communications on the standby CPU Unit's RS-232C port 5AA5 hex: Enable independent communications on the standby CPU Unit's RS-232C port Default: 0000	This setting determines if the RS-232C port on the standby CPU Unit can be used independently for read-only communications. To enable continuous communications for PTs or host computers even when the active CPU Unit is switched, the RS-232C ports on both the active and standby CPU Units must be connected using an RS-232C/RS-422 Adapter. When this is done, set this word to 0000 hex (i.e., disable independent monitoring operation on the standby CPU Unit's RS-232C port). If continuous communications are not required when the active CPU Unit is switched, then set this word to 5A5A hex (i.e., enable independent read-only communications on the standby CPU Unit's RS-232C port).	---	Every cycle

CPU Unit Duplex Transfer Settings

EM Division Transmission, Division Size

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
96	0 to 7	00 hex: 4,906 words 01 to 3F hex: 512 words x 1 to 63 Default: 00	This setting determines the number of words to transfer each cycle in units of 512 words. Normally, the default setting for 4,906 words is used.	---	At startup and at start of operation

Note If either the *Transfer Program* or *Transfer EM* option is selected the specified division size will be transferred each cycle.

Transfer Program

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
96	15	0: Transfer program 1: Do not transfer program Default: 0	This setting determines if the user program is transferred to the standby CPU Unit (including when the standby CPU Unit is replaced) when duplex operation is started. If the standby CPU Unit always contains the same program, then the transfer can be disabled to save time at startup.	---	At startup and at start of operation

EM Division Transmission

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
96	14	0:Transfer the EM Area together for duplex operation 1: Transfer the EM area over more than one cycle Default: 0	This setting determines the method that will be used to transfer the EM Area all at the same time or in pieces over more than one cycle (including when the standby CPU Unit is replaced). This setting can be used to reduce the cycle time by transferring the data in pieces whenever the EM Area is not used by the program, for data links, etc.	---	At startup and at start of operation

Transfer Parameter Area of Inner Board

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
96	11	0: Transfer Inner Board Parameter Area 1: Do not transfer Default: 0	This setting determines if the parameter area is transferred between Duplex Inner Boards.	---	At startup and at start of operation

Note As of October 2006, there are no Inner Boards to which this setting applies. Use the default setting.

Transfer Variable Area of Inner Board

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
96	10	0: Transfer Inner Board Variable Area 1: Do not transfer Default: 0	This setting determines if the variable area is transferred between Duplex Inner Boards.	---	At startup and at start of operation

Note As of October 2006, there are no Inner Boards to which this setting applies. Use the default setting.

Online Replacement Settings

Enabling Unit Removal without a Programming Device

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
131	0 to 15	Value other than 5AA5 hex: Online replacement can be performed with a Programming Device only. (An I/O bus error will occur if the Unit is removed without using a PLC Programming Device.) 5AA5 hex: Enable Unit removal without a Programming Device. Default: 0000	This setting determines if a Unit can be removed without a PLC Programming Device. 5AA5 hex: When Unit removal without Programming Device is enabled, I/O bus errors caused by Unit failures are treated as non-fatal errors. More than one Unit can be replaced at a time. A fatal error will occur if an Expansion Rack Cable, Backplane, Duplex Unit, or Long-distance Expansion I/O Rack is removed or fails.	A09911 A80015 A80215	Every cycle

Note
1. This setting can be used only in Duplex CPU Units with Unit Ver. 1.2 and later.
2. This setting can be selected with CX-Programmer version 6.1 or higher.

Enabling Unit Removal/Addition of Units without a Programming Device

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
132	8 to 15	Value other than AA hex: Online replacement can be performed with a Programming Device only. (An I/O bus error will occur if the Unit is removed without using a PLC Programming Device.) AA hex: Enable Unit removal/addition without a Programming Device. Default: 00	This setting determines if Units can be removed and added without a PLC Programming Device. With this setting, operation will recover automatically even if a Unit is added. AA hex: When Removal/Addition of Units without a Programming Device is enabled, I/O bus errors caused by Unit failures are treated as non-fatal errors. More than one Unit can be replaced at a time. A fatal error will occur if an Expansion Rack Cable, Backplane, Duplex Unit, or Long-distance Expansion I/O Rack is removed or fails.	A09911 A80015 A80215	Every cycle

Note 1. This setting is supported only in CS1D CPU Units with unit version 1.3 or later and a Duplex CPU, Dual I/O Expansion System.
If the *Removal/Addition of Units without a Programming Device* function is selected in a Duplex CPU, Single I/O Expansion System, the function will operate as the earlier *Unit Removal of without a Programming Device* function.

2. Can be set in CX-Programmer Ver. 8.0 or later. The setting will be added to CX-Programmer version 7.0 when its functions are expanded by auto-update.

Note If the *Unit Removal without a Programming Device* or *Removal/Addition of Units without a Programming Device* function is enabled, I/O bus errors will be treated as non-fatal errors and the PLC (CPU Unit) will not stop operating even if a Basic I/O Unit, Special I/O Unit, or CPU Bus Unit fails. If there are any Units that will adversely affect the system if an I/O bus error occurs, do not enable the *Unit Removal without a Programming Device* or *Removal/Addition of Units without a Programming Device* function in the PLC Setup.

Turning ON Error Unit Number Flag when Removing a Special I/O Unit Error or CPU Bus Unit (*When removing any special unit, turn ON the error unit flag* in the CX-Programmer)

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
132	0 to 7	AA hex: When a Special I/O Unit or CPU Bus Unit is replaced online, the corresponding Special I/O Unit Error Unit Number Flag or CPU Bus Unit Error Unit Number Flag will go ON. Value other than AA hex: The Unit Number Flags do not operate. Default: 00	When this setting is enabled, the corresponding Unit Number Error Flag (listed below) will go ON during replacement. Special I/O Units: A41800 to 42315 CPU Bus Units: A41700 to 41715	A418 to A423 A417	Every cycle

Note 1. This setting is supported only in CS1D CPU Units with unit version 1.3.

2. Can be set in CX-Programmer Ver. 8.0 or later. The setting will be added to CX-Programmer version 7.0 when its functions are expanded by auto-update.

6-2-12 Other Settings

Online Replacement: Hot Swap

Replacing Multiple Units Online

Address in Programming Console		Settings	Function	Related flags and words	New setting's effectiveness
Word	Bit(s)				
122	15	0: Disable online replacement of multiple Units 1: Enable online replacement of multiple Units Default: 0	This setting determines if only one Unit can be replaced online at the same time or if multiple Units can be replaced. Replacing more than one Unit at a time will increase the likelihood of operating errors.	---	Every cycle

Note This setting is supported only by a Programming Console.

SECTION 7
I/O Allocations

This section describes I/O allocations to Basic I/O Units, Special I/O Units, and CPU Bus Units, and data exchange with CPU Bus Units.

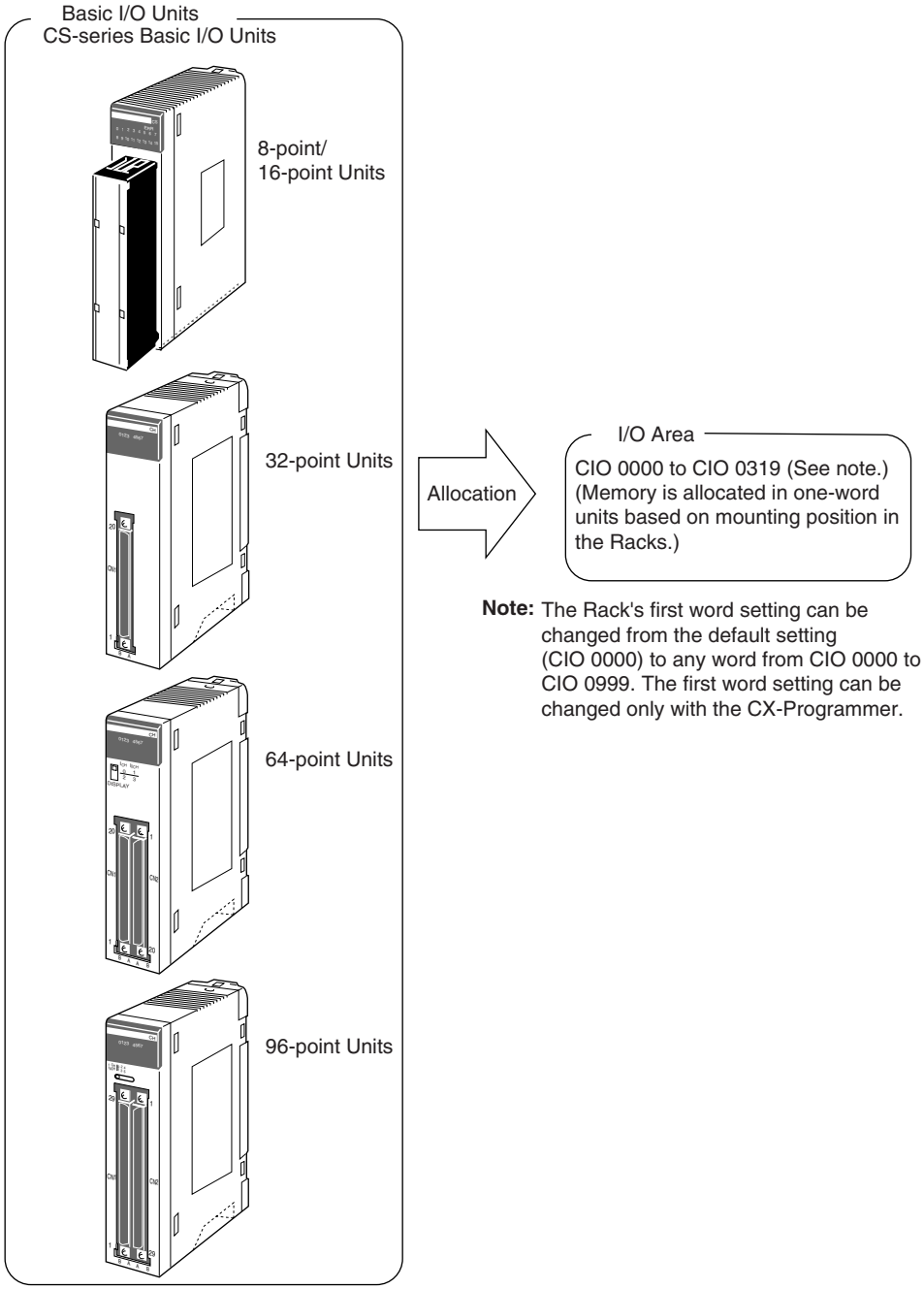
7-1 I/O Allocations

In CS1D PLCs, memory must be allocated to the Units mounted in the PLC. I/O tables containing the models and locations of all Units and the allocations made to each must be created and these I/O tables must be registered in the CPU Unit. When the power supply is turned ON, the I/O tables are compared against the mounted Units to verify their accuracy. The methods for creating I/O tables are the same for both Duplex CPU and Single CPU Systems.

7-1-1 Unit Types

Memory is allocated differently to Basic I/O Units, Special I/O Units, and CS-series CPU Bus Units.

Basic I/O Units

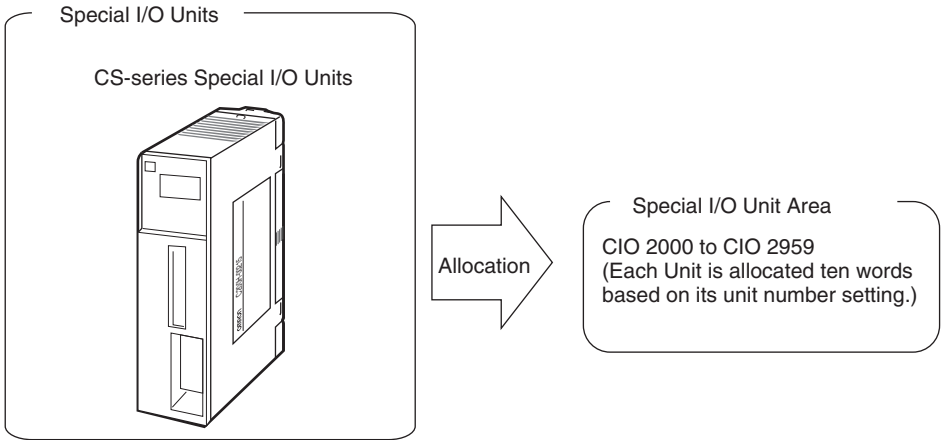


Note: The Rack's first word setting can be changed from the default setting (CIO 0000) to any word from CIO 0000 to CIO 0999. The first word setting can be changed only with the CX-Programmer.

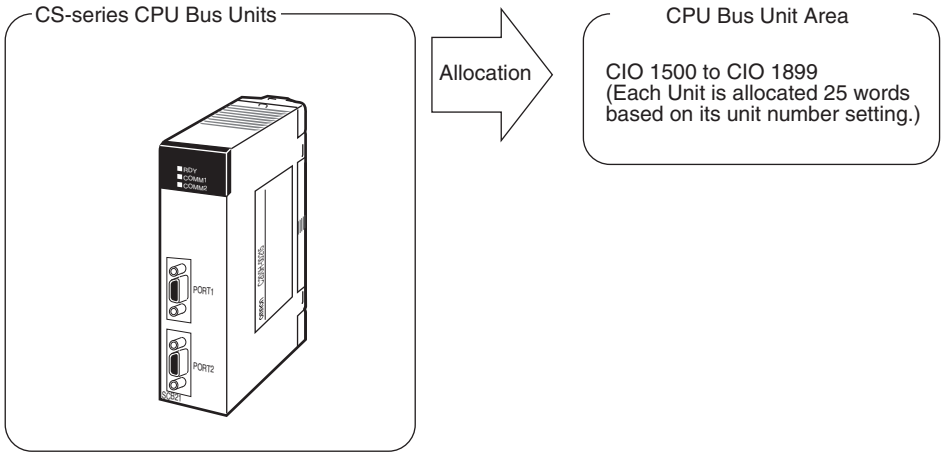
The following table shows the maximum number of Units that can be mounted in each type of system.

System		Max. number of Units
Duplex CPU, Dual I/O Expansion System	Duplex Connecting Cables	52
	Single Connecting Cable	60
Duplex CPU, Single I/O Expansion System		68
Single CPU System		71

Special I/O Units



CS-series CPU Bus Units



7-1-2 Creating I/O Tables

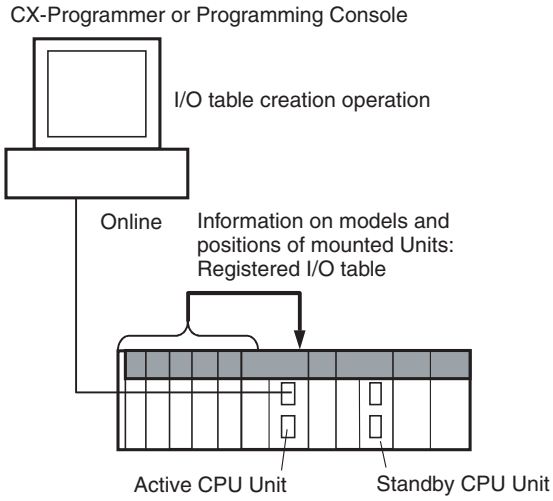
There are two ways to allocate I/O memory to CS1D Units.

- Create the I/O tables online based on the Units actually mounted to the PLC. This can be done from either the CX-Programmer or a Programming Console. The Programming Device is connected online and then the I/O tables are created based on the Units that are mounted.
- Create the I/O tables offline without basing them directly on the mounted Units and then transfer the I/O tables to the PLC. This is done offline on the CX-Programmer.

The word addresses, number of words, and mounting slot for each Unit are registered in the CPU Unit as I/O tables. Data is exchanged between the Units and the CPU Unit, e.g., to help prevent mistakes in mounting when replacing Units.

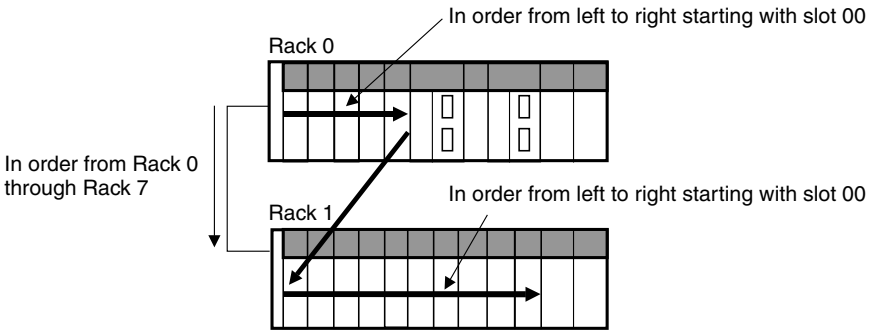
Creating I/O Tables Based on Mounted Units

Connect a Programming Console or the CX-Programmer to a CPU Unit in a PLC with all the Units mounted and create the I/O tables. In the I/O table creation operation, information on the Unit models and mounting locations are registered in the parameter area of the CPU Unit as the registered I/O tables for all Units mounted to the basic PLC system.



I/O Memory Allocations

When I/O memory is allocated automatically, words are automatically allocated to Units in the order they are mounted to the Racks. Words are allocated to Units from left to right starting on Rack 0 and then left to right on each Rack through Rack 7.



II/O Table Creation with CX-Programmer

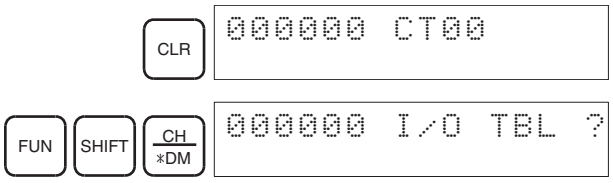
Use the following procedure to create the I/O tables online with the CX-Programmer.

1,2,3...

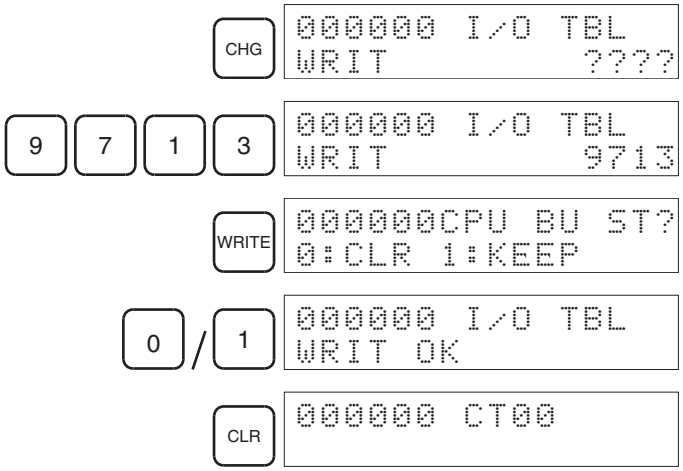
1. Double-click ***IO Table*** in the project tree in the main window. The I/O Table Window will be displayed.
2. Select ***Options - Create.*** The models and positions of the Units mounted to the Racks will be written to the CPU Unit as the registered I/O tables.

I/O Table Creation with a Programming Console

Use the following procedure to register the I/O table with a Programming Console.

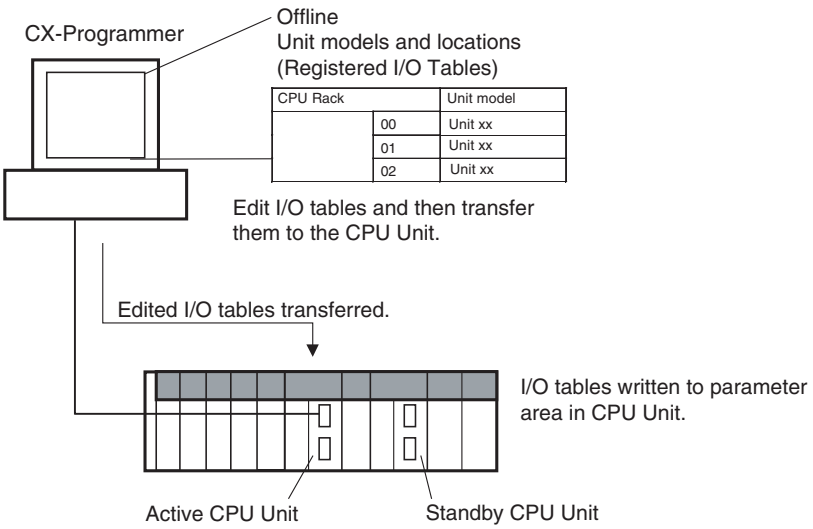


Note If the Rack first words have already been set from the CX-Programmer, "Rack 1st Word En" will be displayed on the second line.



Creating I/O Tables without Mounted Units

With the CX-Programmer, I/O tables can be created offline without mounted Units and then transferred to the CPU Unit. The information on Unit models and mounting locations are written to the parameter area of the CPU Unit as the registered I/O tables.



I/O Table Creation with CX-Programmer

Use the following procedure to create the I/O tables offline with the CX-Programmer and then transfer them to the CPU Unit. Once the Units that are to

be mounted are set for each Rack, the CX-Programmer will automatically allocate words according to Rack and slot positions starting from CIO 0000.

1,2,3...

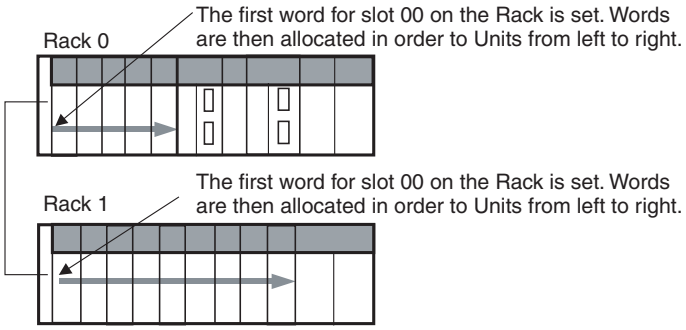
1. Double-click ***IO Table*** in the project tree in the main window. The I/O Table Window will be displayed.
2. Double-click the Rack to be edited. The slots will be displayed for the Rack.
3. Right-click the slot to which to assign a Unit and select the Unit from the pop-up menu.
4. When all the desired Units have been assigned to slots, select ***Options - Transfer to PLC***. The I/O tables will be transferred.

With the CX-Programmer, you can also assign any desired word to an I/O Unit regardless of it's position on the Racks.

Setting the First Word on a Rack

The first word allocated on a Rack can be set to allocate specific words to the Units on the Rack regardless of the order in which the Rack is connected. Words will be allocated consecutively to the Units on the Rack in the order that Units are mounted to the Rack. Refer to *7-3 Allocating First Words to Racks* for details.

Setting the First Word on Each Rack

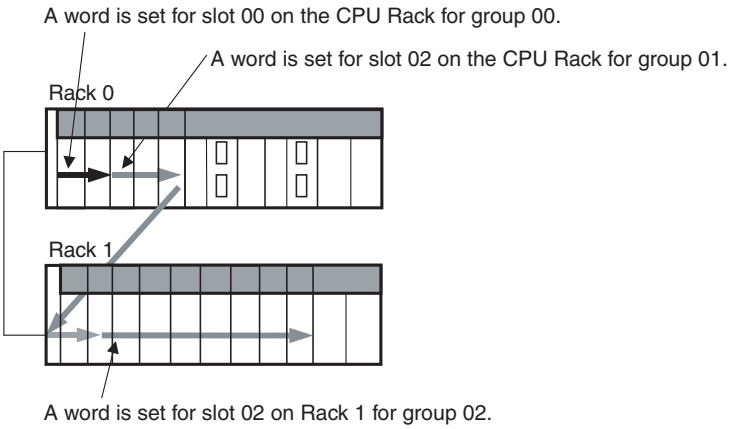


Note The first words for Racks cannot be set at the same time as the first words for slots.

Setting the First Word for a Slot

The first word allocated to the Unit in any slot on any Rack can be set regardless of the order of the Rack or the position of the slot. Words are then allocated in sequence to the following Units in the order they are mounted. Refer to *7-4 Allocating First Words to Slots (Single CPU Systems Only)* for details.

Setting the First Words for Specific Slots



Note The first words for Racks cannot be set at the same time as the first words for slots.

Overview

Method	Operation	Allocations		Rack allocation order	Slot allocation order within Rack
Using actual mounted Units	Perform I/O table creation online.	Automatic allocations according to mounting position		In order from Rack 0 to Rack 7	Left to right from slot 00
Not using actual mounted Units	Edit the I/O tables offline and transfer them to CPU Unit.	Automatic allocations according to mounting position		In order from Rack 0 to Rack 7	Left to right from slot 00
		Partial manual allocation without restrictions by mounting position	Allocating Rack first words	User-set	Left to right from slot 00
			Allocation slot first words		Left to right from any slot allocated a first word

Note

1. Always create I/O tables either online or by editing them offline and transferring them to the CPU Unit. The CPU Unit will not be able to recognize Basic I/O Units, Special I/O Units, or CPU Bus Units unless I/O tables are registered in the CPU Unit.
2. Both duplex Ethernet Units will be reset and communications will temporarily stop when I/O tables are created or transferred or Units are added online in a system that uses duplex Ethernet with the CS1D. Confirm that the system will not be adversely affected before executing these operations.
3. For CPU Bus Units can be used even if they are not registered in the I/O tables, this function is provided to enable online connections from Programming Devices running on personal computers (e.g., the CX-Programmer) and is not intended for normal system operation. Always register I/O tables in the CPU Unit before starting operation.
4. The C200HX/HG/HE, C200H, and C200HS PLCs use fixed word allocations for slots, enabling operation without I/O tables. I/O tables were created only to prevent Units from being mounted to the wrong slot. With the CS-series PLCs, the words allocated to any particular slots are not fixed. Words are merely allocated to the Units actually mounted. If no Unit is mounted, no words are allocated. If the mounted Unit requires more than one word, the required number of words is allocated. Operation for CS-series PLCs is thus not possible unless I/O tables are registered.

7-2 I/O Allocation Methods

7-2-1 I/O Allocations to Basic I/O Units

Basic I/O Units include the following Units:

- CS-series Basic I/O Units

These Units are allocated words in the I/O Area (CIO 0000 to CIO 0319) and can be mounted to the CPU Rack, and CS-series Expansion Racks.

Note Refer to *2-14 I/O Table Settings* for details.

Allocation Methods

When I/O tables are created in the order of the Racks and the order that Units are mounted, I/O words will be allocated as described below. If a Programming Console or the CX-Programmer is connected online and the I/O tables are created automatically according to the Units that are actually mounted, the CPU Unit will automatically create and register the I/O tables. If the I/O tables are created offline using the CX-Programmer, the CX-Programmer will automatically allocate words according to the Unit settings that have been made.

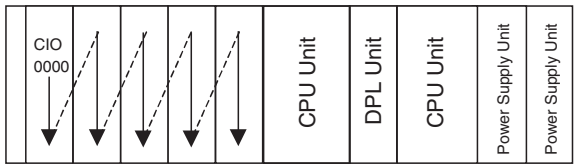
Basic I/O Units on the CPU Rack

Basic I/O Units on the CPU Rack are allocated words from left to right starting from CIO 0000 and each Unit is allocated as many words as it requires.

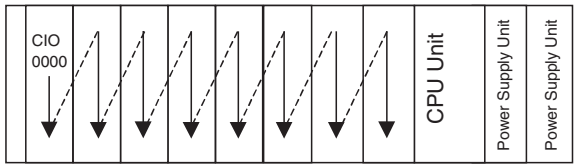
Note

1. Units that have 1 to 16 I/O points are allocated 16 bits (1 word) and Units that have 17 to 32 I/O points are allocated 32 bits (2 words).
2. I/O words are not allocated to empty slots. To allocate words to an empty slot, change the I/O table with a Programming Device.

Duplex CPU System, CPU Rack



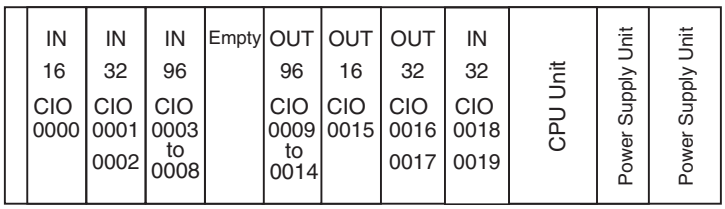
Single CPU System, CPU Rack



Example 1

The following example shows the I/O allocations to 4 Basic I/O Units on the CPU Rack with one empty slot.

Example for Single CPU System, CPU Rack



Example 2

The following example shows the I/O allocations to 5 Basic I/O Units in the CPU Rack. Two slots are filled with Dummy Units to reserve I/O words for those slots.

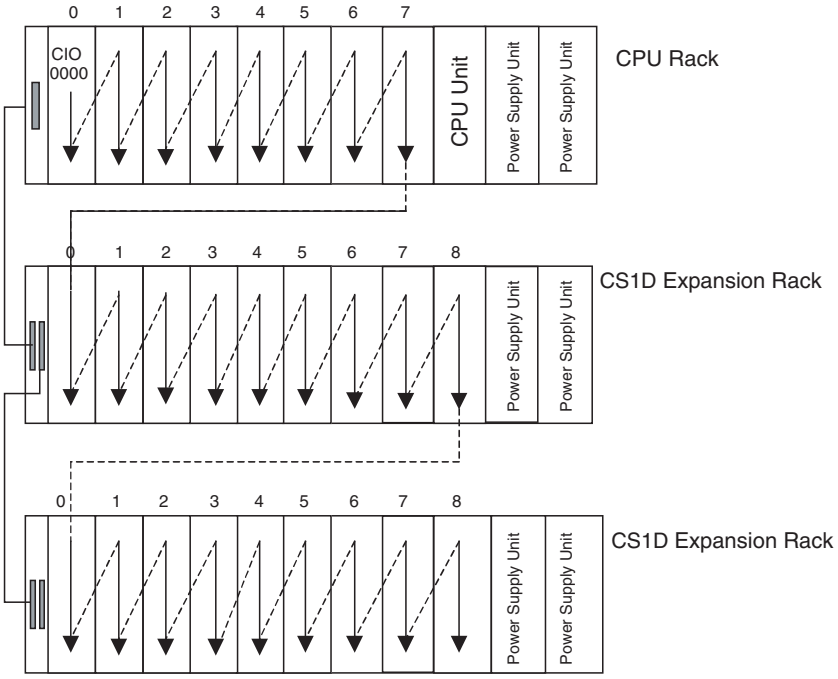
Example for Single CPU System, CPU Rack

	IN 16 CIO 0000	IN 32 CIO 0001 0002	IN 96 CIO 0003 to 0008	Re-served 16 CIO 0009	Re-served 32 CIO 0010 0011	OUT 16 CIO 0012	OUT 32 CIO 0013 0014	OUT 32 CIO 0015 0016	CPU Unit	Power Supply Unit	Power Supply Unit

Note Use the CX-Programmer's I/O table change operation to reserve words for the empty slots.

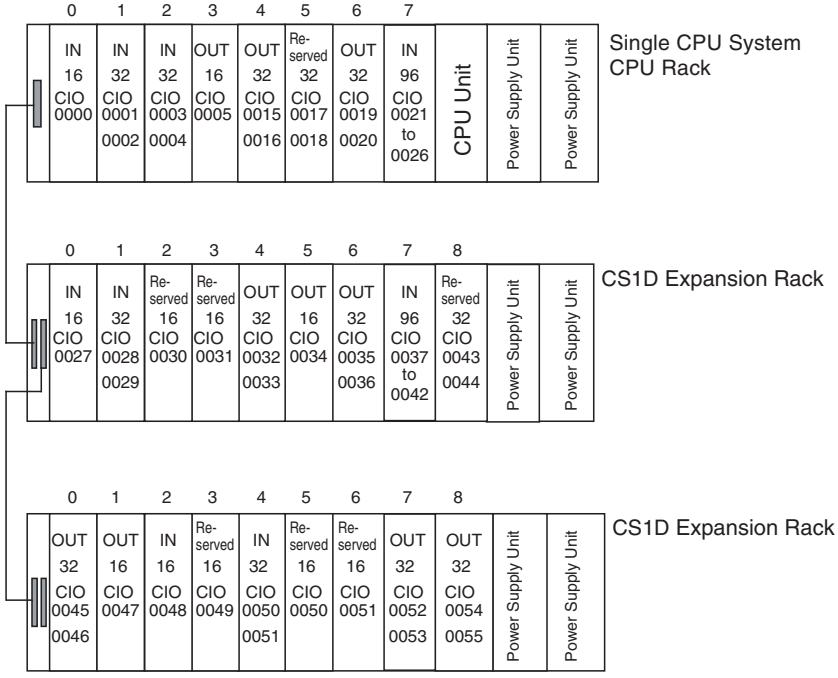
CS1D Expansion Racks

I/O allocation to Basic I/O Units continues from the CPU Rack to the Expansion Rack connected to the CPU Rack. Words are allocated from left to right and each Unit is allocated as many words as it requires, just like Units in the CPU Rack.



Example for Single CPU System

The following example shows the I/O allocation to Basic I/O Units in the CPU Rack and two CS-series Expansion Racks.



Note Use the CX-Programmer's I/O table change operation to reserve a word for the empty slot.

Allocations to CS-series Long-distance Expansion Racks

In configurations containing CS-series Long-distance Expansion Racks, up to two series of CS-series Long-distance Expansion Racks can be included. Words are automatically allocated to the Units mounted to the Racks in order of rack number and slot in the same way as for other configurations. The CPU Rack is rack 0, the CS-series Expansion Rack (if there is one) is Rack 1. Rack numbers are then assigned in order to the Racks in series A of CS-series Long-distance Expansion Racks and finally to the Racks in series B of CS-series Long-distance Expansion Racks, to a maximum rack number of 7. Although words are automatically allocated, the first word on each Rack can be set.

Note

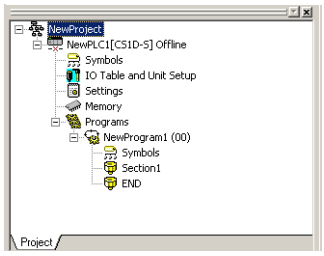
1. I/O words are not allocated to the I/O Control Units or I/O Interface Units.
2. No C200H Units of any kind can be mounted to CS-series Long-distance Expansion Racks.
3. CS-series CPU Bus Units should always be placed on the CPU Rack or CS-series Expansion Rack. Although they can be placed on CS-series Long-distance Expansion Racks, doing so is not recommended because it will increase the cycle time.

Reserving I/O Words for Expected Changes

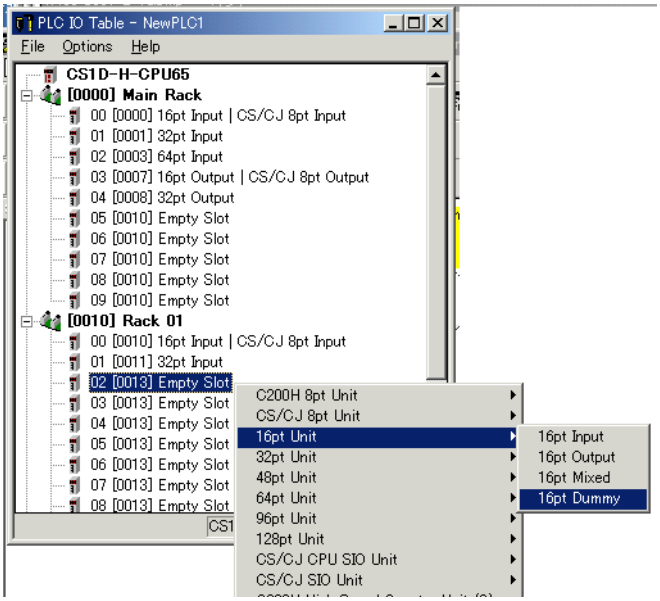
If the system configuration will be changed at a later date, changes to the program can be minimized by reserving I/O words in advance for future Unit changes or additions. To reserve I/O words, edit the I/O table with the CX-Programmer.

I/O Table Editing Operation

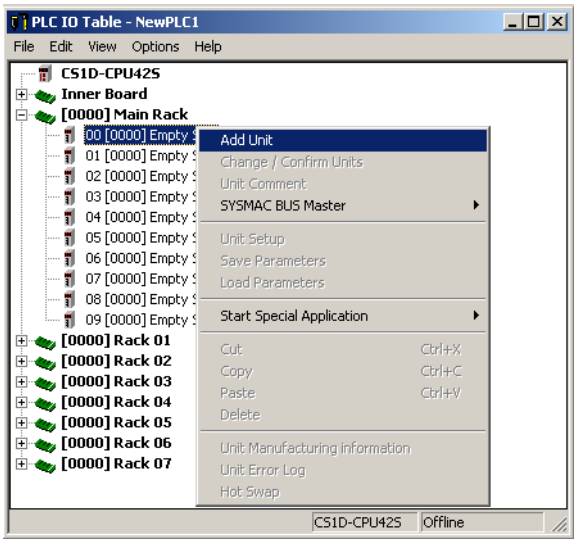
Double-click ***IO Table*** in the project tree in the main window. The I/O Table Window will be displayed.



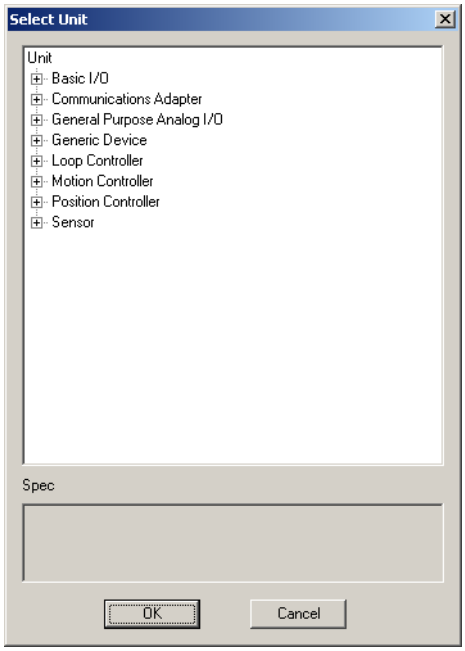
- CX-Programmer Ver. 5.0 or Earlier
  Right-click the slot for which a word is to be reserved and select the *Dummy* item from under the Basic I/O Unit with the correct number of I/O points.



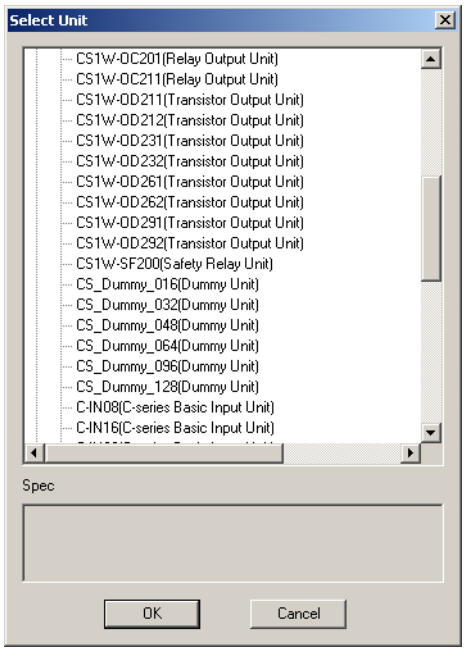
- CX-Programmer Ver. 6.0 or Later
  Right-click the slot for which a word is to be reserved and select ***Add Unit*** (alternatively, double-click the empty slot).



The following Select Unit Dialog Box will be displayed.



Click the expansion button (+) to the left of *Basic I/O*, select one of the Dummy Units *(CS_Dummy_016/032/048/064/096/128*), and click the **OK** Button.



Note Do not execute the I/O table creation operation after completing the above editing operation. The reserved word settings will be lost.

7-2-2 I/O Allocations to Special I/O Units

Special I/O Units include the following Units:

- CS-series Special I/O Units

Each of these Units is allocated ten words in the Special I/O Unit Area (CIO 2000 to CIO 2959) according the unit number set on the Unit.

Special I/O Units can be mounted to the CPU Rack, CS-series Expansion Racks (see note).

Note Refer to *2-14 I/O Table Settings* for more details on the available Special I/O Units.

Word Allocation

The following table shows which words in the Special I/O Unit Area are allocated to each Unit according to unit number.

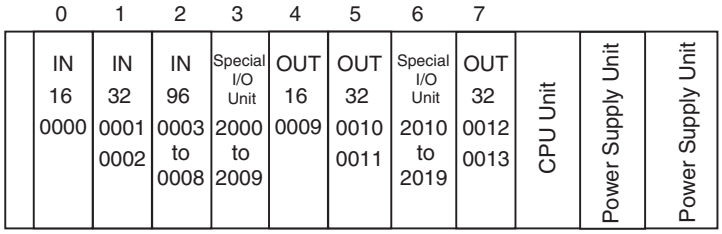
Unit number	Words allocated
0	CIO 2000 to CIO 2009
1	CIO 2010 to CIO 2019
2	CIO 2020 to CIO 2029
:	:
15	CIO 2150 to CIO 2159
:	:
95	CIO 2950 to CIO 2959

Special I/O Units are ignored during I/O allocation to Basic I/O Units. Slots containing Special I/O Units are treated as empty slots and aren't allocated any words in the I/O Area.

Example

The following example shows the I/O word allocation to Basic I/O Units and Special I/O Units in the CPU Rack of a Single CPU System.

Single CPU System, CPU Rack



Slot	Unit	Model number	Words required	Words allocated	Unit number	Group
0	16-point DC Input Unit	CS1W-ID211	1	CIO 0000	---	Basic I/O Unit
1	32-point DC Input Unit	CS1W-ID231	2	CIO 0001 and CIO 0002	---	Basic I/O Unit
2	96-point DC Input Unit	CS1W-ID291	6	CIO 0003 to CIO 0008	---	Basic I/O Unit
3	Analog Input Unit	CS1W-AD081-V1	10	CIO 2000 to CIO 2009	1	Special I/O Unit
4	16-point Transistor Output Unit	CS1W-OD211	1	CIO 0009	---	Basic I/O Unit
5	32-point Transistor Output Unit	CS1W-OD232	2	CIO 0010 and CIO 0011	---	Basic I/O Unit
6	8-point Analog Output Unit	CS1W-DA08C	10	CIO 2010 to CIO 2019	2	Special I/O Unit
7	32-point Transistor Output Unit	CS1W-OD232	2	CIO 0012 and CIO 0013	---	Basic I/O Unit

7-2-3 I/O Allocations to CPU Bus Units

Each CPU Bus Unit is allocated 25 words in the CPU Bus Unit Area (CIO 1500 to CIO 1899) according the unit number set on the Unit. CPU Bus Units can be mounted to the CPU Rack or CS-series Expansion Racks.

Word Allocations

The following table shows which words in the CS-series CPU Bus Unit Area are allocated to each Unit.

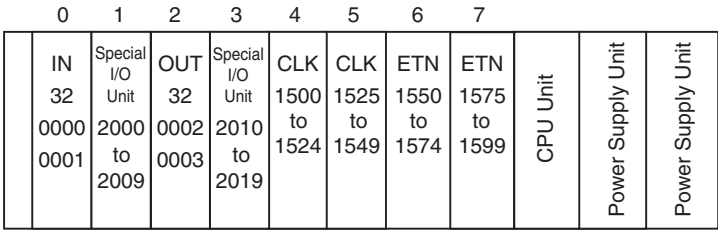
Unit number	Words allocated
0	CIO 1500 to CIO 1524
1	CIO 1525 to CIO 1549
2	CIO 1550 to CIO 1574
:	:
15	CIO 1875 to CIO 1899

CS-series CPU Bus Units are ignored during I/O allocation to Basic I/O Units. Slots containing CS-series CPU Bus Units are treated as empty slots and aren't allocated any words in the I/O Area.

Example

The following example shows the I/O word allocation to Basic I/O Units, Special I/O Units, and CS-series CPU Bus Units in the CPU Rack of a Single CPU System.

Single CPU System, CPU Rack



Slot	Unit	Model number	Words required	Words allocated	Unit number	Group
0	32-point DC Input Unit	CS1W-ID231	2	CIO 0000 and CIO 0001	---	Basic I/O Unit
1	Analog Input Unit	CS1W-AD081	10	CIO 2000 to CIO 2009	0	Special I/O Unit
2	32-point Transistor Output Unit	CS1W-SCU21	2	CIO 0002 and CIO 0003	---	Basic I/O Unit
3	Analog Output Unit	CS1W-DA08C	10	CIO 2000 to CIO 2009	1	Special I/O Unit
4	Controller Link Unit	CS1W-CLK11	25	CIO 1500 to CIO 1524	0	CPU Bus Unit
5	Controller Link Unit	CS1W-CLK11	25	CIO 1525 to CIO 1549	1	CPU Bus Unit
6	Ethernet Unit	CS1W-ETN21	25	CIO 1550 to CIO 1574	2	CPU Bus Unit
7	Ethernet Unit	CS1W-ETN21	25	CIO 1575 to CIO 1599	3	CPU Bus Unit

7-3 Allocating First Words to Racks

In the CS-series PLCs, the first word allocated to each Rack can be set with the CX-Programmer's I/O table edit operation. For example, the CPU Rack can be set to be allocated words starting with CIO 0000; the next Rack, words starting with CIO 0100; the next Rack, words starting with CIO 0200; etc. This can make it easier to check word allocations to Units without calculating all the way from the CPU Rack.

Note The first words for Racks cannot be set at the same time as the first words for slots.

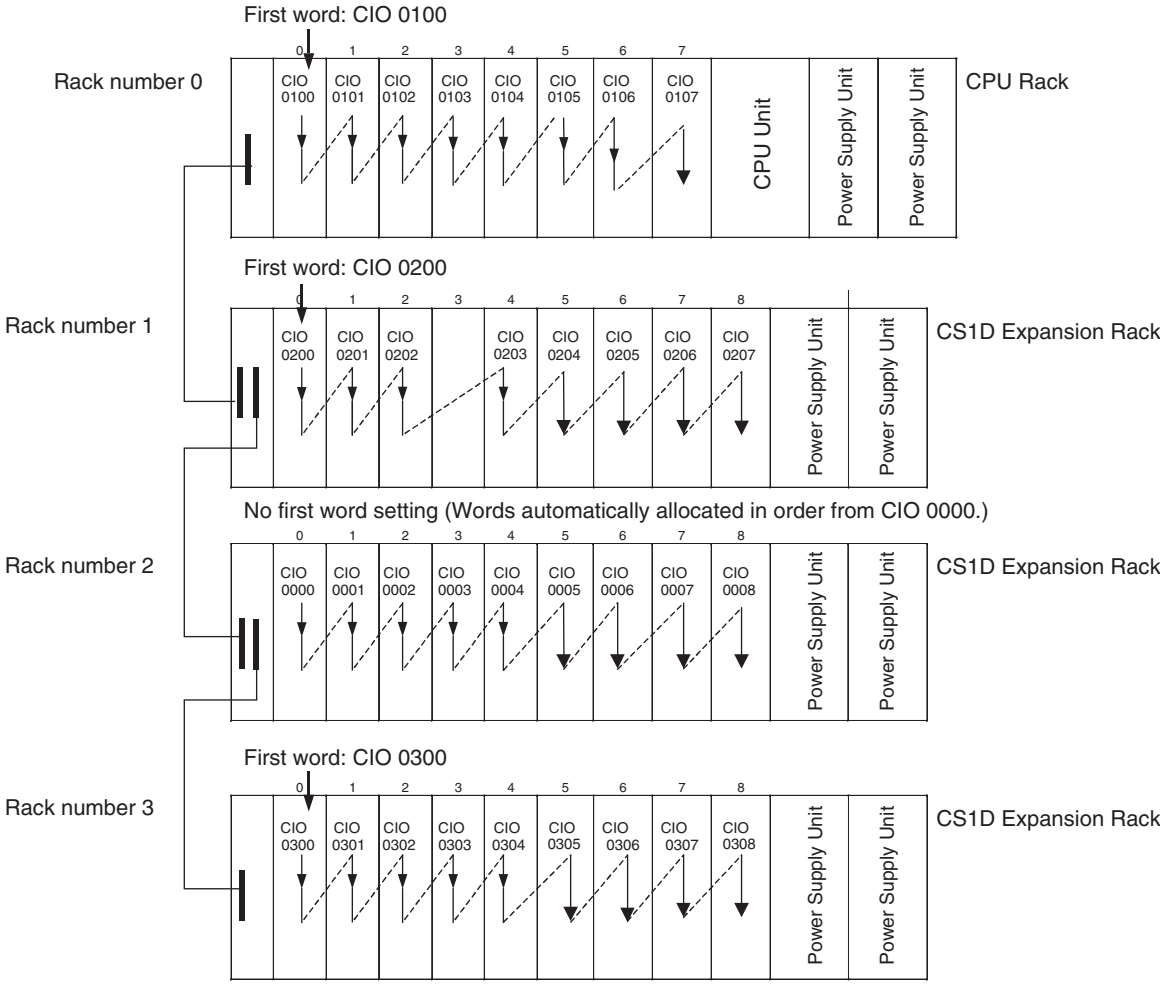
Word Allocations

For Racks in which the first word address has been set, words are allocated to Units in the order that the Units are mounted (from left to right) beginning with the specified first word. Words are not allocated to empty slots.

For Racks in which the first word address has not been set, words are allocated in rack-number order (lowest to highest) continuing from the last word allocated to the previous rack and starting with CIO 0000 on the first Rack for which the first word is not set.

Example: Setting the First Words for Racks

In this example, the first words have been set for Racks 0 (the CPU Rack), 2, and 3. For simplicity, only 16-bit Units have been used.



Rack First Word Settings

Rack	First word
CPU Rack	CIO 0100
Rack 1	CIO 0200
Rack 2	Not set
Rack 3	CIO 0300

Note Rack numbers (0 to 7) are fixed according to the order that the Racks are physically connected with cable. The CPU Rack is always Rack 0 and the other Racks are, in order, Racks 1 to 7. These numbers cannot be changed. In the above example, the shaded Racks are allocated words starting from

the specified first words. The non-shaded Racks are allocated in order from left to right and in order of Rack starting from CIO 0000.

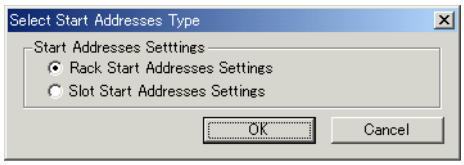
Setting First Rack Words from the CX-Programmer

The first word allocated on each Rack can be set from the CX-Programmer. These settings are not possible from a Programming Console.

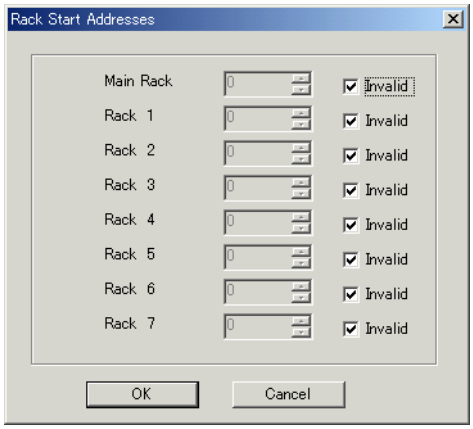
Note For CS1-H CPU Units, an indication of whether or not the first rack words have been set will be displayed on a Programming Console.

Use the following procedure to set the first rack words.

1,2,3... 1. Select the ***Rack/Slot Start Addresses*** from the Option Menu on the I/O Table Window. The following dialog box will be displayed.



2. Select the *Rack Start Addresses Settings* Option and click the **OK** Button.
3. In the dialog box that will appear, remove the checkmarks from the settings disabling the first rack word settings and set the address of the first words for the CPU Rack and Expansion Racks (1 to 7).



Setting	Setting range	Default	Remarks
Rack Start Address	0 to 9000	0	Same for all Racks
Invalid	Selected or cleared	Selected (invalid)	

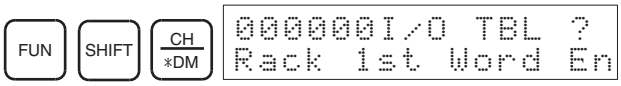
4. Click the **OK** Button.

Note Up to 8 Racks can be set for any CPU Unit model.

Confirming First Rack Word Settings on a Programming Console

With a CS1-H CPU Unit, the Programming Console can be used to check whether or not the first word has been set on a Rack. Use the following procedure.

1,2,3... 1. Press the **FUN**, **SHIFT**, and **CH** Keys to start the I/O table creation operation. If the first work for a Rack has been set, a message saying so will appear on the second line of the display.



If nothing is displayed, then a first word has not been set.

2. Press the **CHG** Key, enter the password (9713), and then press the **WRITE** Key to continue creating the I/O tables, or press the **CLR** Key to cancel the operation and return to the initial display.

Precautions in Setting Rack First Words

- Be sure to make first word settings so that allocated words do not overlap. The first word setting for a rack can be any address from CIO 0000 to CIO 0900. If the same word is allocated to two Racks, the I/O tables cannot be created and the Duplication Error Flag (A26103) in the I/O Table Error Information will turn ON.
- Always register the I/O table after installing an I/O Unit, after setting a rack number, or after setting the first word allocation for a Rack. The I/O Table Registration operation registers the I/O words allocated to the Racks.
- I/O words will not be allocated to empty slots. If an I/O Unit will be installed later, reserve words for the empty slot by changing the I/O table with a Programming Device's I/O Table Change Operation.
- If the actual system configuration is changed after registering the I/O table so that the number of words or I/O type does not match the I/O table, an I/O verification error (A40209) or I/O setting error (A40110) will occur. A CS-series CPU Bus Unit Setting Error (A40203) or Special I/O Unit Setting Error (A40202) may occur as well.
- When a Unit is removed, words can be reserved for the missing Unit using the I/O Table Change Operation. If a Unit is changed or added, all of the words in the program following that Unit's allocated words will be changed and the I/O Table Registration Operation will have to be performed again.

7-4 Allocating First Words to Slots (Single CPU Systems Only)

With a Single CPU System, the first word allocated to a slot on any Rack can be set with the CX-Programmer's I/O table edit operation regardless of the position of the slot. This feature can be used whenever it's necessary to control allocations to specific Units, e.g., to group allocated I/O words by device or circuit.

The first word can be set for up to 64 slots.

Note The first words for slots cannot be set at the same time as the first words for Racks.

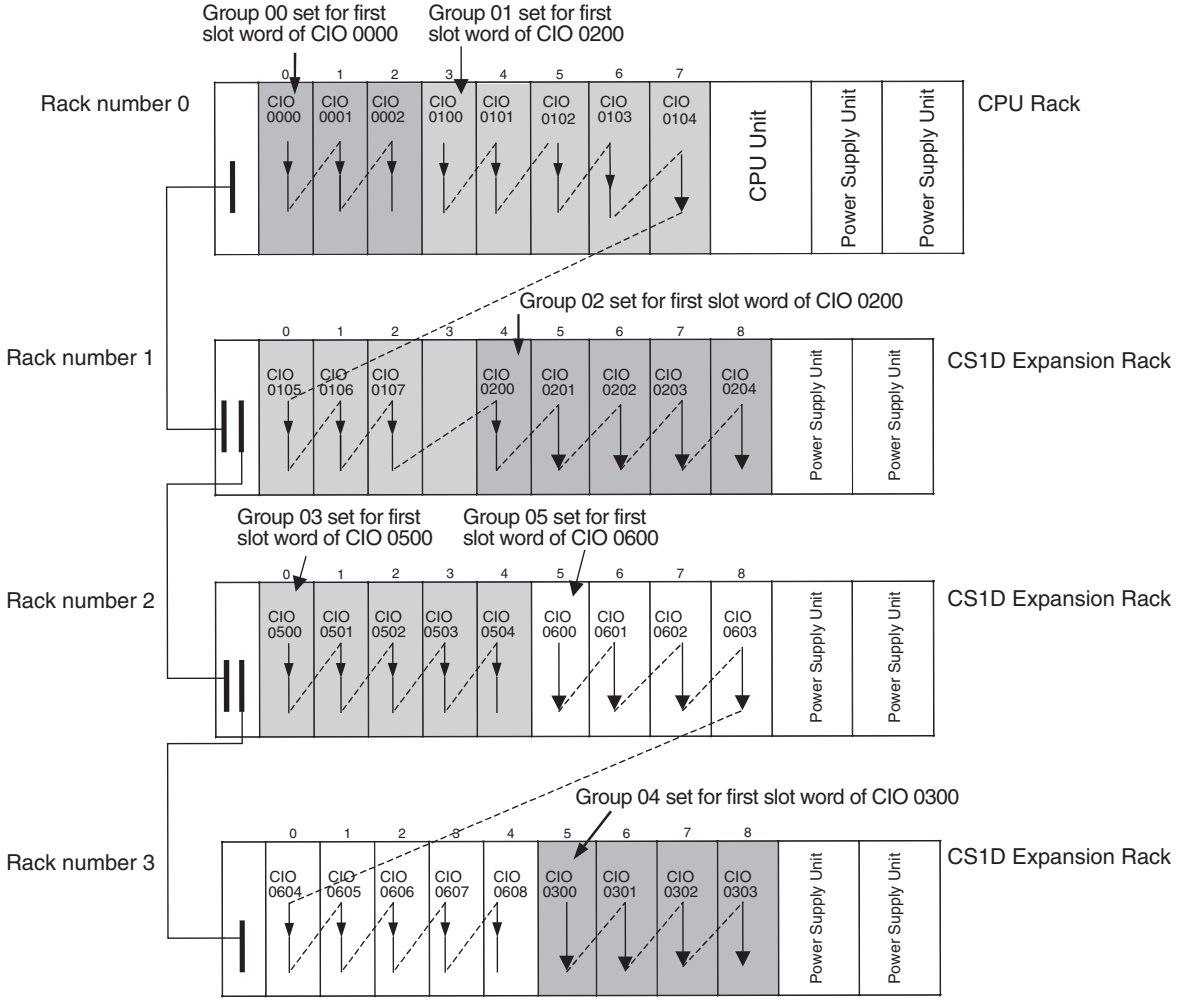
Word Allocations

When setting first words for slots, the first word must be set for slot 00 on the CPU Rack. The first word can then be set for any slot on any Rack for up to 63 other slots.

Each first word set for a slot creates a group starting with that slot. Words are allocated starting from the specified word to the first slot in the group and continuing left to right allocating consecutive words to each Unit until the next group (i.e., until the next Unit for which a first slot word is set). The next group can start on the same Rack or on a following Rack.

Example: Setting the First Words for Racks

In this example, a first slot word has been set in the middle of each Rack. For simplicity, only 16-bit Units have been used.



First Slot Word Settings

Group	Rack	Slot	Word
00 (See note.)	CPU Rack	00	CIO 0000
01	CPU Rack	03	CIO 0100
02	Rack 1	04	CIO 0200
03	Rack 2	00	CIO 0500
04	Rack 3	05	CIO 0300
05	Rack 4	05	CIO 0600

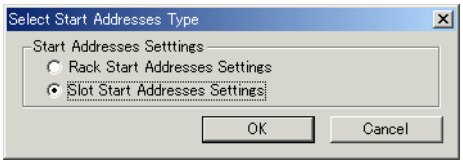
Note Group 00 must start at slot 00 on the CPU Rack. Any word can be set. Any slot can be set on any Rack for groups 01 to 63.

Setting First Slot Words from the CX-Programmer

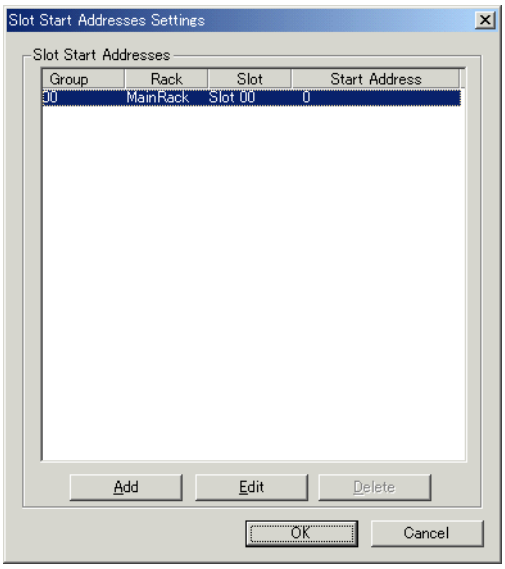
First slot words can be set from the CX-Programmer. These settings are not possible from a Programming Console.

1,2,3... 1. Select the ***Rack/Slot Start Addresses*** from the Option Menu on the I/O Table Window. The following dialog box will be displayed.

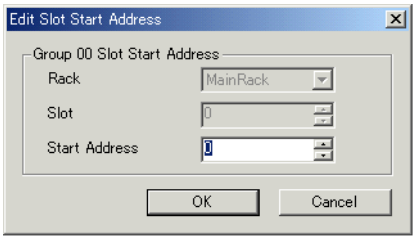
2. Select the *Slot Start Addresses Settings* Option and click the **OK** Button.



3. In the dialog box that will appear, set the first word for slot 00 on the CPU Rack.



4. To change the setting from CIO 0000, click the **Edit** Button. The follow dialog box will appear.



5. Set the desired word and click the **OK** Button.
6. To set slot first words for other groups, click the **Add** Button and make the appropriate settings for the Rack, slot, and word.

Setting	Setting range	Default	Remarks
Group	00 to 63	00	Groups numbers are allocated automatically in the order the groups are displayed and set.
Rack	CPU Rack (“MainRack”) Racks 1 to 7	CPU Rack	Group 00 always starts at slot 00 on the CPU Rack.
Slot	00 to 99	0	
First word	0 to 999	0	---

Precautions in Setting First Slot Words

When the I/O tables are edited, the CX-Programmer checks for any duplications in word allocations caused by first word settings. It is conceivable, however, that duplications in word allocations could occur after the I/O tables have been registered, e.g., as the result of replacing a 1-word Unit with a 2-word Unit. In this case the extra word needed by the new Unit would still also be allocated to the next Unit.

When the PLC is turned ON, the CPU Unit checks the registered I/O tables against the actual Units mounted to the PLC. If there are any duplications, and error will occur and it will be no longer possible to edit the I/O tables. If this happens, the I/O tables will have to be deleted and recreated or retransferred from a Programming Devices.

7-5 Detailed Information on I/O Table Creation Errors

With a CS1-H CPU Unit, the contents of A261 provides information on the Unit causing the error whenever one occurs when creating the I/O tables from the Programming Console or CX-Programmer. This information will make it easier to find the Unit causing the problem with troubleshooting I/O tables. Refer to *SECTION 10 Troubleshooting* for actual procedures.

Name	Address		Contents	When changing to RUN mode	At startup	Setting timing
	Word	Bit				
CPU Bus Unit Setup Area Initialization Error Flag	A261	00	ON: Error in CPU Bus Unit Setup Turns OFF when I/O tables are generated normally.	Held	Cleared	When I/O tables are created
I/O Overflow Flag		02	ON: Overflow in maximum number of I/O points. Turns OFF when I/O tables are generated normally.			
Duplication Error Flag		03	ON: The same unit number was used more than once. Turns OFF when I/O tables are generated normally.			
I/O Bus Error Flag		04	ON: I/O bus error Turns OFF when I/O tables are generated normally.			
SYSMAC BUS Recognition Error Flag		06	ON: SYSMAC BUS detection ended in an error. Turns OFF when I/O tables are generated normally.			
Special I/O Unit Error Flag		07	ON: Error in a Special I/O Unit Turns OFF when I/O tables are generated normally.			
I/O Unconfirmed Error Flag		09	ON: I/O detection has not been completed. Turns OFF when I/O tables are generated normally.			
Online Replacement Flag		10	ON: An online replacement operation is in progress.			
Duplex Communications Unit Error Flag		11	ON: Duplex Units are not mounted for a unit number specified for Duplex Communications Units (i.e., one Unit is missing or the mounted Units do not support duplex operation).			
Duplex Communications Unit Verification Error Flag		12	ON: The duplex setting in the PLC Setup for a unit number specified for Duplex Communications Units does not agree with the setting on the Duplex Communications Units. The I/O tables will not be created and an I/O Table Creation Error will occur. Refer to the Operation Manual for the Communications Units for details on Unit settings.			

7-6 Data Exchange with CPU Bus Units

This section describes how data can be exchanged between Special I/O Units or CS-series CPU Bus Units, and the CPU Unit.

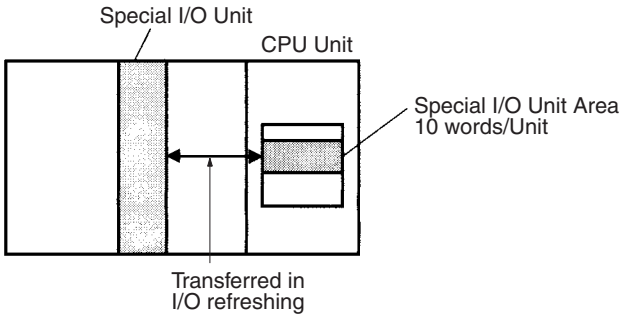
7-6-1 Special I/O Units

Special I/O Units include C200H Special I/O Units and CS-series Special I/O Units. Data can be exchanged between Special I/O Units and the CPU Unit through the Special I/O Unit Area, the DM Area, or FINS commands.

Special I/O Unit Area (I/O Refreshing)

Data is exchanged each cycle during I/O refreshing of the Special I/O Unit Area. Basically, 10 words are allocated to each Special I/O Unit based on its unit number setting. The number of words actually used by the Special I/O Unit varies; there are models that require 2 words, 4 words, and 20 words.

The Special I/O Unit Area ranges from CIO 2000 to CIO 2959 (10 words × 96 Units).



Transfer of Words Allocated in DM Area

C200H Special I/O Units

The 100 words allocated to each Unit are transferred from the DM Area to the Unit when the PLC is turned on or the Unit is restarted. Some C200H Special I/O Units do not use any of the allocated DM words and others use only a part of the allocated words.

CS-series Special I/O Units

There are three times that data may be transferred through the words allocated to each Unit. The timing of data transfers depends on the model being used.

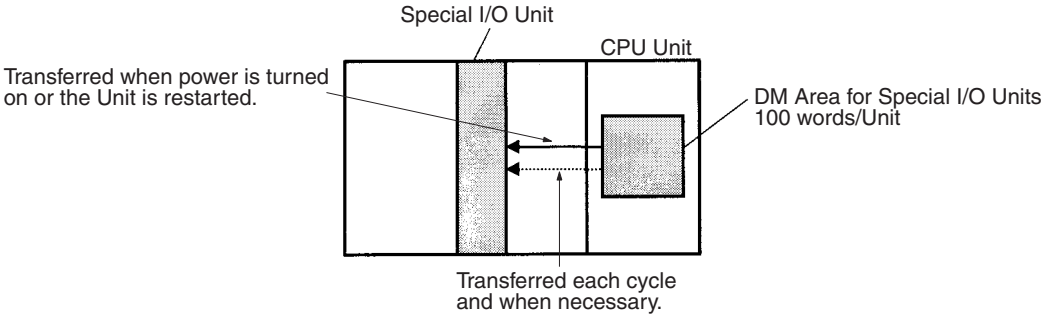
1,2,3...

1. Data transferred when the PLC is turned on.
2. Data transferred when the Unit is restarted.
3. Data transferred when necessary.

Some models transfer data in both directions, from the DM Area to the Unit and from the Unit to the DM Area. See the Unit's *Operation Manual* for details on data transfers.

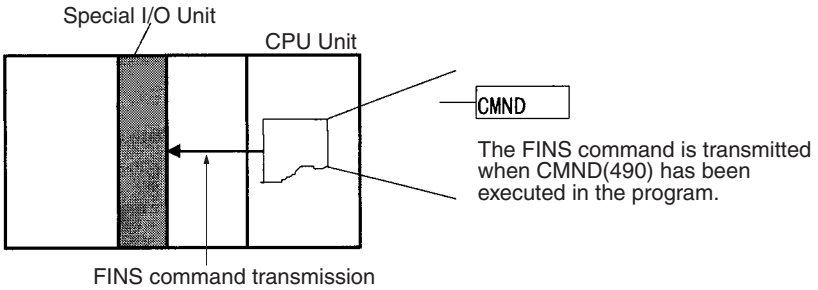
Special I/O Unit Words in the DM Area: D20000 to D29599 (100 Words x 96 Units)

Each Special I/O Unit is allocated 100 words in the DM Area in the range of D20000 to D29599 (100 words × 96 Units). These 100 words are generally used to hold initial settings for the Special I/O Unit. When the contents of this area are changed from the program to reflect a change in the system, the Restart Bits for affected Units must be turned ON to restart the Units.

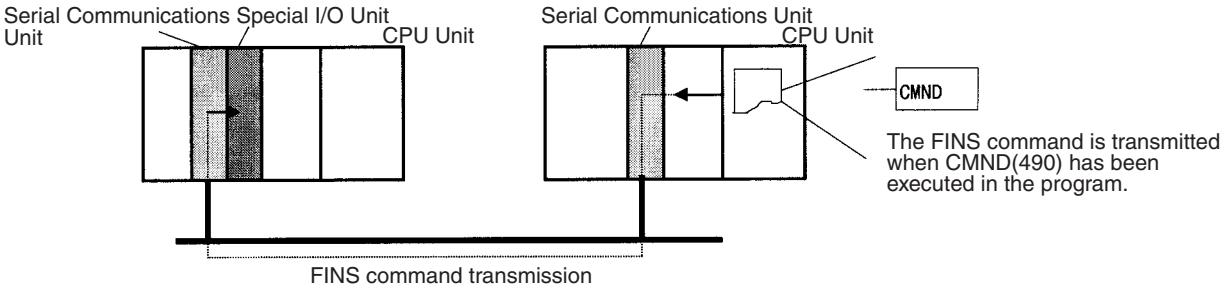


FINS Commands

The CMND(490) instruction can be added to the ladder program to issue a FINS command to the Special I/O Unit.



FINS commands can be transmitted to Special I/O Units in other PLCs in the network, not just the local PLC.



Special I/O Unit Initialization

Special I/O Units are initialized when the PLC's power is turned on or the Unit's Restart Bit is turned ON. The Unit's Special I/O Unit Initialization Flag (A33000 to A33515) will be ON while the Unit is initializing.

I/O refreshing (cyclic I/O refreshing or refreshing by IORF(097)) will not be performed for a Special I/O Unit while its Initialization Flag is ON.

7-6-2 Disabling Special I/O Unit Cyclic Refreshing

Ten words are allocated to each Special I/O Unit in the Special I/O Unit Area (CIO 2000 to CIO 2959) based on the unit number set on the front of each Unit. The data in the Special I/O Unit Area is refreshed in the CPU Unit every cycle during I/O refreshing (just after execution of the END(001) instruction).

I/O refreshing may take too long if too many Special I/O Units are installed. If I/O refreshing is taking too much time, the PLC Setup can be set to disable cyclic refreshing for particular Special I/O Units. (The Special I/O Unit Cyclic Refreshing Disable Bits are in PLC Setup addresses 226 to 231.)

If the I/O refreshing time is too short, the Unit's internal processing will not be able to keep pace, the Special I/O Unit Error Flag (A40206) will be turned ON, and the Special I/O Unit may not operate properly. In this case, the cycle time

can be extended by setting a minimum cycle time in the PLC Setup or cyclic I/O refreshing with the Special I/O Unit can be disabled. When cyclic refreshing has been disabled, the Special I/O Unit's data can be refreshed during program execution with IORF(097).

Note

1. Always disable a Special I/O Unit's cyclic refreshing if the Unit's I/O will be refreshed in an interrupt task with IORF(097). An interrupt task error (A40213) will occur if cyclic refreshing and IORF(097) refreshing are performed simultaneously.
2. Whenever disabling a Special I/O Unit's cyclic refreshing, be sure that the I/O for that Unit is refreshed with IORF(097) in the program at least every 11 seconds during operation. A CPU Unit service monitoring error will occur in the Special I/O Unit if it is not refreshed every 11 seconds.

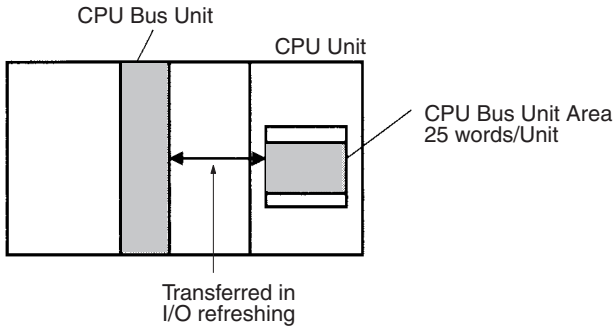
7-6-3 CPU Bus Units

Data can be exchanged between CPU Bus Units and the CPU Unit through the CPU Bus Unit Area, the DM Area, or FINS commands.

CPU Bus Unit Area (I/O Refreshing)

Data is exchanged each cycle during I/O refreshing of the CPU Bus Unit Area. Basically, 25 words are allocated to each CPU Bus Unit based on its unit number setting. The number of words actually used by the CPU Bus Unit varies.

The Special I/O Unit Area ranges from CIO 1500 to CIO 1899 (25 words × 16 Units).



Note With CS1-H CPU Units, the CPU BUS I/O REFRESH instruction (DLNK(226)) can be executed in the ladder program to refresh the CIO Area words allocated to the CPU Bus Unit of a specified unit number.

Transfer of Words Allocated in the DM Area

Each CPU Bus Unit is allocated 100 words in the DM Area in the range of D30000 to D31599 (100 words × 16 Units). There are three times that data may be transferred through the words allocated to each Unit. The timing of data transfers depends on the model being used.

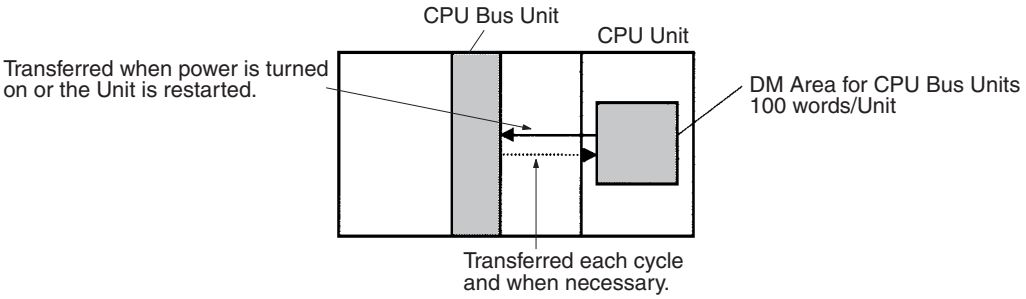
1,2,3...

1. Data transferred when the PLC is turned ON.
2. Data transferred each cycle.
3. Data transferred when necessary.

Note With CS1-H CPU Units, the CPU BUS I/O REFRESH instruction (DLNK(226)) can be executed in the ladder program to refresh the DM Area words allocated to the CPU Bus Unit of a specified unit number.

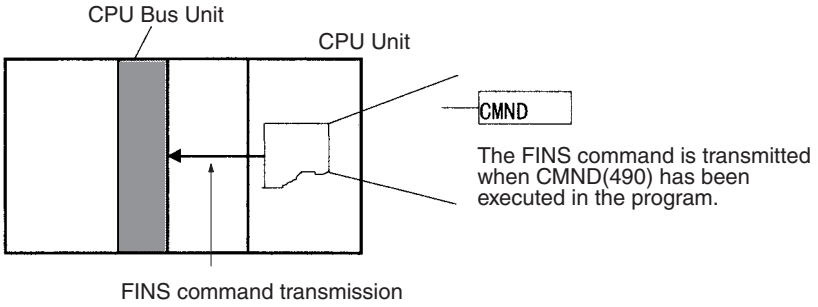
Some models transfer data in both directions, from the DM Area to the Unit and from the Unit to the DM Area. See the Unit's Operation Manual for details on data transfers.

These 100 words are generally used to hold initial settings for the CPU Bus Unit. When the contents of this area are changed from the program to reflect a change in the system, the Restart Bits (A50100 to A50115) for affected Units must be turned ON to restart the Units.

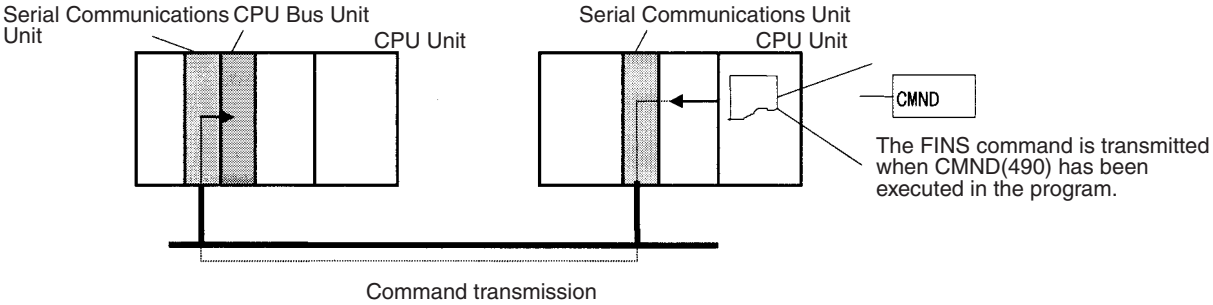


FINS Commands

The CMND(490) instruction can be added to the ladder program to issue a FINS command to the CPU Bus Unit.



FINS commands can be transmitted to CPU Bus Units in other PLCs in the network, not just the local PLC.



CPU Bus Unit Initialization

CPU Bus Units are initialized when the PLC's power is turned on or the Unit's Restart Bit is turned ON. The Unit's CPU Bus Unit Initialization Flag (A30200 to A30215) will be ON while the Unit is initializing.

Cyclic I/O refreshing will not be performed for a CPU Bus Unit while its Initialization Flag is ON.

7-7 Online Addition of Units and Backplanes

This function allows previously unregistered Units to be added and controlled during operation. Both Units and Expansion Racks can be added during operation.

Note

1. A Duplex CPU Unit with unit version 1.3 or later is required to add Units online. CPU Bus Units cannot be added online. Expansion Racks can be added online only in a Duplex CPU, Dual I/O Expansion System.
2. Both duplex Ethernet Units will be reset and communications will temporarily stop when I/O tables are created or transferred or Units are added online in a system that uses duplex Ethernet with the CS1D. Confirm that the system will not be adversely affected before executing these operations.

7-7-1 Conditions Required for Online Addition

Systems Supporting Online Addition

The following table shows the Units that can be added to each system.

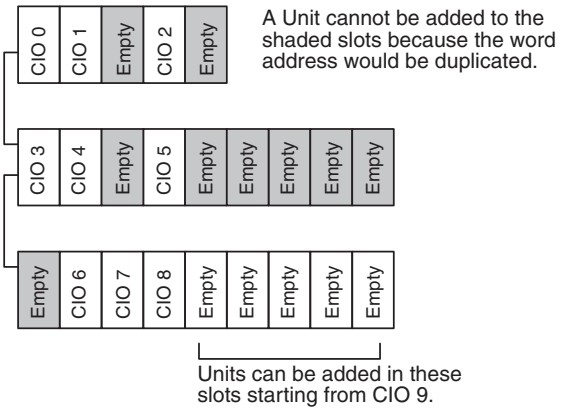
Operation	Duplex CPU, Dual I/O Expansion System	Duplex CPU, Single I/O Expansion System	Single CPU System
Online Unit addition	Supported	Supported	Not supported
Online Expansion Rack addition	Supported	Not supported (See note.)	Not supported (See note.)

Note With a Duplex CPU, Single I/O Expansion System or Single CPU System, the system may stop if an Expansion Rack is added.

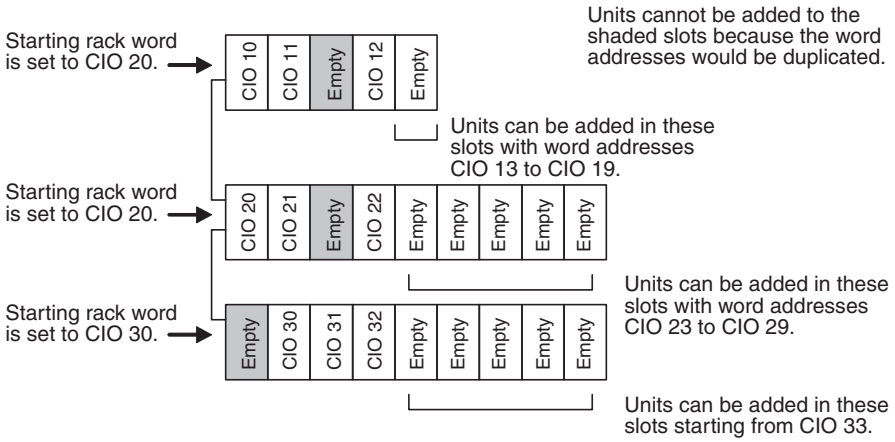
Online Addition of Basic I/O Units

When adding a Basic I/O Unit online, the new Unit's allocated words must not duplicate any words allocated to other Basic I/O Units that are already mounted. Add the new Unit to a slot position so that the allocated words will not be duplicated, as shown in the following diagrams.

- Creating the I/O Table using the Default Starting Words for each Rack



- Creating the I/O Table by setting the Starting Word for each Rack



Online Addition of Special I/O Units

When adding a Special I/O Unit online, the new Unit's allocated words must not duplicate any words allocated to other Special I/O Units that are already mounted. Add the new Unit to a slot position so that the allocated words will not be duplicated. There are no other restrictions on the slot position.

Online Addition of CPU Bus Units

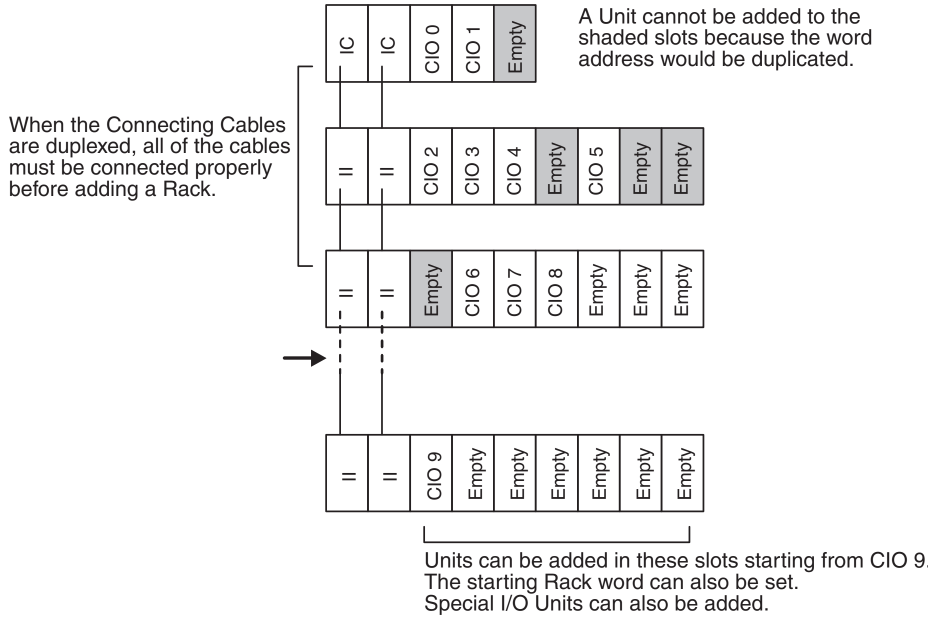
CPU Bus Units cannot be added online.

Online Addition of Expansion Backplanes

With a Duplex CPU Dual I/O Expansion System, Expansion Backplanes can be added in addition to Units. The Expansion Backplane being added must be a CS1D-BI082D Backplane with CS1D-II102D I/O Interface Units. The starting Rack word of the added Expansion Rack can be set.

When an Expansion Backplane is added, a Basic I/O Unit or Special I/O Unit must be mounted in the Backplane. The Expansion Backplane will not be added if it does not contain a Basic I/O Unit or Special I/O Unit.

When the Connecting Cables are duplexed, all of the Connecting Cable connections must be normal. The Expansion Backplane will not be added if there is even one Connecting Cable disconnected.



Maximum Number of Additional Units

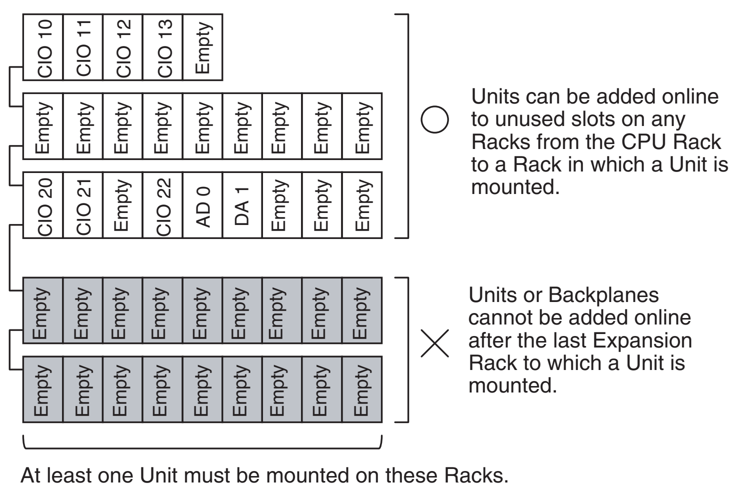
Only 1 Unit can be added at a time. When multiple Units are being added, add the Units one at a time.

Restrictions on Last Rack

At least one Unit must always be mounted.

If no Unit is mounted, Units cannot be added online and Backplanes cannot be added from the last Rack until the last Rack in which a Unit is mounted.

To add Units or Backplanes, the power supply must be cycled.



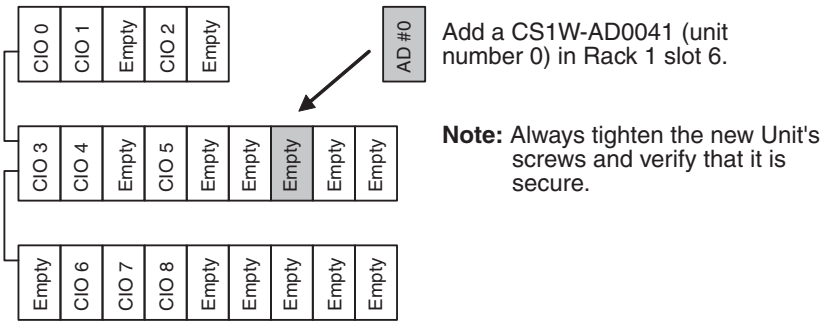
7-7-2 Online Addition Procedure

Units and Backplanes can be added online only from the CX-Programmer's I/O Table Window; they cannot be added online from a Programming Console.

Note The online addition function is supported by CX-Programmer Ver. 8.0 or later, or CX-Programmer Ver. 7.0 only when it has been added as an expansion function.

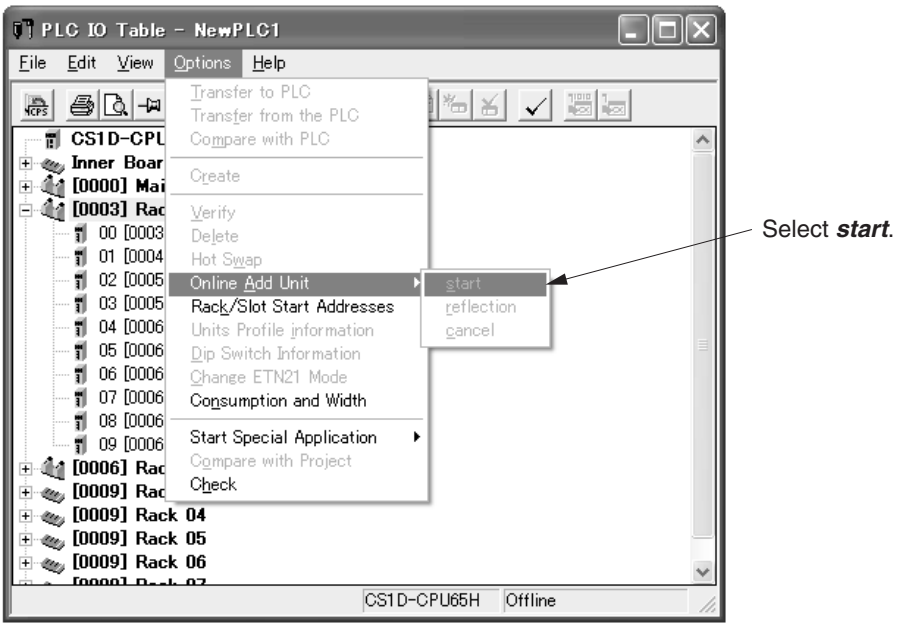
Online Addition of Units

1,2,3... 1. Mount the additional Unit in an empty slot.

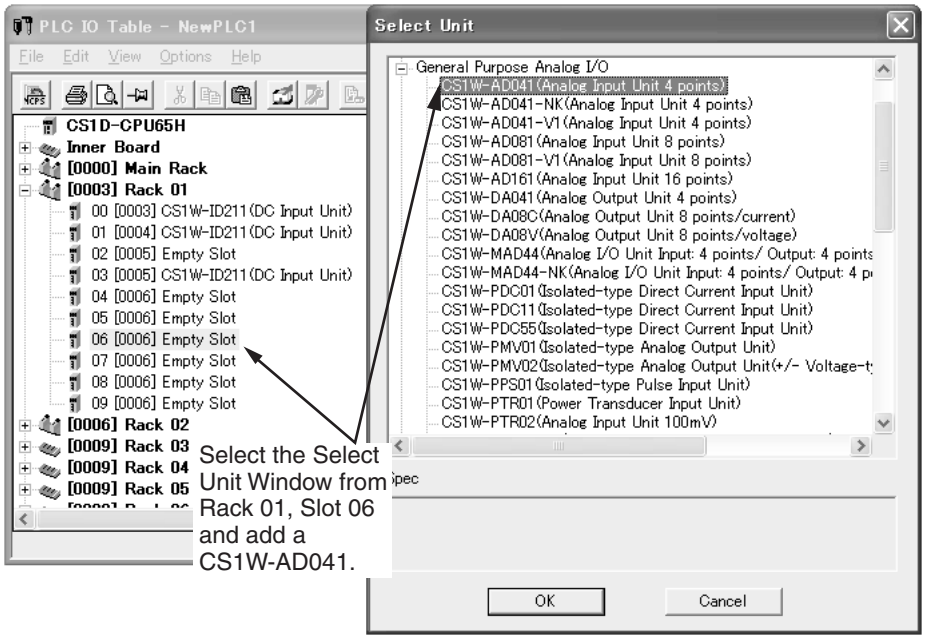


2. Connect the CX-Programmer to the CPU Unit and go online.
3. Display the I/O Table Window. The I/O table will be matched to the PLC's status. If the I/O table does not match, transfer the I/O table from the PLC to the computer.
4. Select ***Options - Online Add Unit - start***. At this point, the CX-Programmer will check whether the I/O table matches the PLC configuration.

Note If the I/O table does not match, the online addition will not be executed.

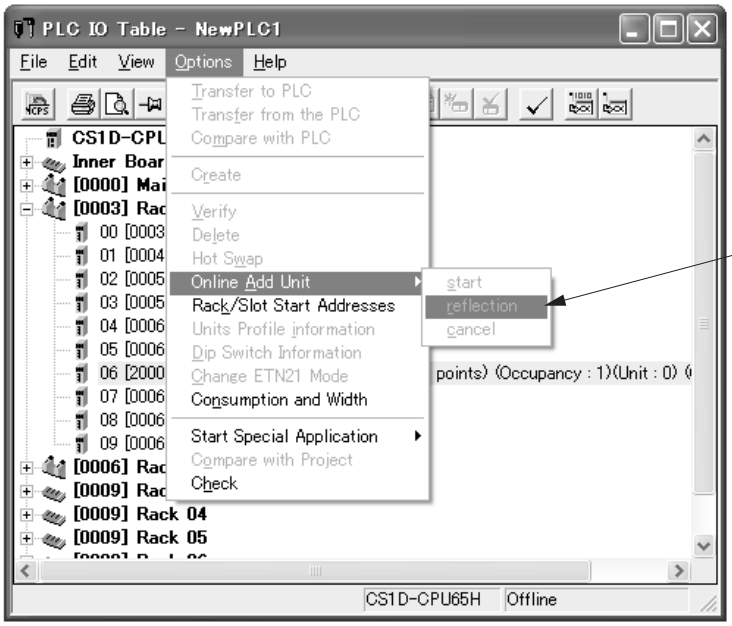


5. Right-click the Rack/slot in which the Unit will be added and select ***Add Unit*** from the pop-up menu.
   The Select Unit Window will be displayed. Select the Unit to add.



6. Select ***Options - Online Add Unit - reflection***. The Unit addition will be completed if the Unit selected in the CX-Programmer matches the Unit that was actually added.

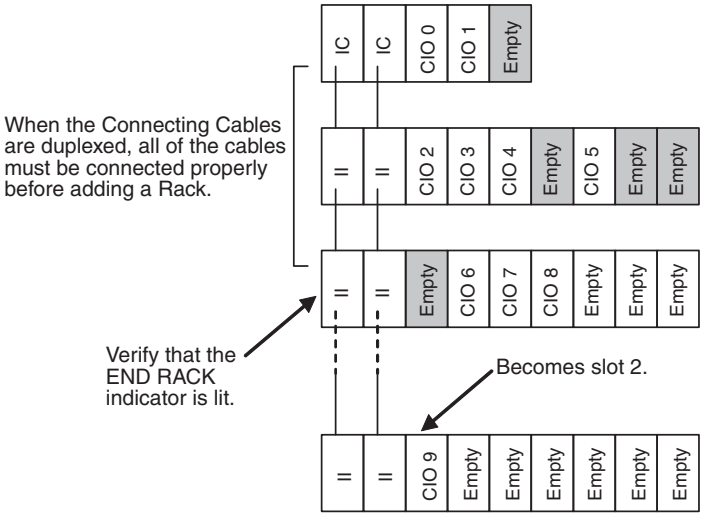
Note If the Unit does not match, the online addition will not be executed.



Online Addition of a Unit and Backplane

1,2,3... 1. Mount the additional Unit in the Expansion Backplane and connect the CS-series Connecting Cables to the operating PLC.

Note When the cables are duplexed, always verify that both cables are connected properly. When adding a Rack, also verify that the connecting Rack is the last Expansion Rack (or CPU Rack). Verify that the END RACK Indicator is lit in the Rack's CS1D I/O Control Unit or CS1D I/O Interface Unit.



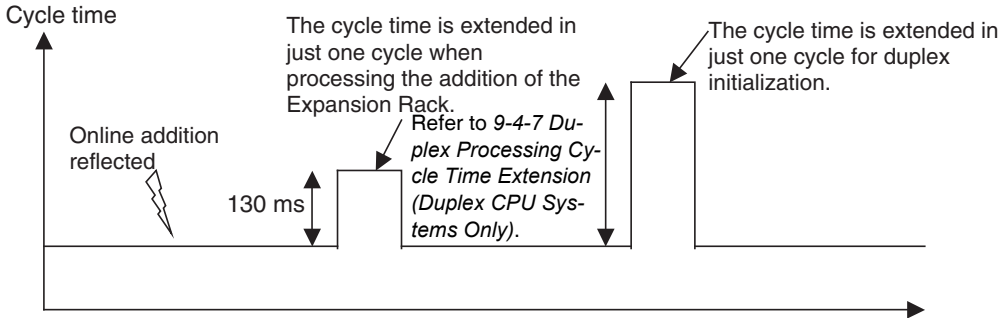
Note: When adding a Unit and Backplane, always tighten the screws and verify that the Unit is secure.

2. Turn ON the power supply to the Rack that was added.
3. Follow steps 2 to 6 in the above *Online Addition of Units* procedure to use the CX-Programmer to add the Unit.

7-7-3 Cycle Time Extension during Online Addition

The following table shows how much longer the cycle time will be during online addition of an Expansion Rack.

Operation	Cycle time extension	Remarks
Cycle time extension due to online addition of an Expansion Rack	130 ms	The cycle time will be longer while an Expansion Rack is being added. The cycle time will not be extended when only a Unit is being added.
Cycle time extension due to duplex initialization	For details, refer to *9-4-7 Duplex Processing Cycle Time Extension (Duplex CPU Systems Only)*.	The cycle time will be longer while a Unit or Expansion Rack is being added.



SECTION 8
Memory Areas

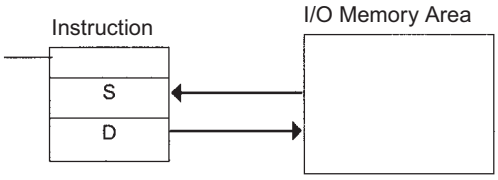
This section describes the structure and functions of the I/O Memory Areas and Parameter Areas.

8-1 Introduction

The CPU Unit's memory (RAM with battery back-up) can be divided into three parts: the User Program Memory, I/O Memory Area, and Parameter Area. This section describes the I/O Memory Area and Parameter Area.

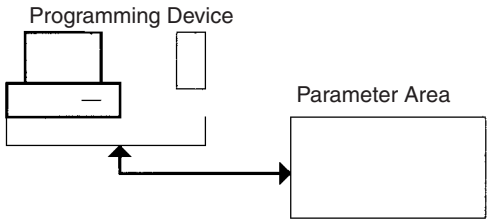
I/O Memory Area

This region of memory contains the data areas which can be accessed by instruction operands. The data areas include the CIO Area, Work Area, Holding Area, Auxiliary Area, DM Area, EM Area, Timer Area, Counter Area, Task Flag Area, Data Registers, Index Registers, Condition Flag Area, and Clock Pulse Area.



Parameter Area

This region of memory contains various settings that cannot be specified by instruction operands; they can be specified from a Programming Device only. The settings include the PLC Setup, I/O Table, Routing Table, and CPU Bus Unit settings.



8-2 I/O Memory Areas

8-2-1 I/O Memory Area Structure

The following table shows the basic structure of the I/O Memory Area.

Area		Size	Range	External I/O allocation	Bit access	Word access	Access		Change from Programming Device	Status at startup or mode change	Forcing bit status
							Read	Write			
CIO Area	I/O Area	5,120 bits (320 words)	CIO 0000 to CIO 0319 (See note 1.)	Basic I/O Units	OK	OK	OK	OK	OK	Cleared (See note 2.)	OK
	Data Link Area	3,200 bits (200 words)	CIO 1000 to CIO 1199	Data link	OK	OK	OK	OK	OK		OK
	CPU Bus Unit Area	6,400 bits (400 words)	CIO 1500 to CIO 1899	CPU Bus Units	OK	OK	OK	OK	OK		OK
	Special I/O Unit Area	15,360 bits (960 words)	CIO 2000 to CIO 2959	Special I/O Units	OK	OK	OK	OK	OK		OK
	Inner Board Area	1,600 bits (100 words)	CIO 1900 to CIO 1999	Inner Boards	OK	OK	OK	OK	OK		OK
	CS-series DeviceNet Area	9,600 bits (600 words)	CIO 3200 to CIO 3799	DeviceNet Slaves	OK	OK	OK	OK	OK		OK
	Internal I/O Areas	37,504 bits (2,344 words) 4,800 bits (300 words)	CIO 1200 to CIO 1499 CIO 3800 to CIO 6143	---	OK	OK	OK	OK	OK		OK
Work Area		8,192 bits (512 words)	W000 to W511	---	OK	OK	OK	OK	OK		OK
Holding Area(See note 3.)		8,192 bits (512 words)	H000 to H511	---	OK	OK	OK	OK	OK	Maintained	OK
Auxiliary Area		15,360 bits (960 words)	A000 to A447	---	OK	OK	OK	No	No	Varies from address to address.	No
			A448 to A959					OK	OK		
TR Area		16 bits	TR0 to TR15	---	OK	---	OK	OK	No	Cleared	No

Area	Size	Range	External I/O allocation	Bit access	Word access	Access		Change from Programming Device	Status at startup or mode change	Forcing bit status
						Read	Write			
DM Area	32,768 words	D00000 to D32767	---	No (See note 4.)	OK	OK	OK	OK	Maintained	No
EM Area	32,768 words per bank (0 to 18, 25 max.)	E0_00000 to E18_32767	---	No (See note 4.)	OK	OK	OK	OK	Maintained	No
Timer Completion Flags	4,096 bits	T0000 to T4095	---	OK	---	OK	OK	OK	Cleared (See note 2.)	OK
Counter Completion Flags	4,096 bits	C0000 to C4095	---	OK	---	OK	OK	OK	Maintained	OK
Timer PVs	4,096 words	T0000 to T4095	---	---	OK	OK	OK	OK	Cleared (See note 2.)	No (See note 6.)
Counter PVs	4,096 words	C0000 to C4095	---	---	OK	OK	OK	OK	Maintained	No (See note 7.)
Task Flag Area	32 bits	TK00 to TK31	---	OK	---	OK	No	No	Cleared	No
Index Registers (See note 5.)	16 registers	IR0 to IR15	---	OK	OK	Indirect addressing only	Specific instructions only	No	Cleared (See note 2.)	No
Data Registers (See note 5.)	16 registers	DR0 to DR15	---	No	OK	OK	OK	No	Cleared (See note 2.)	No

Note

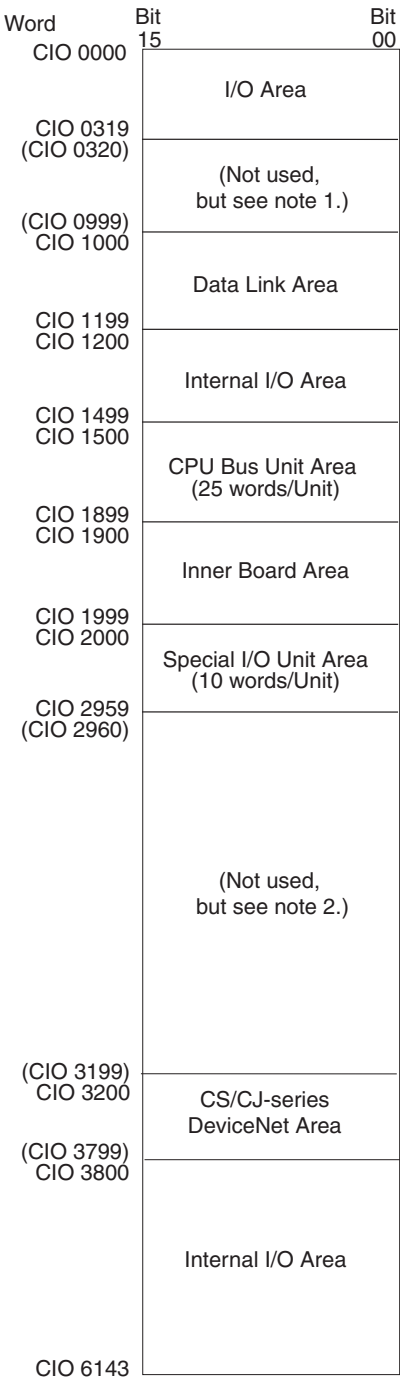
1. The I/O Area can be expanded to CIO 0000 to CIO 0999 by changing the first words allocated to Racks.
2. If the IOM Hold Bit (A50012) is ON, the content of these words will be held even if the operating mode is changed.
   If the PLC Setup's "IOM Hold Bit Status at Startup" setting is also set to protect the IOM Hold Bit, the contents of the I/O Area won't be cleared when the PLC's power supply is cycled OFF and ON again.
3. H512 to H1535 are Function Block Holding Area words.
   They can be set only in the FB instance area (internally-assigned range of variables).
4. Bits in the DM Area and EM Area can be manipulated using TST(350), TSTN(351), SET, SETB(532), RSTB(533), OUTB(534).
5. Index registers and data registers can be used either individually by task or they can be shared by all the tasks.
6. Timer PVs can be refreshed indirectly by forced setting/resetting Timer Completion Flags.
7. Counter PVs can be refreshed indirectly by forced setting/resetting Counter Completion Flags.

8-2-2 Overview of the Data Areas

The data areas in the I/O Memory Area are described in detail below.

CIO Area

It isn't necessary to input the "CIO" acronym when specifying an address in the CIO Area. The CIO Area is generally used for data exchanges such as I/O refreshing with various Units. Words that aren't allocated to Units may be used as work words and work bits in the program only.



Note

1. It is possible to use CIO 0320 to CIO 0999 for I/O words by making the appropriate settings for the first words on the Racks. Settings for the first words on the Racks can be made using the CX-Programmer to set the first Rack addresses in the I/O table. The settings range for the first Rack addresses is from CIO 0000 to CIO 0900.
2. The parts of the CIO Area that are labelled “Not used” may be used in programming as work bits. In the future, however, unused CIO Area bits may be used when expanding functions. Always use Work Area bits first.

I/O Area

These words are allocated to external I/O terminals on Basic I/O Units. Words that aren’t allocated to external I/O terminals may be used only in the program.

Link Area

Words in the Link Area are used for data links when *LR* is set as the data link area for automatic allocation for Controller Link Networks. It is also used for PLC Links. Words in the Link Area can be used in the program when *LR* is not set as the data link area for Controller Link Networks and PLC Links are not used.

CPU Bus Unit Area

These words are allocated to CPU Bus Units to transfer status information. Each Unit is allocated 25 words and up to 16 Units (with unit numbers 0 to 15) can be used. Words that aren't used by CPU Bus Units may be used only in the program.

Special I/O Unit Area

These words are allocated to Special I/O Units. Each Unit is allocated 10 words and up to 96 Units (unit numbers 0 to 95) can be used.
Words that aren't used by Special I/O Units may be used only in the program.

Inner Board Area

These words are allocated to Inner Boards such as Communications Boards. Up to 100 words can be allocated for input and output.

Note The Inner Board Area is used for Inner Boards only in Single CPU Systems or for the Inner Boards in a Process-control CPU Units in Duplex CPU Systems.

CS-series DeviceNet Area

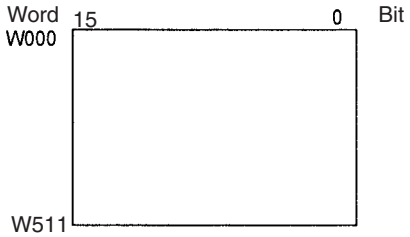
These words are allocated to Slaves for DeviceNet Remote I/O Communications for CS-series DeviceNet Units (CS1W-DRM21). Allocations are fixed and cannot be changed. Be sure that allocates to not overlap with those used for other I/O points.

Internal I/O Area

These words can be used only in the program; they cannot be used for I/O exchange with external I/O terminals. Be sure to use the work words provided in the Work Area (WR) before allocating words in the Internal I/O Area or other unused words in the CIO Area. It is possible that these words will be assigned to new functions in future versions of CS1D CPU Units, so the program may have to be changed before being used in a new CS1D PLC if CIO Area words are used as work words in the program.

Work Area (WR)

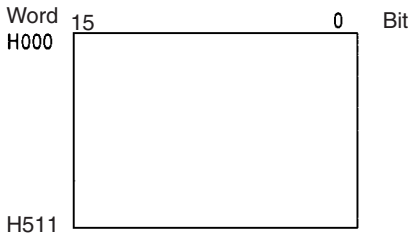
Words in the Work Area can be used only in the program; they cannot be used for I/O exchange with external I/O terminals. No new functions will be assigned to this area in future versions of CS1D PLCs, so use this area for work words and bits before any words in the CIO Area.



Holding Area (HR)

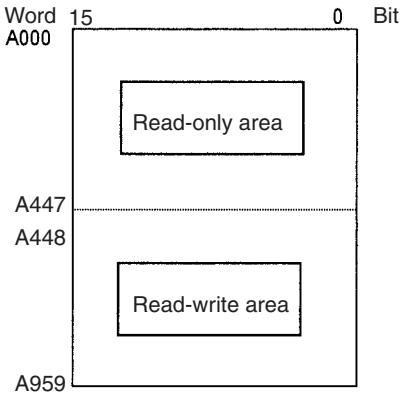
Words in the Holding Area can be used only in the program. These words retain their content when the PLC is turned ON or the operating mode is switched between PROGRAM mode and RUN or MONITOR mode.

Note H512 to H1535 are Function Block Holding Area words. They can be set only in the FB instance area (internally-assigned range of variables). Note that they cannot be specified as the operand of the instructions on the user program.



Auxiliary Area (AR)

The Auxiliary Area contains flags and control bits used to monitor and control PLC operation. This area is divided into two parts: A000 to A447 are read-only and A448 to A959 can be read or written. Refer to *8-11 Auxiliary Area* for details on the Auxiliary Area.

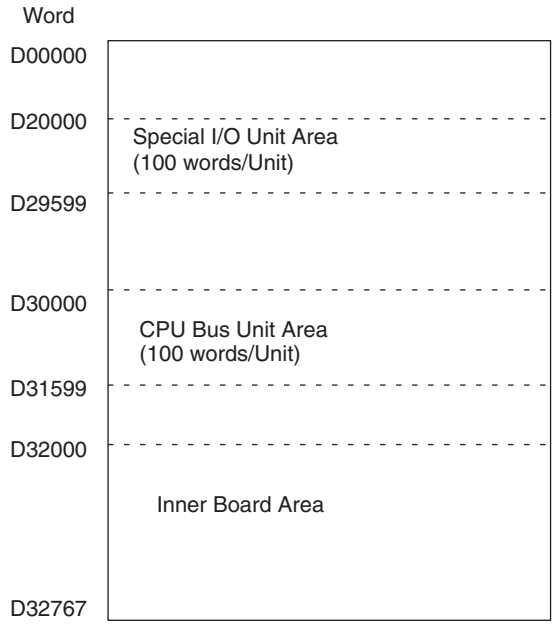


Temporary Relay Area (TR)

The TR Area contains bits that record the ON/OFF status of program branches. The TR bits are used with mnemonics only.

Data Memory Area (DM)

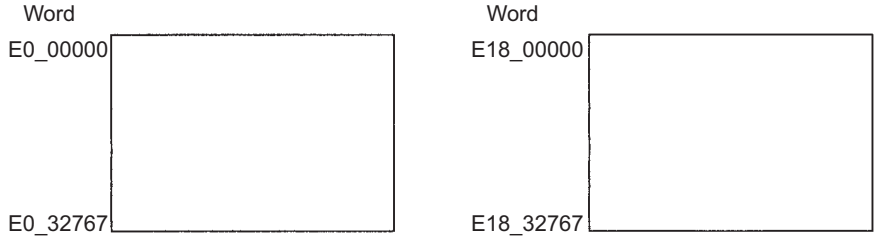
The DM Area is a multi-purpose data area that can be accessed in word-units only (16-bit words). These words retain their content when the PLC is turned ON or the operating mode is switched between PROGRAM mode and RUN or MONITOR mode.



Extended Data Memory Area (EM)

The EM Area is a multi-purpose data area that can be accessed in word-units only (16-bit words). These words retain their content when the PLC is turned ON or the operating mode is switched between PROGRAM mode and RUN or MONITOR mode.

The EM Area is divided into 32,767-word regions called banks. The number of EM banks depends upon the model of CPU Unit, with a maximum of 13 banks (0 to C). Refer to *2-1 Specifications* for details on the number of EM banks provided in each model of CPU Unit.



Timer Area

There are two timer data areas, the Timer Completion Flags and the Timer Present Values (PVs). Up to 4,096 timers with timer numbers T0000 to T4095 can be used. The same number is used to access a timer's Completion Flag and PV.

Timer Completion Flags

These flags are read as bits. A Completion Flag is turned ON by the system when the corresponding timer times out (the set time elapses).

Timer PVs

The PVs are read and written as words (16 bits). The PVs count up or down as the timer operates.

Counter Area

There are two counter data areas, the Counter Completion Flags and the Counter Present Values (PVs). Up to 4,096 counters with counter numbers C0000 to C4095 can be used. The same number is used to access a counter's Completion Flag and PV.

Counter Completion Flags These flags are read as bits. A Completion Flag is turned ON by the system when the corresponding counter counts out (the set value is reached).

Counter PVs The PVs are read and written as words (16 bits). The PVs count up or down as the counter operates.

Condition Flags

These flags include the Arithmetic Flags such as the Error Flag and Equals Flag which indicate the results of instruction execution as well as the Always ON and Always OFF Flags. The Condition Flags are specified with labels (symbols) rather than addresses.

Clock Pulses

The Clock Pulses are turned ON and OFF by the CPU Unit's internal timer. These bits are specified with labels (symbols) rather than addresses.

Task Flag Area (TK)

Task Flags range from TK00 to TK31 and correspond to cyclic tasks 0 to 31. A Task Flag will be ON when the corresponding cyclic task is in executable (RUN) status and OFF when the cyclic task hasn't been executed (INI) or is in standby (WAIT) status.

Index Registers (IR)

These registers (IR0 to IR15) are used to store PLC memory addresses (absolute memory addresses in RAM) to indirectly address words in I/O memory. The Index Registers can be used separately in each task or they can be shared by all tasks.

Data Registers (DR)

These registers (DR0 to DR15) are used together with the Index Registers. When a Data Register is input just before an Index Register, the content of the Data Register is added to the PLC memory address in the Index Register to offset that address. The Data Registers are used separately in each task or they can be shared by all tasks.

8-2-3 Data Area Properties

Content After Fatal Errors, Forced Set/Reset Usage

Area		External allocation	Fatal Error Generated				Forced Set/ Forced Reset Functions Usable?
			Execution of FALS(007)		Other Fatal Error		
			IOM Hold Bit OFF	IOM Hold Bit ON	IOM Hold Bit OFF	IOM Hold Bit ON	
CIO Area	I/O Area	Basic I/O Units	Retained	Retained	Cleared	Retained	Yes
	Data Link Area	Controller Link data links					
	CPU Bus Units	CPU Bus Units					
	Special I/O Unit Area	Special I/O Units					
	Inner Board Area	Inner Boards					
	CS-series DeviceNet Area	DeviceNet Slaves or Master					
	Internal I/O Area	None					

Area	External allocation	Fatal Error Generated				Forced Set/ Forced Reset Functions Usable?
		Execution of FALS(007)		Other Fatal Error		
		IOM Hold Bit OFF	IOM Hold Bit ON	IOM Hold Bit OFF	IOM Hold Bit ON	
Work Area (W)	None	Retained	Retained	Cleared	Retained	Yes
Holding Area (H)		Retained	Retained	Retained	Retained	Yes
Auxiliary Area (A)		Status varies from address to address.				No
Data Memory Area (D)		Retained	Retained	Retained	Retained	No
Extended Data Memory Area (E)		Retained	Retained	Retained	Retained	No
Timer Completion Flags (T)		Retained	Retained	Cleared	Retained	Yes
Timer PVs (T)		Retained	Retained	Cleared	Retained	No
Counter Completion Flags (C)		Retained	Retained	Retained	Retained	Yes
Counter PVs (C)		Retained	Retained	Retained	Retained	No
Task Flags (TK)		Retained	Retained	Cleared	Cleared	No
Index Registers (IR)		Retained	Retained	Cleared	Retained	No
Data Registers (DR)		Retained	Retained	Cleared	Retained	No

Content After Mode Change or Power Interruption

Area		Mode Changed[1]		PLC Power OFF to ON			
				IOM Hold Bit Cleared[2]		IOM Hold Bit Held[2]	
		IOM Hold Bit OFF	IOM Hold Bit ON	IOM Hold Bit OFF	IOM Hold Bit ON	IOM Hold Bit OFF	IOM Hold Bit ON
CIO Area	I/O Area	Cleared	Retained	Cleared	Cleared	Cleared	Retained
	Data Link Area						
	CPU Bus Units						
	Special I/O Unit Area						
	Inner Board Area						
	CS-series DeviceNet Area						
	Internal I/O Area						
Work Area (W)		Cleared	Retained	Cleared	Cleared	Cleared	Retained
Holding Area (H)		Retained	Retained	Retained	Retained	Retained	Retained
Auxiliary Area (A)		Status varies from address to address.					
Data Memory Area (D)		Retained	Retained	Retained	Retained	Retained	Retained
Extended Data Memory Area (E)		Retained	Retained	Retained	Retained	Retained	Retained
Timer Completion Flags (T)		Cleared	Retained	Cleared	Cleared	Cleared	Retained
Timer PVs (T)		Cleared	Retained	Cleared	Cleared	Cleared	Retained
Counter Completion Flags (C)		Retained	Retained	Retained	Retained	Retained	Retained
Counter PVs (C)		Retained	Retained	Retained	Retained	Retained	Retained
Task Flags (TK)		Cleared	Cleared	Cleared	Cleared	Cleared	Cleared
Index Registers (IR)		Cleared	Retained	Cleared	Cleared	Cleared	Cleared
Data Registers (DR)		Cleared	Retained	Cleared	Cleared	Cleared	Cleared

Note
1. Mode changed from PROGRAM to RUN/MONITOR or vice-versa.
2. The PLC Setup's "IOM Hold Bit Status at Startup" setting determines whether the IOM Hold Bit's status is held or cleared when the PLC is turned ON.

8-3 I/O Area

I/O Area addresses range from CIO 0000 to CIO 0319 (CIO bits 000000 to 031915), but the area can be expanded to CIO 0000 to CIO 0999 by changing

the first Rack word with any Programming Device other than a Programming Console. The maximum number of bits that can be allocated for external I/O will still be 5,120 (320 words) even if the I/O Area is expanded.

Note The maximum number of external I/O points depends upon the CPU Unit being used.

Words in the I/O Area are allocated to I/O terminals on Basic I/O Units.

Words are allocated to Basic I/O Units based on the slot position (left to right) and number of words required. The words are allocated consecutively and empty slots are skipped. Words in the I/O Area that aren't allocated to Basic I/O Units can be used only in the program.

Bits in the I/O Area can be force-set and force-reset.

I/O Area Initialization

The contents of the I/O Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM to RUN or MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
   (See the following explanation of IOM Hold Bit Operation.)
2. The PLC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PLC Setup.
   (See the following explanation of IOM Hold Bit Operation.)
3. The I/O Area is cleared from a Programming Device.
4. PLC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the I/O Area will be retained if FALS(007) is executed.)

IOM Hold Bit Operation

By default, the I/O Area is cleared when power is interrupted or the CPU Unit is restarted.

If the IOM Hold Bit (A50012) is ON, the contents of the I/O Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN or MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the I/O Area won't be cleared when the PLC's power supply is cycled. All I/O bits, including outputs, will retain the status that they had before the PLC was turned off.

Note If the I/O Hold Bit is turned ON, the outputs from the PLC will not be turned OFF and will maintain their previous status when the PLC is switched from RUN or MONITOR mode to PROGRAM mode. Make sure that the external loads will not produce dangerous conditions when this occurs. (When operation stops for a fatal error, including those produced with the FALS(007) instruction, all outputs from Output Unit will be turned OFF and only the internal output status will be maintained.)

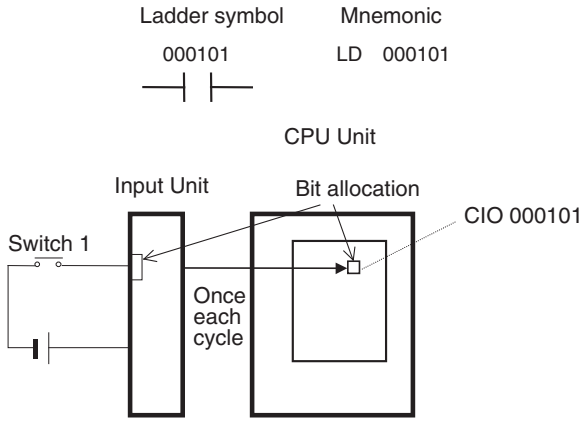
Input Bits

A bit in the I/O Area is called an input bit when it is allocated to an Input Unit. Input bits reflect the ON/OFF status of devices such as push-button switches, limit switches, and photoelectric switches. There are two ways for the status of input points to be refreshed in the PLC: normal I/O refreshing and IORF(097) refreshing.

Normal I/O Refreshing

The status of I/O points on external devices is read once each cycle after program execution.

In the following example, CIO 000101 is allocated to switch 1, an external switch connected to the input terminal of an Input Unit. The ON/OFF status of switch 1 is reflected in CIO 000101 once each cycle.



Immediate Refreshing (Single CPU Systems Only)

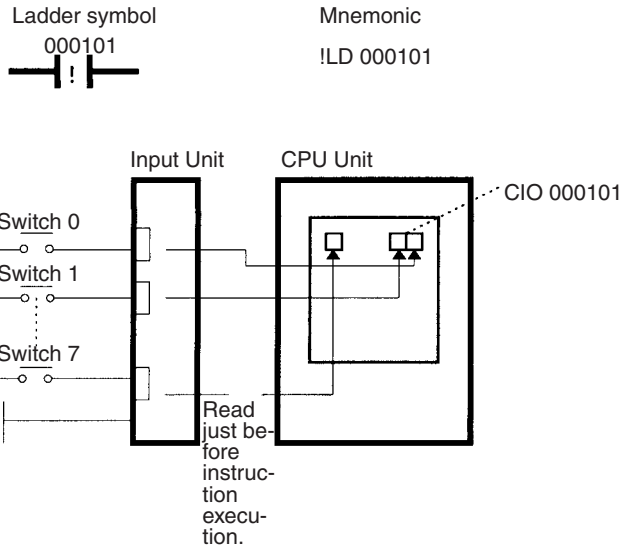
When the immediate refreshing variation of an instruction is specified by inputting an exclamation point just before the instruction, and the instruction's operand is an input bit or word, the word containing the bit or the word itself will be refreshed just before the instruction is executed. This immediate refreshing is performed in addition to the normal I/O refreshing performed once each cycle.

Note Immediate refreshing will be performed for input bits allocated to Basic I/O Units only (excluding C200H Group-2 High-density I/O Units and Basic I/O Units mounted in Remote I/O Slave Racks), not High-density I/O Units which are Special I/O Units.

1,2,3... 1. Bit Operand
Just before the instruction is executed, the ON/OFF status of the 16 I/O points allocated to the word containing the specified bit will be read to the PLC.

2. Word Operand
Just before the instruction is executed, the ON/OFF status of the 16 I/O points allocated to the specified word will be read to the PLC.

In the following example, CIO 000101 is allocated to switch 1, an external switch connected to the input terminal of an Input Unit. The ON/OFF status of switch 1 is read and reflected in CIO 000101 just before !LD 000101 is executed.

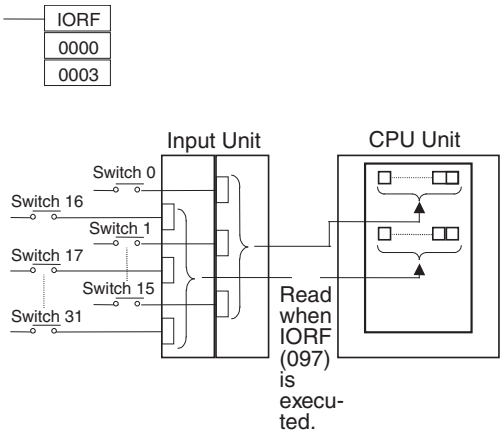


IORF(097) Refreshing

When IORF(097) (I/O REFRESH) is executed, the input bits in the specified range of words are refreshed. This I/O refreshing is performed in addition to the normal I/O refreshing performed once each cycle.

The following IORF(097) instruction refreshes the status of all I/O points in I/O Area words CIO 0000 to CIO 0003. The status of input points is read from the Input Units and the status of output bits is written to the Output Units.

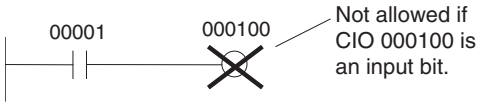
In the following example, the status of input points allocated to CIO 0000 and CIO 0001 are read from the Input Unit. (CIO 0002 and CIO 0003 are allocated to Output Units.)



Limitations on Input bits

There is no limit on the number of times that input bits can be used as normally open and normally closed conditions in the program and the addresses can be programmed in any order.

An input bit cannot be used as an operand in an Output instruction.

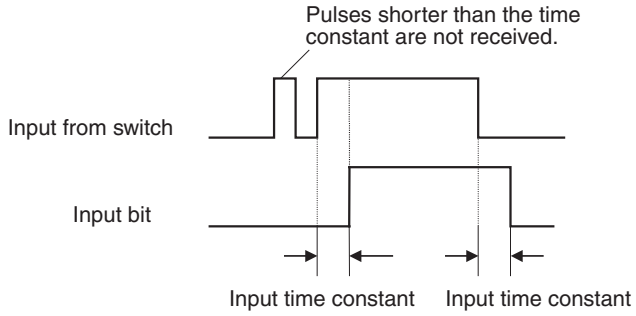


Input Response Time Settings

The input response times for each Input Unit can be set in the PLC Setup. Increasing the input response time will reduce chattering and the effects of noise and decreasing the input response time allows higher speed input pulses to be received.

The default value for input response times is 8 ms and the setting range is 0 to 32 ms.

Note If the time is set to 0 ms, there will still be an ON delay time of 20 μs max. and an OFF delay time of 300 μs due to delays caused by internal elements.



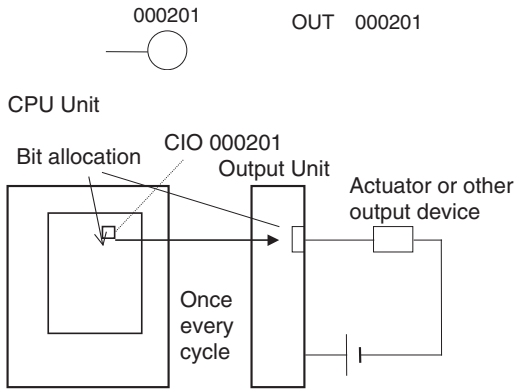
Output Bits

A bit in the I/O Area is called an output bit when it is allocated to an Output Unit. The ON/OFF status of an output bits are output to devices such as actuators. There are two ways for the status of output bits to be refreshed to an Output Unit: normal I/O refreshing and IORF(097) refreshing.

Normal I/O Refreshing

The status of output bits are output to external devices once each cycle after program execution.

In the following example, CIO 000201 is allocated to an actuator, an external device connected to an output terminal of an Output Unit. The ON/OFF status of CIO 000201 is output to that actuator once each cycle.



Immediate Refreshing (Single CPU Systems Only)

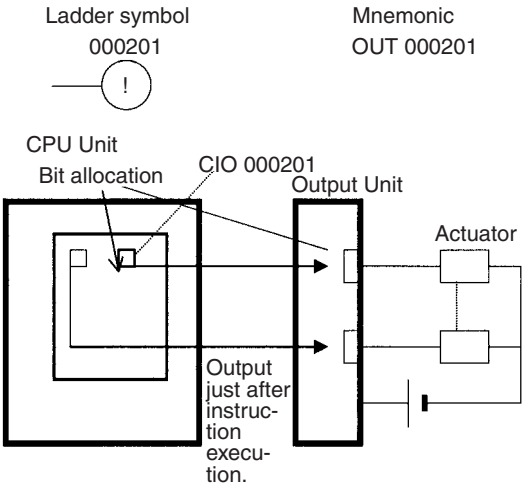
When the immediate refreshing variation of an instruction is specified by inputting an exclamation point just before the instruction, and the instruction's operand is an output bit or word, the content of the word containing the bit or the word itself will be output just after the instruction is executed. This immediate refreshing is performed in addition to the normal I/O refreshing performed once each cycle.

Note Immediate refreshing will be performed for output bits allocated to Basic I/O Units only (excluding C200H Group-2 High-density I/O Units and Basic I/O Units mounted in Remote I/O Slave Racks), not High-density I/O Units which are Special I/O Units.

1,2,3... 1. Bit Operand
Just after the instruction is executed, the ON/OFF status of the 16 I/O points allocated to the word containing the specified bit will be output to the output device(s).

2. Word Operand
   Just after the instruction is executed, the ON/OFF status of the 16 I/O points allocated to the specified word will be output to the output device(s).

In the following example, CIO 000201 is allocated to an actuator, an external device connected to the output terminal of an Output Unit. The ON/OFF status of CIO 000201 is output to the actuator just after !OUT 000201 is executed.

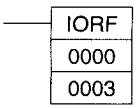


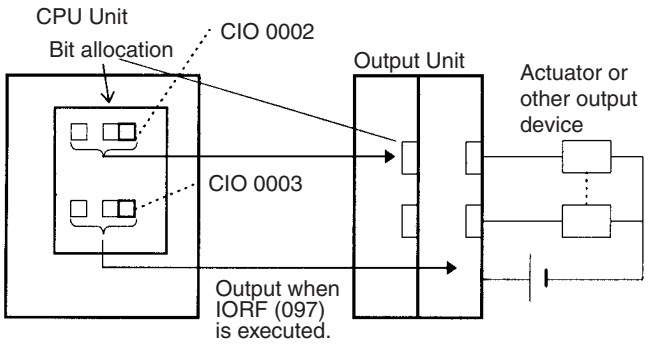
IORF(097) Refreshing

When IORF(097) (I/O REFRESH) is executed, the ON/OFF status of output bits in the specified range of words is output to their external devices. This I/O refreshing is performed in addition to the normal I/O refreshing performed once each cycle.

The following IORF(097) instruction refreshes the status of all I/O points in I/O Area words CIO 0000 to CIO 0003. The status of input points is read from the Input Units and the status of output bits is written to the Output Units.

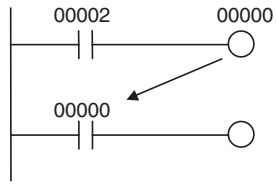
In this example, the status of input points allocated to CIO 0002 and CIO 0003 are output to the Output Unit. (CIO 0000 and CIO 0001 are allocated to Input Units.)



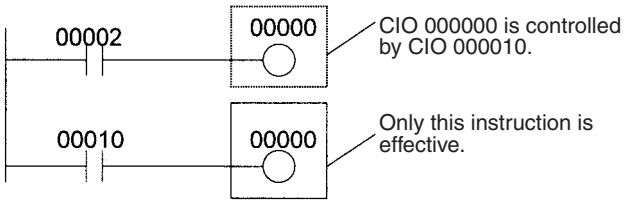


Limitations on Output Bits

Output bits can be programmed in any order. Output bits can be used as operands in Input instructions and there is no limit on the number of times that an output bit is used as a normally open and normally closed condition.



An output bit can be used in only one Output instruction that controls its status. If an output bit is used in two or more Output instructions, only the last instruction will be effective.



Note All outputs on Basic I/O Units and Special I/O Units can be turned OFF by turning ON the Output OFF Bit (A50015). The status of the output bits won't be affected even though the actual outputs are turned OFF.

8-4 CS-series DeviceNet Area

The CS-series DeviceNet Area addresses run from CIO 3200 to CIO 3799 (600 words).

Words in the CS-series DeviceNet Area are used for fixed allocations to Slaves for DeviceNet remote I/O communications for the CS-series DeviceNet Unit (CS1W-DRM21-V1).

The Fixed Allocation Setting Switches 1 to 3 (Software Switches) in the CIO Area words allocated to the DeviceNet Unit determine which fixed allocation words are used.

Area	Master to Slave (Output Words)	Slave to Master (Input Words)
Fixed Allocation Area 1	CIO 3200 to CIO 3263	CIO 3300 to CIO 3363
Fixed Allocation Area 2	CIO 3400 to CIO 3463	CIO 3500 to CIO 3563
Fixed Allocation Area 3	CIO 3600 to CIO 3663	CIO 3700 to CIO 3763

Note If the DeviceNet Unit is set to use the I/O slave function, the following words are also allocated.

Area	Master to Slave (Output Word)	Slave to Master (Input Word)
Fixed Allocation Area 1	CIO 3370	CIO 3270
Fixed Allocation Area 2	CIO 3570	CIO 3470
Fixed Allocation Area 3	CIO 3770	CIO 3670

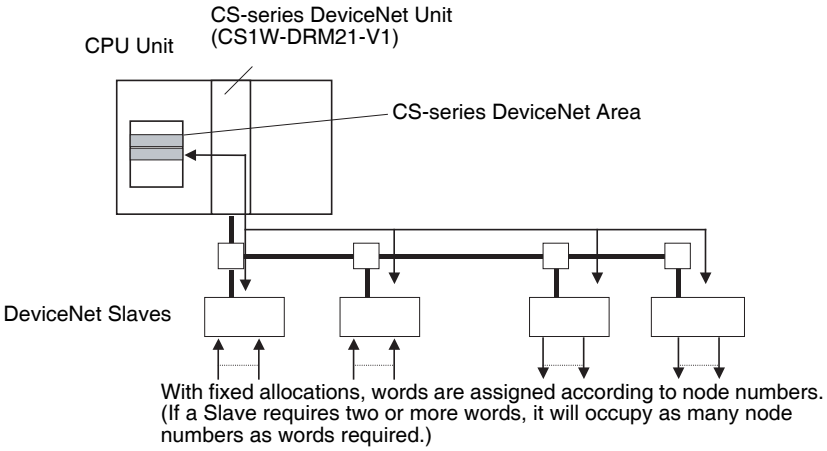
Data is exchanged regularly to Slaves in the network (independent of the program) through the CS-series DeviceNet Unit (CS1W-DRM21-V1) mounted in the CPU Rack.

Words can be allocated to Slaves in two ways: fixed allocation (words allocated by node number) or free allocation (user-set word allocation).

- With fixed allocations, words in the CS-series DeviceNet Area are allocated automatically in node-number order in one of the fixed allocation areas (1 to 3).

- With user-set allocations, the user can allocate words to Slaves from the following words.
  CIO 0000 to CIO 0235, CIO 0300 to CIO 0511, CIO 1000 to CIO 1063
  W000 to W511
  H000 to H511
  D00000 to D32767
  E00000 to E32767 (banks 0 to C)

For details on word allocations, refer to the CS/CJ Series *DeviceNet Unit Operation Manual* (W380).



Forcing Bit Status

Bits in the CS-series DeviceNet Area can be force-set and force-reset.

DeviceNet Area Initialization

The contents of the DeviceNet Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed between PROGRAM and RUN or MONITOR mode and the IOM Hold Bit is OFF.
2. The PLC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PLC Setup.
3. The DeviceNet Area is cleared from a Programming Device.
4. PLC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the DeviceNet Area will be retained when FALS(007) is executed.)

IOM Hold Bit Operation

By default, the DeviceNet Area is cleared when power is interrupted or the CPU Unit is restarted.

If the IOM Hold BIt (A50012) is ON, the contents of the DeviceNet Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN or MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the DeviceNet Area won't be cleared when the PLC's power supply is cycled.

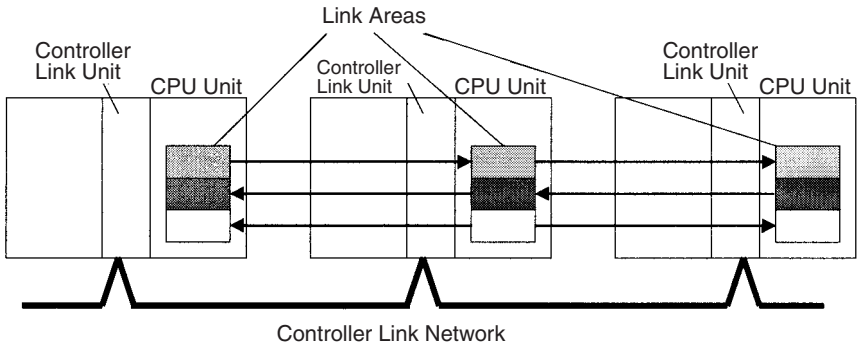
8-5 Data Link Area

Data Link Area addresses range from CIO 1000 to CIO 1199 (CIO bits 100000 to 119915). Words in the Link Area are used for data links when *LR* is set as the data link area for automatic allocation for Controller Link Networks. It is also used for PLC Links.

A data link automatically (independently of the program) shares data with Link Areas in other CPU Units in the network through a Controller Link Unit mounted to the PLC's CPU Rack.

Data links can be generated automatically (using the same number of words for each node) or manually. When a user defines the data link manually, he can assign any number of words to each node and make nodes receive-only or transmit-only. Refer to the *Controller Link Units Operation Manual* (W309) for more details.

Words in the Link Area can be used in the program when *LR* is not set as the data link area for automatic allocation for Controller Link Networks and PLC Links are not used.



Link Area Initialization

The contents of the Link Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PLC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PLC Setup.
3. The Link Area is cleared from a Programming Device.
4. PLC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the Link Area will be retained if FALS(007) is executed.)

IOM Hold Bit Operation

By default, the Data Link Area is cleared when power is interrupted or the CPU Unit is restarted.

If the IOM Hold BIt (A50012) is ON, the contents of the Link Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the Link Area won't be cleared when the PLC's power supply is cycled.

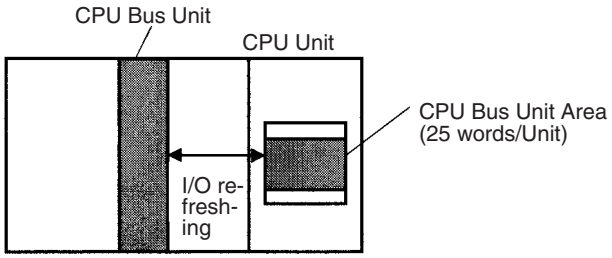
Forcing Bit Status

Bits in the Link Area can be force-set and force-reset.

8-6 CPU Bus Unit Area

The CPU Bus Unit Area contains 400 words with addresses ranging from CIO 1500 to CIO 1899. Words in the CPU Bus Unit Area can be allocated to CPU Bus Units to transfer data such as the operating status of the Unit. Each Unit is allocated 25 words based on the Unit's unit number setting.

Data is exchanged with CPU Bus Units once each cycle during I/O refreshing, which occurs after program execution. (Words in this data area cannot be refreshed with IORF(097).)



Each CPU Bus Unit is allocated 25 words based on its unit number, as shown in the following table.

Unit number	Allocated words
0	CIO 1500 to CIO 1524
1	CIO 1525 to CIO 1549
2	CIO 1550 to CIO 1574
3	CIO 1575 to CIO 1599
4	CIO 1600 to CIO 1624
5	CIO 1625 to CIO 1649
6	CIO 1650 to CIO 1674
7	CIO 1675 to CIO 1699
8	CIO 1700 to CIO 1724
9	CIO 1725 to CIO 1749
A	CIO 1750 to CIO 1774
B	CIO 1775 to CIO 1799
C	CIO 1800 to CIO 1824
D	CIO 1825 to CIO 1849
E	CIO 1850 to CIO 1874
F	CIO 1875 to CIO 1899

The function of the 25 words depends upon the CPU Bus Unit being used. For details, refer to the Unit's operation manual.

Words in the CPU Bus Unit Area that aren't allocated to CPU Bus Units can be used only in the program.

Bits in the CPU Bus Unit Area can be force-set and force-reset.

CPU Bus Unit Area Initialization

The contents of the CPU Bus Unit Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM to RUN or MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PLC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PLC Setup.
3. The CPU Bus Unit Area is cleared from a Programming Device.
4. PLC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the CPU Bus Unit Area will be retained when FALS(007) is executed.)

IOM Hold Bit Operation

By default, the CPU Bus Unit Area is cleared when power is interrupted or the CPU Unit is restarted.

If the IOM Hold BIt (A50012) is ON, the contents of the CPU Bus Unit Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the CPU Bus Unit Area won't be cleared when the PLC's power supply is cycled.

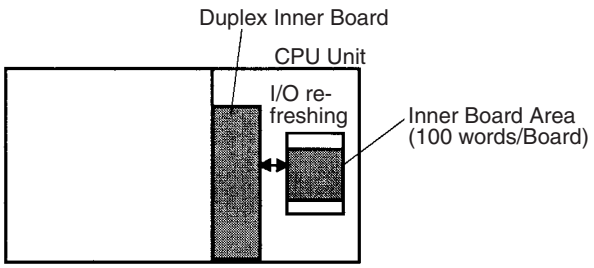
8-7 Inner Board Area

The Inner Board Area contains 100 words with addresses ranging from CIO 1900 to CIO 1999. Words in the Inner Board Area can be allocated to a Duplex Inner Board to transfer data such as the operating status of the Unit. All 100 words must be allocated to just one Inner Board.

Note

1. The Inner Board Area is used for Inner Boards only in Single CPU Systems or for the Inner Boards in a Process-control CPU Units in Duplex CPU Systems.
2. The user cannot mount Inner Boards into CPU Units for Duplex CPU Systems.

Data is exchanged with the Duplex Inner Board once each cycle during normal I/O refreshing, which occurs after program execution. Depending on the type of Inner Board that is mounted, data can also be refreshed directly.



The function of the 100 words in the Inner Board Area depends upon the Duplex Inner Board being used. For details, refer to the Board's Operation Manual.

When the words in the Inner Board Area aren't allocated to an Duplex Inner Board, they can be used only in the program.

Bits in the Inner Board Area can be force-set and force-reset.

Inner Board Area Initialization

The contents of the Inner Board Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PLC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PLC Setup.
3. The Inner Board Area is cleared from a Programming Device.
4. PLC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the Inner Board Area will be retained when FALS(007) is executed.)

IOM Hold Bit Operation

By default, the Inner Board Area is cleared when power is interrupted or the CPU Unit is restarted.

If the IOM Hold BIt (A50012) is ON, the contents of the Inner Board Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the Inner Board Area won't be cleared when the PLC's power supply is cycled.

8-8 Special I/O Unit Area

The Special I/O Unit Area contains 960 words with addresses ranging from CIO 2000 to CIO 2959. Words in the Special I/O Unit Area are allocated to CS-series Special I/O Units to transfer data such as the operating status of the Unit. Each Unit is allocated 10 words based on its unit number setting.

Data is exchanged with Special I/O Units once each cycle during I/O refreshing, which occurs after program execution. The words can also be refreshed with IORF(097).

Each Special I/O Unit is allocated 25 words based on its unit number, as shown in the following table.

Unit number	Allocated words
0	CIO 2000 to CIO 2009
1	CIO 2010 to CIO 2019
2	CIO 2020 to CIO 2029
3	CIO 2030 to CIO 2039
4	CIO 2040 to CIO 2049
5	CIO 2050 to CIO 2059
6	CIO 2060 to CIO 2069
7	CIO 2070 to CIO 2079
8	CIO 2080 to CIO 2089
9	CIO 2090 to CIO 2099
10	CIO 2100 to CIO 2109
11	CIO 2110 to CIO 2119
12	CIO 2120 to CIO 2129
13	CIO 2130 to CIO 2139
14	CIO 2140 to CIO 2149
15	CIO 2150 to CIO 2159
16	CIO 2160 to CIO 2169
17	CIO 2170 to CIO 2179
95	CIO 2950 to CIO 2959

The function of the words allocated to a Unit depends upon the Special I/O Unit being used. For details, refer to the Unit's Operation Manual.

Words in the Special I/O Unit Area that aren't allocated to Special I/O Units can be used only in the program.

Bits in the Special I/O Unit Area can be force-set and force-reset.

Special I/O Unit Area Initialization

The contents of the Special I/O Unit Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PLC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PLC Setup.
3. The Special I/O Unit Area is cleared from a Programming Device.
4. PLC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the Special I/O Unit Area will be retained when FALS(007) is executed.)

IOM Hold Bit Operation

By default, the Special I/O Unit Area is cleared when power is interrupted or the CPU Unit is restarted.

If the IOM Hold BIt (A50012) is ON, the contents of the Special I/O Unit Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the Special I/O Unit Area won't be cleared when the PLC's power supply is cycled.

8-9 Work Area

The Work Area contains 512 words with addresses ranging from W000 to W511. These words can be used only in the program as work words.

There are unused words in the CIO Area (CIO 1200 to CIO 1499 and CIO 3800 to CIO 6143) that can also be used in the program, but use any available words in the Work Area first because the unused words in the CIO Area may be allocated to new functions in future versions of CS1D CPU Units.

Bits in the Work Area can be force-set and force-reset.

Work Area Initialization

The contents of the Work Area will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM to RUN or MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PLC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PLC Setup.
3. The Work Area is cleared from a Programming Device.
4. PLC operation is stopped when a fatal error other than an FALS(007) error occurs. (The contents of the Work Area will be retained when FALS(007) is executed.)

IOM Hold Bit Operation

By default, the Work Area is cleared when power is interrupted or the CPU Unit is restarted.

If the IOM Hold BIt (A50012) is ON, the contents of the Work Area won't be cleared when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

If the IOM Hold BIt (A50012) is ON and the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the contents of the Work Area won't be cleared when the PLC's power supply is cycled.

8-10 Holding Area

The Holding Area contains 512 words with addresses ranging from H000 to H511 (bits H00000 to H51115). These words can be used only in the program.

Holding Area bits can be used in any order in the program and can be used as normally open or normally closed conditions as often as necessary.

Forcing Bit Status

Bits in the Holding Area can be force-set and force-reset.

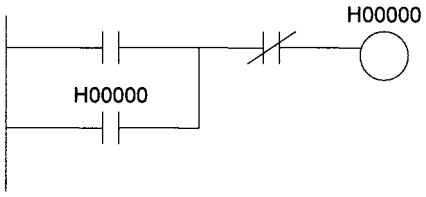
Holding Area Initialization

Data in the Holding Area is not cleared when the PLC's power supply is cycled or the PLC's operating mode is changed from PROGRAM mode to RUN or MONITOR mode or vice-versa.

A Holding Area bit will be cleared if it is programmed between IL(002) and ILC(003) and the execution condition for IL(002) is OFF. To keep a bit ON even when the execution condition for IL(002) is OFF, turn ON the bit with the SET instruction just before IL(002).

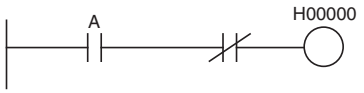
Self-maintaining Bits

When a self-maintaining bit is programmed with a Holding Area bit, the self-maintaining bit won't be cleared even when the power is reset.



Note

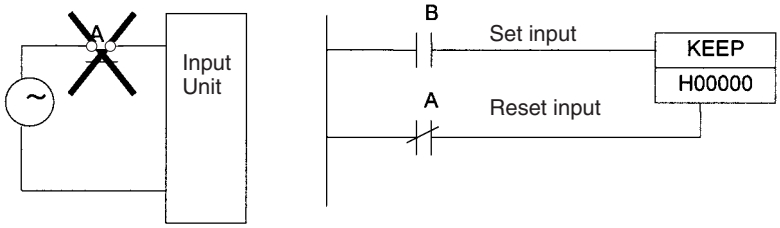
1. If a Holding Area bit is not used for the self-maintaining bit, the bit will be turned OFF and the self-maintaining bit will be cleared when the power is reset.
2. If a Holding Area bit is used but not programmed as a self-maintaining bit as in the following diagram, the bit will be turned OFF by execution condition A when the power is reset.



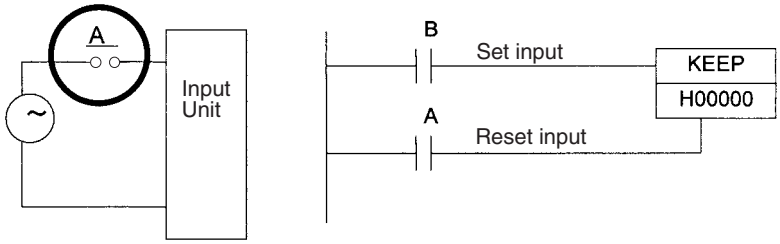
3. H512 to H1535 are Function Block Holding Area words. They can be set only in the FB instance area (internally-assigned range of variables). Note that they cannot be specified as the operand of the instructions on the user program.

Precautions

When a Holding Area bit is used in a KEEP(011) instruction, never use a normally closed condition for the reset input if the input device uses an AC power supply. When the power supply goes OFF or is temporarily interrupted, the input will go OFF before the PLC's internal power supply and the Holding Area bit will be reset.



Instead, use a configuration like the one shown below.



There are no restrictions in the order of using bit address or in the number of N.C. or N.O. conditions that can be programmed.

8-11 Auxiliary Area

The Auxiliary Area contains 960 words with addresses ranging from A000 to A959). These words are preassigned as flags and control bits to monitor and control operation.

Some words and bits in the Auxiliary area are controlled by the system, others can be set by the program or from a Programming Device. The Auxiliary Area includes error flags, initialization flags, control bits, and monitoring data.

Forcing Bit Status

Bits in the Auxiliary Area cannot be force-set and force-reset continuously.

Writing Auxiliary Area Data

The following operations can be performed from a Programming Device to write data in the Auxiliary Area.

- Using the CX-Programmer:
  Online set/reset (not force-set/force-reset, see note), changing present values when monitoring programming addresses (set values dialog box), or transferring data to the PLC after editing the PLC data tables.
  Refer to the *CX-Programmer User Manual*.
- Using a Programming Console:
  Temporarily force-setting/force-resetting bits from the Bit/Word Monitor or the 3-word Monitor operation (see Programming Consoles Operation Manual).

Note Online set/reset operations are supported for Duplex CPU Systems by CX-Programmer version 3.0 or higher and for Single CPU Systems by CX-Programmer version 4.0 or higher.

Functions

The following table lists the functions of Auxiliary Area flags and control bits. The table is organized according to the functions of the flags and bits. For more details or to look up a bit by its address, refer to *Appendix B Auxiliary Area*.

Switching from Duplex to Simplex Operation (Duplex CPU Systems Only)

■ Cause of Switching

Name	Address	Description	Access
Duplex Verification Error Switch Flag	A02300	ON: A duplex verification error caused a switch from duplex to simplex operation. Only operation is switched and the active CPU Unit will not be switched. This flag is turned OFF when duplex operation is restored.	Read-only
Duplex Bus Error Switch Flag	A02301	ON: A duplex bus error caused a switch from duplex to simplex operation. Only operation is switched and the active CPU Unit will not be switched. This flag is turned OFF when duplex operation is restored.	Read-only
Duplex Initialization Error Switch Flag	A02302	ON: An error during duplex initialization caused a switch from duplex to simplex operation and duplex operation was never started. The active CPU Unit will not be switched. This flag is turned OFF when duplex operation is restored.	Read-only
CPU Unit Setting Switch Flag	A02303	ON: Changing the CPU Unit's switch from USE to NO USE caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	Read-only
CPU Error (WDT) Switch Flag	A02304	ON: A CPU Unit error (WDT) caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	Read-only
FALS Instruction Error Switch Flag	A02306	ON: Execution of an FALS instruction caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	Read-only
Cycle Time Overrun Switch Flag	A02308	ON: Exceeding the cycle time caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	Read-only
Program Error Switch Flag	A02309	ON: A program error caused a switch from duplex to simplex operation.The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	Read-only
Fatal Inner Board Error Switch Flag (Process-control CPU Units only)	A02312	ON: A fatal Inner Board error caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	Read-only
Memory Error Switch Flag	A02315	ON: A memory error caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	Read-only

The following programming can be used with the flags in A023 to detect when the system switches from duplex to simplex operation.

If the contents of A023 is not 0, the "duplex error" output is turned ON to indicate that the system has switched to simplex operation.

■ Time of Switching

Name	Address	Description	Access
Time of Switch from Duplex to Simplex Operation	A024 to A026	The time when operation was switched from duplex to simplex operation is stored. The time is cleared when duplex operation is restored. A02400 to A02407: Seconds (00 to 59) A02408 to A02415: Minutes (00 to 59) A02500 to A02507: Hours (00 to 23) A02508 to A02515: Day of month (01 to 31) A02600 to A02607: Month (01 to 12) A02608 to A02615: Year (00 to 99)	Read-only

■ Previous Cause of Switching

Name	Address	Description	Access
Duplex Verification Error Switch Flag	A01900	ON: A duplex verification error caused the previous switch from duplex to simplex operation.	Read-only
Duplex Bus Error Switch Flag	A01901	ON: A duplex bus error caused the previous switch from duplex to simplex operation.	Read-only
Duplex Initialization Error Switch Flag	A01902	ON: An error during duplex initialization caused the previous switch from duplex to simplex operation and duplex operation was never started.	Read-only
CPU Unit Setting Switch Flag	A01903	ON: Changing the CPU Unit's switch from USE to NO USE caused the previous switch from duplex to simplex operation.	Read-only
CPU Error (WDT) Switch Flag	A01904	ON: A CPU Unit error (WDT) caused the previous switch from duplex to simplex operation.	Read-only
FALS Instruction Error Switch Flag	A01906	ON: Execution of an FALS instruction caused the previous switch from duplex to simplex operation.	Read-only
Cycle Time Overrun Switch Flag	A01908	ON: Exceeding the cycle time caused the previous switch from duplex to simplex operation.	Read-only
Program Error Switch Flag	A01909	ON: A program error caused the previous switch from duplex to simplex operation.	Read-only
Fatal Inner Board Error Switch Flag (Process-control CPU Units only)	A01912	ON: A fatal Inner Board error caused the previous switch from duplex to simplex operation.	Read-only
Memory Error Switch Flag	A01915	ON: A memory error caused the previous switch from duplex to simplex operation.	Read-only

■ Previous Time of Switching

Name	Address	Description	Access
Time of Previous Switch from Duplex to Simplex Operation	A020 to A022	The time of the previous switch from duplex to simplex operation is stored. A02000 to A02007: Seconds (00 to 59) A02008 to A02015: Minutes (00 to 59) A02100 to A02107: Hours (00 to 23) A02108 to A02115: Day of month (01 to 31) A02200 to A02207: Month (01 to 12) A02208 to A02215: Year (00 to 99)	Read-only

Non-fatal Duplex Errors

Name	Address	Description	Reference
Non-fatal Duplex Error Flag	A40214	ON: One of the following errors occurred: Duplex verification error, duplex bus error, duplex power supply unit error, or duplex communications error (See note.)	Duplex Verifications Errors Duplex Power Supply Errors Duplex Communications Errors
Duplex Verification Error Flag (See note.)	A31600	ON: An inconsistency exists between the program or memory of the active and standby CPU Units in Duplex Mode. (Refer to A317, A804 for details.)	Duplex Verifications Errors
Duplex Bus Error Flag (See note.)	A31601	ON: An error occurred on the sync transfer bus in the duplex system.	---
Duplex Power Supply Unit Error Flag	A31602	ON: An error occurred in the Power Supply Unit or power supply system on a duplex CPU Rack, Expansion Rack, or Long-distance Expansion Rack.	Duplex Power Supply Errors
Duplex Communications Error Flag	A31603	ON: One of the duplex Communications Units has failed. (Refer to A434 to A437 for details.)	Duplex Communications Errors

Note Duplex CPU Systems only.

■ Duplex Verifications Errors (Duplex CPU Systems Only)

Name	Address	Description	Access
Duplex Verification Error Flag	A31600	ON: An inconsistency exists between the program or memory of the active and standby CPU Units in Duplex Mode. (Refer to A317, A804 for details.)	Read-only
Other CPU Unit Duplex Verification Error Flag	A31706	ON: A duplex error occurred in the other CPU Unit when entering Duplex Mode.	Read-only
CPU Unit Model Verification Error Flag	A31707	ON: The CPU Units were not the same model when entering Duplex Mode.	Read-only
CPU Unit Version Verification Error Flag	A31708	ON: The unit version of the standby CPU Unit is earlier than the unit version of the active CPU Unit and the active CPU Unit uses function not supported by the standby CPU Unit.	Read-only
Inner Board Model Verification Error Flag (Process-control CPU Units only)	A31710	ON: The duplex Inner Boards in the two Process-control CPU Units were not the same model when entering Duplex Mode.	Read-only
Parameter Area Verification Error Flag	A31713	ON: The parameter area in the two CPU Units in duplex mode do not have the same contents.	Read-only
No Active CPU Unit Error Flag	A31714	ON: When the power is ON, the CPU Unit set to standby in duplex mode detected that the active CPU is missing. This happens in the following cases. • The active CPU Unit is not mounted. • The use active CPU setting switch is set to NO USE. • Because DIP Switch Pin 7 is ON on the active CPU Unit, simple backup (reading from memory card to CPU Unit) is set. • A DIP switch setting error has occurred on the active CPU Unit.	Read-only
User Program Verification Error Flag	A31715	ON: The user program in the two CPU Units in duplex mode do not have the same contents.	Read-only
Ethernet Duplex Setting Flag	A80400	ON: The unit version of the standby CPU Unit is earlier than the unit version of the active CPU Unit and the active CPU Unit uses a PLC Setup setting (Ethernet Duplex Setting) that is not supported by the standby CPU Unit.	Read-only

Name	Address	Description	Access
Unit Removal without a Programming Device Function Setting Flag	A80401	ON: The unit version of the standby CPU Unit is earlier than the unit version of the active CPU Unit and the active CPU Unit uses a PLC Setup setting (Unit Removal without a Programming Device Function Setting) that is not supported by the standby CPU Unit.	Read-only
Removal/Addition of Units without a Programming Device Setting Flag	A80402	ON: The unit version of the standby CPU Unit is earlier than the unit version of the active CPU Unit and the active CPU Unit uses a PLC Setup setting (Removal/Addition of Units without a Programming Device Setting) that is not supported by the standby CPU Unit.	Read-only
Turn ON Error Unit Number Flag when Removing a Special Unit Setting Flag	A80403	ON: The unit version of the standby CPU Unit is earlier than the unit version of the active CPU Unit and the active CPU Unit uses a PLC Setup setting (Turn ON Error Unit Number Flag when Removing a Special Unit Setting) that is not supported by the standby CPU Unit.	Read-only
Communications Port Auto-allocation Instruction	A80404	ON: The unit version of the standby CPU Unit is earlier than the unit version of the active CPU Unit and the active CPU Unit uses an instruction (automatically allocating the communications port) that is not supported by the standby CPU Unit.	Read-only
Non-fatal Duplex Error Flag	A40214	ON: One of the following errors occurred: Non-fatal duplex error, duplex verification error, duplex bus error, duplex power supply unit error, or duplex communications error	Read-only

■ Duplex Power Supply Information

Name	Address	Description	Access
Duplex Power Supply Unit Error Flag	A31602	ON: An error occurred in the Power Supply Unit or power supply system on a duplex CPU Rack, Expansion Rack, or Long-distance Expansion Rack.	Read-only
Error Power Supply Unit Location	A31900 to A31915	When an error in a Power Supply Unit results in an error in the 5-V/26-V output, one of the following bits will turn ON to show the location of the Power Supply Unit with the error. A31900: Right Power Supply Unit on CPU Rack (rack 0). A31901: Left Power Supply Unit on CPU Rack (rack 0). A31902: Right Power Supply Unit on Expansion Rack (rack 1). A31903: Left Power Supply Unit on Expansion Rack (rack 1). ... A31914: Right Power Supply Unit on Expansion Rack (rack 7). A31915: Left Power Supply Unit on Expansion Rack (rack 7).	Read-only
	A32000 to A32015	When the voltage on the primary side of the Power Supply Unit drops or is interrupted, one of the following bits will turn ON to show the location of the Power Supply Unit with the error. A32000: Right Power Supply Unit on CPU Rack (rack 0). A32001: Left Power Supply Unit on CPU Rack (rack 0). A32002: Right Power Supply Unit on Expansion Rack (rack 1). A32003: Left Power Supply Unit on Expansion Rack (rack 1). ... A32014: Right Power Supply Unit on Expansion Rack (rack 7). A32015: Left Power Supply Unit on Expansion Rack (rack 7).	Read-only

■ Duplex Communications Unit Information for I/O Table Generation

Name	Address	Description	Access
Duplex Communications Unit Missing or Non-Duplex Communications Unit Flag	A26111	ON: Duplex Units are not mounted for a unit number specified for Duplex Communications Units (i.e., one Unit is missing or the mounted Units do not support duplex operation). The I/O tables will not be created and an I/O Table Creation Error will occur.	Read-only
Duplex Communications Unit Verification Error Flag	A26112	ON: The duplex setting in the PLC Setup for a unit number specified for Duplex Communications Units does not agree with the setting on the Duplex Communications Units. The I/O tables will not be created and an I/O Table Creation Error will occur. Refer to the Operation Manual for the Communications Units for details on Unit settings.	Read-only

■ Duplex Communications Cable Information

Name	Address	Description	Access
Duplex Communications Cable Status Flags	A271	ON: The corresponding I/O Communications Cable is duplexed. A27100: Cable between CPU Rack and Expansion Rack 1 A27101: Cable between Expansion Racks 1 and 2 A27102: Cable between Expansion Racks 2 and 3 A27103: Cable between Expansion Racks 3 and 4 A27104: Cable between Expansion Racks 4 and 5 A27105: Cable between Expansion Racks 5 and 6 A27106: Cable between Expansion Racks 6 and 7	Read-only
Duplex Communications Cable Error Flags	A270	ON: An error has occurred at some point in the corresponding I/O Communications Cable. A27000: Error between CPU Rack slot 0 and Expansion Rack 1 A27001: Error between CPU Rack slot 1 and Expansion Rack 1 A27002: Error between Expansion Rack 1 slot 0 and Rack 2 A27003: Error between Expansion Rack 1 slot 1 and Rack 2 A27004: Error between Expansion Rack 2 slot 0 and Rack 3 A27005: Error between Expansion Rack 2 slot 1 and Rack 3 A27006: Error between Expansion Rack 3 slot 0 and Rack 4 A27007: Error between Expansion Rack 3 slot 1 and Rack 4 A27008: Error between Expansion Rack 4 slot 0 and Rack 5 A27009: Error between Expansion Rack 4 slot 1 and Rack 5 A27010: Error between Expansion Rack 5 slot 0 and Rack 6 A27011: Error between Expansion Rack 5 slot 1 and Rack 6 A27012: Error between Expansion Rack 6 slot 0 and Rack 7 A27013: Error between Expansion Rack 6 slot 1 and Rack 7	Read-only

■ Duplex Communications Errors

Name	Address	Description	Access
Duplex Communications Unit Operating Flags	A02700 to A02715	ON: The Communications Unit with the corresponding unit number is in duplex operation. Bits 00 to 15 correspond to unit numbers 0 to F.	Read-only
Duplex Communications Error Flag	A31603	ON: One of the duplex Communications Unit has failed. (Refer to A434 to A437 for details.)	Read-only
Duplex Communications Recognition Error Flags	A43400 to A43415	ON: Duplex Communications Units for the corresponding unit number does not exist, i.e., it is not mounted, the Unit does not support duplex operation, or the unit number is illegal. Bits 00 to 15 correspond to unit numbers 0 to F.	Read-only
Duplex Communications Verification Error Flags	A43500 to A43515	ON: The settings of the pair of Units mounted for duplex communications are not the same. Refer to the Operation Manual for the Communications Unit for details on settings. Bits 00 to 15 correspond to unit numbers 0 to F.	Read-only

Name	Address	Description	Access
Duplex Communications Switched Flags (non-fatal communications error)	A43600 to A43615	Active/Standby Communications Units ON: An error was detected in self-diagnosis in the active Communications Unit and operation was switched to the standby Communications Unit. Communications will be continued by the standby Communications Unit. Primary/Secondary Communications Units (See Note) ON: An error was detected in self-diagnosis in the primary Communications Unit and operation was switched to the secondary Communications Unit. Communications will be continued by the secondary Communications Unit. All Communications Units Bits 00 to 15 correspond to unit numbers 0 to F. This flag is turned OFF when online Unit replacement is performed for the faulty Communications Unit. **Note:** Primary/Secondary Communications Units are supported by CPU Unit Ver. 1.1 or later.	Read-only
Duplex Communications Standby Unit Error Flags (non-fatal communications error)	A43700 to A43715	Active/Standby Communications Units ON: An error was detected in self-diagnosis in the standby Communications Unit. Communications will be continued by the active Communications Unit. Primary/Secondary Communications Units (See Note) ON: An error was detected in self-diagnosis in the secondary Communications Unit. Communications will be continued by the primary Communications Unit. All Communications Units Bits 00 to 15 correspond to unit numbers 0 to F. This flag is turned OFF when online Unit replacement is performed for the faulty Communications Unit. **Note:** Primary/Secondary Communications Units are supported by CPU Unit Ver. 1.1 or later.	Read-only
Duplex Communications Switch Cause Flags	A042 to A049	Active/Standby Communications Units When an error occurs in the active Communications Unit and operation is switched to the standby Communications Unit, an error code will be stored to show the cause of the error in the active Communications Unit. An error code is not stored when an error occurs in the standby Communications Unit. Primary/Secondary Communications Units (See Note) When an error occurs in the primary Communications Unit and operation is switched to the secondary Communications Unit, an error code will be stored to show the cause of the error in the primary Communications Unit. When an error occurs in the secondary Communications Unit, an error code is stored in the words for one unit number higher than the primary Communications Unit. All Communications Units The corresponding bit in A436 (Duplex Communications Switched Flags) will also turn ON. Refer to the Operation Manual for the Communications Unit for details on error codes. **Note:** Primary/Secondary Communications Units are supported by CPU Unit Ver. 1.1 or later.	Read-only

Duplex System Status

Name	Address	Description	Access
Duplex/Simplex Mode Flag (Duplex CPU Systems only)	A32808	Indicates the current mode as follows: 1: Duplex Mode 0: Simplex Mode A32808 is turned OFF in duplex initialization and thus cannot be used alone to detect errors causing a switch to Simplex Mode. Use A32808 together with A43915 as shown below.  The Duplex Initialization Flag is also used for write processing in online editing, when the initialize switch is pressed, when processing commands from communications or Programming Devices, etc. **Note** The above output will also indicate a duplex error for one cycle when online editing is performed. If this causes a problem in the system, use the flags in A023 that indicate the cause of switching to detect switching to simplex operation.	Read-only
Active CPU Unit Location Flag (Duplex CPU Systems only)	A32809	Indicates which CPU Unit is the active CPU Unit. ON: Right CPU Unit, OFF: Left CPU Unit	Read-only
Duplex System Configuration Flags	A32810 and A32811	Indicates the system configuration, CS1H CPU Units or CS1D CPU Units. A32810 OFF, A32811 OFF: CS1-H CPU Unit A32810 ON, A32811 OFF: CS1D CPU Unit for Single CPU System A32810 ON, A32811 ON: CS1D CPU Unit for Duplex CPU System	Read-only
Right CPU Unit Duplex Recovery Failed Flag (Duplex CPU Systems only)	A32814	ON: The right CPU Unit failed to recover duplex operation in Duplex Mode even after the error was cleared and an attempt was made to recover duplex operation automatically.	Read-only
Left CPU Unit Duplex Recovery Failed Flag (Duplex CPU Systems only)	A32815	ON: The left CPU Unit failed to recover duplex operation in Duplex Mode even after the error was cleared and an attempt was made to recover duplex operation automatically.	Read-only
This CPU Unit Location Flag (Duplex CPU Systems only)	A32515	Indicates where this CPU Unit is mounted. ON: Right side, OFF: Left side	Read-only
Duplex Initialization Flag (Duplex CPU Systems only)	A43915	ON: Duplex operation being initialized.	Read-only

■ I/O Table Generation Errors

Name	Address	Description	Access
CPU Bus Unit Setup Area Initialization Error Flag	A26100	ON: Error in CPU Bus Unit Setup Turns OFF when I/O tables are generated normally.	Read-only
I/O Overflow Flag	A26102	ON: Overflow in maximum number of I/O points. Turns OFF when I/O tables are generated normally.	Read-only
Duplication Error Flag	A26103	ON: The same unit number was used more than once. Turns OFF when I/O tables are generated normally.	Read-only
I/O Bus Error Flag	A26104	ON: I/O bus error Turns OFF when I/O tables are generated normally.	Read-only
Special I/O Unit Error Flag	A26107	ON: Error in a Special I/O Unit Turns OFF when I/O tables are generated normally.	Read-only

Name	Address	Description	Access
I/O Unconfirmed Error Flag	A26109	ON: I/O detection has not been completed. Turns OFF when I/O tables are generated normally.	Read-only
Online Replacement Flag	A26110	ON: An online replacement operation is being performed (It is treated as an I/O table creation error.) This flag will be turned OFF automatically when the online replacement operation has been completed. (Do not attempt to create the I/O tables while this flag is ON.) (See *Unit Online Replacement Information* below.)	Read-only
Duplex Communications Unit Error Flag	A26111	ON: Duplex Units are not mounted for a unit number specified for Duplex Communications Units (i.e., one Unit is missing or the mounted Units do not support duplex operation).	Read-only
Duplex Communications Unit Verification Error Flag	A26112	ON: The duplex setting in the PLC Setup for a unit number specified for Duplex Communications Units does not agree with the setting on the Duplex Communications Units. The I/O tables will not be created and an I/O Table Creation Error will occur. Refer to the Operation Manual for the Communications Units for details on Unit settings.	Read-only

CPU Standby Information

Name	Address	Description	Access
CPU Bus/Special I/O Unit Startup Flag	A32203	ON: The CPU Unit is on standby waiting for CPU Bus or Special I/O Units to start.	Read-only
Duplex Bus Error Standby Flag (Duplex CPU Systems only)	A32204	ON: The CPU Unit is on standby because a duplex bus error occurred at startup.	Read-only
Duplex Verification Error Standby Flag (Duplex CPU Systems only)	A32205	ON: The CPU Unit is on standby because a duplex verification error occurred at startup.	Read-only
Waiting for Other CPU Unit Standby Flag (Duplex CPU Systems only)	A32206	ON: The CPU Unit is on standby waiting for the other CPU Unit to start operation at startup.	Read-only
Inner Board Startup Flag (Duplex CPU Systems only)	A32207	ON: The CPU Unit is on standby waiting for an Inner Board to start.	Read-only
Expansion Power OFF Standby Flag	A32208	ON: The CPU Unit is on standby because power is not being supplied to an Expansion Rack.	Read-only

Unit Online Replacement Information

Name	Address	Description	Access
Online Replacement Flag(See note 4.)	A03115	ON: A Basic I/O Unit, Special I/O Unit, or CPU Bus Unit is being replaced online on the CPU Rack, an Expansion Rack, or a Long-distance Expansion Rack. (See note 3.)	Read-only
I/O Table Creation Error Flag	A26110	ON: User attempted to generate the I/O table during online replacement, causing an I/O table creation error. (See note 3.) (Do not attempt to create an I/O table while a Basic I/O Unit, Special I/O Unit, or CPU Bus Unit is being replaced online, i.e., while one of the Online Replacement Slot Flags in A034 to A041 is ON.)	Read-only
Online Replacement Slot Flags	A034 to A041	ON: Online replacement is being performed (see note 3) for the slot that corresponds to the ON bit. A03400 to A03404: CPU Rack slots 0 to 4 A03405 to A03407: CPU Rack slots 5 to 7 (Single CPU Systems only) A03415: Duplex Unit A03500 to A03508: Expansion Rack 1, slots 0 to 8 A03600 to A03608: Expansion Rack 2, slots 0 to 8 ... A04100 to A04108: Expansion Rack 7, slots 0 to 8	Read-only

Name	Address	Description	Access
CPU Bus Unit Error, Unit Number Flags	A41700 to A41715	When an error occurs in a data exchange between the CPU Unit and a CPU Bus Unit, the CPU Bus Unit Error Flag (A40207) and the corresponding flag in A417 are turned ON. If the PLC Setup is set to turn ON the corresponding Error Unit Number Flag when a Special Unit (Special I/O Unit or CPU Bus Unit) is being replaced, the corresponding flag will be turned ON when the Unit is being replaced. If a duplexed CLK Unit is being replaced, the corresponding flag will be turned ON during replacement. Bits 00 to 15 correspond to unit numbers 0 to F.	Read-only
Special I/O Unit Error, Unit Number Flags	A41800 to A42315	When an error occurs in a data exchange between the CPU Unit and a Special I/O Unit, the Special I/O Unit Error Flag (A40206) and the corresponding flag in these words are turned ON. If the PLC Setup is set to turn ON the corresponding Error Unit Number Flag when a Special Unit (Special I/O Unit or CPU Bus Unit) is being replaced, the corresponding flag will be turned ON when the Unit is being replaced.	Read-only
Unit Replacement without a Programming Device Enabled Flag	A09911	ON when the *Unit Removal without a Programming Device* or *Removal/Addition of Units without a Programming Device* function has been enabled in the PLC Setup.	Read-only
Maintenance Start Bit	A80015	This bit is provided to prevent non-fatal errors from occurring during Unit removal without a Programming Device. When this bit is ON, a Basic I/O Unit error, Special I/O Unit error, or CPU Bus Unit error will not occur when a Unit is removed. In addition, the CPU Unit will not detect an error even if a Basic I/O Unit error, Special I/O Unit error, or CPU Bus Unit error occurs in a Unit other than the one being removed. When this bit is OFF, a Basic I/O Unit error, Special I/O Unit error, or CPU Bus Unit error will occur when a Unit is removed. In addition, the CPU Unit will detect Basic I/O Unit errors, Special I/O Unit errors, or CPU Bus Unit errors occurring in Units other than the one being removed. After replacing the Units, turn ON the Online Replacement Completed Bit (A80215) to restart data exchange. This bit is turned OFF automatically when the Online Replacement Completed Bit goes ON. (See note 5.) This bit can also be turned OFF manually by the user before all of the online replacements have been completed. Turn this bit OFF when you want to detect errors in Units other than the ones being replaced.	Read/write
Online Replacement Completed Bit	A80215	The bit is provided to restart the data exchange between the replaced Unit and CPU Unit. After a Unit has been replaced without a Programming Device, turn ON the Online Replacement Completed Bit to restart the data exchange between the CPU Unit and the slot where the Unit was replaced. Once data exchange has started, the bit goes OFF.	Read/write
Online Replacement Completion Error Flag	A80115	ON: Online replacement (see note 3) failed. This flag indicates the completion status for the last online Unit replacement that occurred, so it will be turned OFF when a Unit is successfully replaced even if there is still a Unit in the PLC which was not replaced successfully.	Read/write
Online Replacement Completion Error Details	A80300 to A80302	When an online replacement function (see note 3) failed, the relevant flag will be turned ON. A80300: No Unit mounted or Unit mounted in another slot. A80301: Different unit types, unit numbers, or serial numbers on replaced and new unit. A80302: Different node numbers on replaced and new Units (when replacing a duplex Communications Unit).	Read/write

Note

1. Do not turn ON the Maintenance Start Bit continuously from the ladder program or other source. As long as the Maintenance Start Bit is ON, errors will not be generated even if there are Unit malfunctions, so the system may be adversely affected.
2. Do not turn ON the Online Replacement Completed Bit continuously from the ladder program or other source. If the Unit is mounted while the Online Replacement Completed Bit is ON, the PLC (CPU Unit) may stop operating.
3. The flags in A034 to A041 indicate removal of a Unit with any one of the following functions.
   - Online Unit Replacement using a Programming Device
   - Unit Removal without a Programming Device
   - Unit Removal/Addition without a Programming Device
4. CS1D CPU Units for Duplex-CPU System only.
5. This bit will turn OFF automatically after all Units have been mounted to complete the online replacement operation (i.e., after data exchange has started) when the Unit Removal/Addition without a Programming Device function is used for a Duplex CPU, Dual I/O Expansion System.

Online Backplane/Unit Addition Information

Name	Address	Description	Access
Online Addition Failed Flag	A27215	ON: An error occurred that prevented a Backplane and Unit from being added online.	Read/write
Online Addition Failure Cause Flags	A27300 to A27309	When an error occurred that prevented a Backplane and Unit from being added online, the relevant flag will be turned ON. A27300: Transmitted I/O tables are invalid (changed or deleted). A27301: Basic I/O Unit mounted in an invalid slot. A27302: No Unit mounted in the added slot. A27303: Specified an Expansion Backplane addition to an earlier CPU Backplane version. A27304: A CPU Bus Unit was added. A27305: The added Unit's model is different from the Unit that was specified to be mounted. A27306: The added Basic I/O Unit's allocated words duplicate the words of an existing Unit. A27307: The added unit number duplicates an existing unit number. A27308: The number of I/O points exceeds the maximum (5,120 I/O points). A27309: There is an error in the added Expansion Backplane (power supply OFF).	Read/write

■ **Operation Start/Stop Times (CPU Unit Ver. 1.1 or Later Only)**

Name	Address	Description	Access
Operation Start Time	A515 to A517	The time that operation started as a result of changing the operating mode to RUN or MONITOR mode is stored here in BCD. A51500 to A51507: Seconds (00 to 59) A51508 to A51515: Minutes (00 to 59) A51600 to A51607: Hour (00 to 23) A51608 to A51615: Day of month (01 to 31) A51700 to A51707: Month (01 to 12) A51708 to A51715: Year (00 to 99) **Note:** The previous start time is stored after turning ON the power supply until operation is started.	Read/write
Operation End Time	A518 to A520	The time that operation stopped as a result of changing the operating mode to PROGRAM mode is stored here in BCD. A51800 to A51807: Seconds (00 to 59) A51808 to A51815: Minutes (00 to 59) A51900 to A51907: Hour (00 to 23) A51908 to A51915: Day of month (01 to 31) A52000 to A52007: Month (01 to 12) A52008 to A52015: Year (00 to 99) **Note:** If an error occurs in operation, the time of the error will be stored. If the operating mode is then changed to PROGRAM mode, the time that PROGRAM mode was entered will be stored.	Read/write

■ **Power Supply Information**

Name	Address	Description	Access
Startup Time	A510 and A511	These words contain the time (in BCD) at which the power was turned ON. The contents are updated every time that the power is turned ON. A51000 to A51007: Seconds (00 to 59) A51008 to A51015: Minutes (00 to 59) A51100 to A51107: Hour (00 to 23) A51108 to A51115: Day of the month (01 to 31)	Read/write
Power Interruption Time	A512 and A513	These words contain the time (in BCD) at which the power was interrupted. The contents are updated every time that the power is interrupted. A51200 to A51207: Seconds (00 to 59) A51208 to A51215: Minutes (00 to 59) A51300 to A51307: Hour (00 to 23) A51308 to A51315: Day of month (01 to 31) These words are not cleared when the power supply is turned ON.	Read/write
Number of Power Interruptions	A514	Contains the number of times (in binary) that power has been interrupted since the power was first turned on. To reset this value, overwrite the current value with 0000.	Read/write
Total Power ON Time	A523	Contains the total time (in binary) that the PLC has been on in 10-hour units. The data is stored is updated every 10 hours. To reset this value, overwrite the current value with 0000.	Read/write
Power ON Clock Data 1 (see note 1, 2)	A720 to A722	These words contain the startup date/time (the same time as the startup time stored in words A510 to A511 as well as the month and year information) for the last time that power was turned ON. The data is BCD. (see note 3) A72000 to A72007: Seconds (00 to 59) A72008 to A72015: Minutes (00 to 59) A72100 to A72107: Hour (00 to 23) A72108 to A72115: Day of month (01 to 31) A72200 to A72207: Month (01 to 12) A72208 to A72215: Year (00 to 99)	Read/write

Name	Address	Description	Access
Power ON Clock Data 2 (see note 1, 2)	A723 to A725	These words contain the startup time/date for the second-to-last time that power was turned ON. The data is BCD and the storage format is the same as words A720 to A722. (see note 3)	Read/write
Power ON Clock Data 3 (see note 1, 2)	A726 to A728	These words contain the startup time/date for the third-to-last time that power was turned ON. The data is BCD and the storage format is the same as words A720 to A722. (see note 3)	Read/write
Power ON Clock Data 4 (see note 1, 2)	A729 to A731	These words contain the startup time/date for the fourth-to-last time that power was turned ON. The data is BCD and the storage format is the same as words A720 to A722. (see note 3)	Read/write
Power ON Clock Data 5 (see note 1, 2)	A732 to A734	These words contain the startup time/date for the fifth-to-last time that power was turned ON. The data is BCD and the storage format is the same as words A720 to A722. (see note 3)	Read/write
Power ON Clock Data 6 (See note 1) Power OFF Time History Data #1 (see note 2)	A735 to A737	These words contain the startup time/date for the sixth-to-last time that power was turned ON. In a CS1D Duplex-CPU System, this is the Power OFF Time data. (see note 3) The data is BCD and the storage format is the same as words A720 to A722.	Read/write
Power ON Clock Data 7 (See note 1) Power OFF Time History Data #2 (see note 2)	A738 to A740	These words contain the startup time/date for the seventh-to-last time that power was turned ON. In a CS1D Duplex-CPU System, this is the Power OFF Time data. (see note 3) The data is BCD and the storage format is the same as words A720 to A722.	Read/write
Power ON Clock Data 8 (See note 1) Power OFF Time History Data #3 (see note 2)	A741 to A743	These words contain the startup time/date for the eighth-to-last time that power was turned ON. In a CS1D Duplex-CPU System, this is the Power OFF Time data. (see note 3) The data is BCD and the storage format is the same as words A720 to A722.	Read/write
Power ON Clock Data 9 (See note 1) Power OFF Time History Data #4 (see note 2)	A744 to A746	These words contain the startup time/date for the ninth-to-last time that power was turned ON. In a CS1D Duplex-CPU System, this is the Power OFF Time data. (see note 3) The data is BCD and the storage format is the same as words A720 to A722.	Read/write
Power ON Clock Data 10 (See note 1) Power OFF Time History Data #5 (see note 2)	A747 to A749	These words contain the startup time/date for the tenth-to-last time that power was turned ON. In a CS1D Duplex-CPU System, this is the Power OFF Time data. (see note 3) The data is BCD and the storage format is the same as words A720 to A722.	Read/write

Note
1. CS1D-CPU□□SA only
2. CS1D Duplex-CPU System Unit version 1.2 or later
3. Since the Startup Time /Power OFF Time history of a CS1D Duplex-CPU System is registered while looping #1 to #5, it may not be saved in an order.

■ Battery Errors

Name	Address	Description	Access
Battery Error Flag (Non-fatal error)	A40204	ON if the CPU Unit's battery is disconnected or its voltage is low and the PLC Setup has been set to detect this error. (Detect Low Battery)	Read-only
Right CPU Unit Battery Error Flag (Duplex CPU Systems only)	A32411	ON if A40204 is ON in the right CPU Unit.	Read-only
Left CPU Unit Battery Error Flag (Duplex CPU Systems only)	A32413	ON if A40204 is ON in the left CPU Unit.	Read-only

File Memory Information

■ File Memory Information for Active CPU Unit or CPU Unit in Single CPU System

The following words and bits provide file memory status for Single CPU Systems or for the active CPU Unit in a Duplex CPU Systems. For a Only the Memory Card in the active CPU Unit is accessed. For information on the CPU Unit's file memory-related status, refer to *Read-only Words* in *Appendix B Auxiliary Area Allocations*.

Name	Address	Description	Access
Memory Card Type	A34300 to A34302	The Memory Card type is output to A34300 to A34302. (0 hex: No Memory Card; 4 hex: Flash ROM) With a Duplex CPU System, the information depends on the setting of duplex operation for the Memory Card, as shown below. • Memory Card duplex operation disabled: Memory Card type for active CPU Unit is stored. • Memory Card duplex operation enabled: Memory Card type is stored only when mounted in both CPU Units.	Read-only
EM File Memory Format Error Flag	A34306	Turns ON when a format error occurs in the first EM bank allocated for file memory in the CPU Unit. Turns OFF when formatting is completed normally.	Read-only
Memory Card Format Error Flag	A34307	ON when the Memory Card is not formatted or a formatting error has occurred in the active CPU Unit.	Read-only
File Transfer Error Flag	A34308	ON when an error occurred while writing data to file memory in the active CPU Unit.	Read-only
File Write Error Flag	A34309	ON when data cannot be written to file memory because it is write-protected or the data exceeds the capacity of the file memory in the active CPU Unit.	Read-only
File Read Error	A34310	ON when a file could not be read because of a malfunction (file is damaged or data is corrupted) in the active CPU Unit.	Read-only
File Missing Flag	A34311	ON when an attempt is made to read a file that doesn't exist or an attempt is made to write to a file in a directory that doesn't exist in the active CPU Unit.	Read-only
File Memory Operation Flag	A34313	ON while any of the following operations is being executed in the active CPU Unit. OFF when none of them are being executed. CMND instruction sending a FINS command to the local CPU Unit. FREAD/FWRIT instructions. Program replacement using the control bit in the Auxiliary Area. Simple backup operation.	Read-only
Accessing File Data Flag	A34314	ON while file data is being accessed in the active CPU Unit.	Read-only
Memory Card Detected Flag	A34315	ON when a Memory Card has been detected in the active CPU Unit. OFF when a Memory Card has not been detected.	Read-only

■ File Memory Information for Left CPU Unit (Duplex CPU Systems Only)

Name	Address	Description	Access
Memory Card Type	A34100 to A34102	Indicates the type of Memory Card, if any, installed in the left CPU Unit. 0 hex: No Memory Card, Flash ROM: 4 hex	Read-only
EM File Memory Format Error Flag	A34106	Turns ON when a format error occurs in the first EM bank allocated for file memory in the left CPU Unit. Turns OFF when formatting is completed normally.	Read-only

Name	Address	Description	Access
Memory Card Format Error Flag	A34107	ON when the Memory Card is not formatted or a formatting error has occurred in the left CPU Unit.	Read-only
File Transfer Error Flag	A34108	ON when an error occurred while writing data to file memory in the left CPU Unit.	Read-only
File Write Error Flag	A34109	ON when data cannot be written to file memory because it is write-protected or the data exceeds the capacity of the file memory in the left CPU Unit.	Read-only
File Read Error	A34110	ON when a file could not be read because of a malfunction (file is damaged or data is corrupted) in the left CPU Unit.	Read-only
File Missing Flag	A34111	ON when an attempt is made to read a file that doesn't exist or an attempt is made to write to a file in a directory that doesn't exist in the left CPU Unit.	Read-only
File Memory Operation Flag	A34113	ON while any of the following operations is being executed in the left CPU Unit. OFF when none of them are being executed. CMND instruction sending a FINS command to the local CPU Unit. FREAD/FWRIT instructions. Program replacement using the control bit in the Auxiliary Area. Simple backup operation.	Read-only
Accessing File Data Flag	A34114	ON while file data is being accessed in the left CPU Unit.	Read-only
Memory Card Detected Flag	A34115	ON when a Memory Card has been detected in the left CPU Unit. OFF when a Memory Card has not been detected.	Read-only

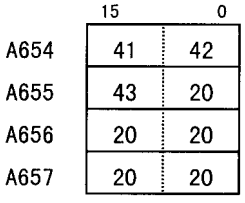
■ File Memory Information for Right CPU Unit (Duplex CPU Systems Only)

Name	Address	Description	Access
Memory Card Type	A34200 to A34202	Indicates the type of Memory Card, if any, installed in the right CPU Unit. 0 hex: No Memory Card, Flash ROM: 4 hex	Read-only
EM File Memory Format Error Flag	A34206	Turns ON when a format error occurs in the first EM bank allocated for file memory in the right CPU Unit. Turns OFF when formatting is completed normally.	Read-only
Memory Card Format Error Flag	A34207	ON when the Memory Card is not formatted or a formatting error has occurred in the right CPU Unit.	Read-only
File Transfer Error Flag	A34208	ON when an error occurred while writing data to file memory in the right CPU Unit.	Read-only
File Write Error Flag	A34209	ON when data cannot be written to file memory because it is write-protected or the data exceeds the capacity of the file memory in the right CPU Unit.	Read-only
File Read Error	A34210	ON when a file could not be read because of a malfunction (file is damaged or data is corrupted) in the right CPU Unit.	Read-only
File Missing Flag	A34211	ON when an attempt is made to read a file that doesn't exist or an attempt is made to write to a file in a directory that doesn't exist in the right CPU Unit.	Read-only
File Memory Operation Flag	A34213	ON while any of the following operations is being executed in the right CPU Unit. OFF when none of them are being executed. CMND instruction sending a FINS command to the local CPU Unit. FREAD/FWRIT instructions. Program replacement using the control bit in the Auxiliary Area. Simple backup operation.	Read-only

Name	Address	Description	Access
Accessing File Data Flag	A34214	ON while file data is being accessed in the right CPU Unit.	Read-only
Memory Card Detected Flag	A34215	ON when a Memory Card has been detected in the right CPU Unit. OFF when a Memory Card has not been detected.	Read-only

Other File Memory Information

Name	Address	Description	Access
Number of Items to Transfer	A346 to A347	These words contain the number of words or fields remaining to be transferred (8-digit hexadecimal). For binary files (.IOM), the value is decremented for each word that is read. For text (.TXT) or CSV (.CSV) data, the value is decremented for each field that is read.	Read-only
EM File Memory Starting Bank	A344	Contains the starting bank number of EM file memory (bank number of the first formatted bank). This number is read when starting to write data from a Memory Card. If the largest bank number for which there is an EM file for simple backup (BACKUPE□.IOM, where represents consecutive bank numbers) is the same as the largest bank number supported by the CPU Unit, the EM Area will be formatted as file memory using the value in A344. If the maximum bank numbers are different, the EM Area will be returned to it's unformatted (not file memory) status.	Read-only
Symbol Table File Flag (Unit version 4.0 or later)	A34501	Turns ON when the comment memory contains a symbol table file. 0: No file 1: File present	Read-only
Comment File Flag (Unit version 4.0 or later)	A34502	Turns ON when the comment memory contains a comment file. 0: No file 1: File present	Read-only
Program Index File Flag (Unit version 4.0 or later)	A34503	Turns ON when the comment memory contains a program index file. 0: No file 1: File present	Read-only
File Deletion Flags	A39506	The system automatically deleted the remainder of an EM file memory file that was being updated when a power interruption occurred.	Read-only
	A39507	The system automatically deleted the remainder of a Memory Card file that was being updated when a power interruption occurred.	Read-only
Simple Backup Write Capacity	A397	If a write for a simple backup operation fails, A397 will contain the Memory Card capacity that would have been required to complete the write operation. The value is in Kbytes. (This indicates that the Memory Card did not have the specified capacity when the write operation was started.) 0001 to FFFF hex: Write error (value indicates required capacity from 1 to 65,535 Kbytes). A397 will be cleared to 0000 hex when the write is completed successfully for a simple backup operation.	Read-only

Name	Address	Description	Access
Program Replacement End Code	A65000 to A65007	Normal End (i.e., when A65014 is OFF) 01 hex: Program file (.OBJ) replaced. Error End (i.e., when A65014 is ON) 00 hex: Fatal error 01 hex: Memory error 11 hex: Write-protected 12 hex: Program replacement password error 21 hex: No Memory Card 22 hex: No such file 23 hex: Specified file exceeds capacity (memory error). 31 hex: One of the following in progress: File memory operation User program write Operating mode change	Read-only
Replacement Error Flag	A65014	ON when the Replacement Start Bit (A65015) has been turned ON to replace the program, but there is an error. If the Replacement Start Bit is turned ON again, the Replacement Error Flag will be turned OFF.	Read/write
Replacement Start Bit	A65015	Program replacement starts when the Replacement Start Bit is turned ON if the Program Password (A651) is valid (A5A5 hex). Do not turn OFF the Replacement Start Bit during program replacement. When the power is turned ON or program replacement is completed, the Replacement Start Bit will be turned OFF, regardless of whether replacement was completed normally or in error. It is possible to confirm if program replacement is being executed by reading the Replacement Start Bit using a Programming Device, PT, or host computer.	Read/write
Program Password	A651	Store the password to replace a program. A5A5 hex: Replacement Start Bit (A65015) is enabled. Any other value: Replacement Start Bit (A65015) is disabled. When the power is turned ON or program replacement is completed, the Replacement Start Bit will be turned OFF, regardless of whether replacement was completed normally or in error.	Read/write
Program File Name	A654 to A657	When program replacement starts, the program file name will be stored in ASCII. File names can be specified up to eight characters in length excluding the extension. File names are stored in the following order: A654 to A657 (i.e., from the lowest word to the highest), and from the highest byte to the lowest. If a file name is less than eight characters, the lowest remaining bytes and the highest remaining word will be filled with spaces (20 hex). Null characters and space characters cannot be used within file names. Example: File name is ABC.OBJ 	Read/write

CPU Unit/Duplex Unit Setting

Name	Address	Description	Access
DIP Switch Setting Flag	A39512	Shows the ON/OFF status of the following switches depending on the system. Duplex CPU Systems: Status of the “A39512” switch on the DIP switch on the front of the Duplex Unit. Single CPU Systems: Status of the pin 6 on the DIP switch on the front of the CPU Unit.	Read-only

Initial Settings

Name	Address	Description	Access
I/O Response Times in Basic I/O Units	A22000 to A25915	Contains the current I/O response times for Basic I/O Units.	Read-only
Basic I/O Unit Information Bits	A05000 to A08915	These flags correspond to slots 0 to 8 on Racks 0 to 7 in order from slot 0 on Rack 0 to slot 8 on Rack 7. A flag will be ON when the fuse is burnt out in a Basic I/O Unit mounted in the corresponding slot.	Read-only

CPU Bus Unit Flags/Bits

Name	Address	Description	Access
CPU Bus Unit Initialization Flags	A30200 to A30215	These flags correspond to CPU Bus Units 0 to 15. A flag will be ON while the corresponding Unit is initializing after the power is turned ON or the Unit’s Restart Bit (A50100 to A50115) is turned ON.	Read-only
CPU Bus Unit Restart Bits	A50100 to A50115	These bits correspond to CPU Bus Units 0 to 15. Turn a bit from OFF to ON to restart the corresponding Unit. **Note:** After a Unit restarts, its CPU Bus Unit Initialization Flag (in A302) will go ON and this bit will be turned OFF by the system automatically after initialization. Do not turn this bit OFF from a Programming Device or the ladder program.	Read/write

Special I/O Unit Flags/Bits

Name	Address	Description	Access
Special I/O Unit Initialization Flags	A33000 to A33515	These flags correspond to Special I/O Units 0 to 95. A flag will be ON while the corresponding Unit is initializing after the power is turned ON or the Unit’s Restart Bit is turned ON. (Restart Bits A50200 to A50715 correspond to Units 0 to 95.)	Read-only
Special I/O Unit Restart Bits	A50200 to A50715	These bits correspond to Special I/O Units 0 to 95. Turn a bit from OFF to ON to restart the corresponding Unit. **Note:** After a Unit restarts, its Special I/O Unit Initialization Flag (in A330 to A335) will go ON and this bit will be turned OFF by the system automatically after initialization. Do not turn this bit OFF from a Programming Device or the ladder program.	Read/write

Inner Board Flags/Bits (Single CPU Systems or Process-control CPU Units)

Name	Address	Description	Access
Inner Board Monitoring Area	A35500 to A35915	The function of these words is defined in the Inner Board.	Read-only
Inner Board Restart Bit	A60800	Turn the bit from OFF to ON to restart the corresponding Inner Board.	Read/write
Inner Board User Interface Area	A60900 to A61315	This interface area can be used to transfer data from the CPU Unit to the Inner Board. The function of the data is defined in the Inner Board.	Read/write

Program Creation Flags

Name	Address	Description	Access
First Cycle Flag	A20011	This flag is turned ON for one cycle when program execution starts (the operating mode is switched from PROGRAM to RUN/MONITOR).	Read-only
Initial Task Execution Flag	A20015	When a task switches from INI to RUN status for the first time, this flag will be turned ON within the task for one cycle only.	Read-only
Task Started Flag	A20014	When a task switches from WAIT or INI to RUN status, this flag will be turned ON within the task for one cycle only. The only difference between this flag and A20015 is that this flag also turns ON when the task switches from WAIT to RUN status.	Read-only
10-ms Incrementing Free Running Timer (Unit version 4.0 or later)	A000	This word contains the system timer used after the power is turned ON. 0000 hex is set when the power is turned ON and this value is automatically incremented by 1 every 10 ms. The value returns to 0000 hex after reaching FFFF hex (655,350 ms), and then continues to be automatically incremented by 1 every 10 ms. **Note:** The timer will continue to be incremented when the operating mode is switched to RUN mode. Example: The interval can be counted between processing A and processing B without requiring timer instructions. This is achieved by calculating the difference between the value in A000 for processing A and the value in A000 for processing B. The interval is counted in 10 ms units.	Read-only
100-ms Incrementing Free Running Timer (Unit version 4.0 or later)	A001	This word contains the system timer used after the power is turned ON. 0000 hex is set when the power is turned ON and this value is automatically incremented by 1 every 100 ms. The value returns to 0000 hex after reaching FFFF hex (655,350 ms), and then continues to be automatically incremented by 1 every 10 ms. **Note:** The timer will continue to be incremented when the operating mode is switched to RUN mode.	Read-only
1-s Incrementing Free Running Timer (Unit version 4.0 or later)	A002	This word contains the system timer used after the power is turned ON. 0000 hex is set when the power is turned ON and this value is automatically incremented by 1 every 1 s. The value returns to 0000 hex after reaching FFFF hex (65,535 s), and then continues to be automatically incremented by 1 every 1 s. **Note:** The timer will continue to be incremented when the operating mode is switched to RUN mode.	Read-only

Cycle Time Information

Maximum Cycle Time	A262 to A263	These words contain the maximum cycle time in units of 0.1 ms. The time is updated every cycle and is recorded in 32-bit binary (0 to FFFF FFFF, or 0 to 429,496,729.5 ms). (A263 is the leftmost word.) (See note.)	Read-only
Present Cycle Time	A264 to A265	These words contain the present cycle time in units of 0.1 ms. The time is updated every cycle and is recorded in 32-bit binary (0 to FFFF FFFF, or 0 to 429,496,729.5 ms). (A265 is the leftmost word.) (See note.)	Read-only
Peripheral Processing Cycle Time (Single CPU Systems only)	A268	When Parallel Processing Mode (with or without synchronous access to I/O memory) is being used, this word contains the peripheral processing cycle time in binary. 0000 to 4E20 hex: 0.0 to 2,000.0 ms (unit: 0.1 ms) **Note:** If the cycle time exceeds 2,000.0 ms, then 4E20 hex will be stored.	Read-only

Note With a Single CPU System, this would be the same as the instruction execution cycle if Parallel Processing Mode is being used.

Task Information

Name	Address	Description	Access
Task Number when Program Stopped	A294	This word contains the task number of the task that was being executed when program execution was stopped because of a program error.	Read-only
Maximum Interrupt Task Processing Time (Single CPU Systems only)	A440	This word contains the maximum processing time for any interrupt task in binary (unit: 0.1 ms).	Read-only
Number of Task with Maximum Interrupt Task Processing Time (Single CPU Systems only)	A441	This word contains the number of the interrupt task that generated the maximum processing time in binary (8000 to 80FF hex). Bit 15 will turn ON when an interrupt has occurred. The lower two digits of the hexadecimal value correspond to the task number (00 to FF hex).	Read-only
IR/DR Operation between Tasks	A09914	Turn ON this bit to share index and data registers between all tasks. Turn OFF this bit to use separate index and data registers between in each task.	Read-only

Debugging Information

■ Online Editing

Name	Address	Description	Access
Online Editing Wait Flag	A20110	ON when an online editing process is waiting. (An online editing request was received while online editing was disabled.)	Read-only
Online Editing Processing Flag	A20111	ON when an online editing process is being executed.	Read-only
Online Editing Disable Bit Validator	A52700 to A52707	The Online Editing Disable Bit (A52709) is valid only when this byte contains 5A.	Read/write
Online Editing Disable Bit	A52709	Turn this bit ON to disable online editing. (A52700 to A52707 must be set to 5A.)	Read/write

■ Output Control

Name	Address	Description	Access
Output OFF Bit	A50015	Turn this bit ON to turn OFF all outputs from Basic I/O Units, Output Units, and Special I/O Units.	Read/write

■ Differentiate Monitor

Name	Address	Description	Access
Differentiate Monitor Completed Flag	A50809	ON when the differentiate monitor condition has been established during execution of differentiation monitoring.	Read/write

■ Data Tracing

Name	Address	Description	Access
Sampling Start Bit	A50815	When a data trace is started by turning this bit from OFF to ON from a Programming Device, the PLC will begin storing data in Trace Memory by one of the three following methods: 1) Periodic sampling (10 to 2,550 ms) 2) Sampling at execution of TRSM(045) 3) Sampling at the end of every cycle.	Read/write
Trace Start Bit	A50814	Turn this bit from OFF to ON to establish the trigger condition. The offset indicated by the delay value (positive or negative) determines which data samples are valid.	Read/write
Trace Busy Flag	A50813	ON when the Sampling Start Bit (A50815) is turned from OFF to ON. OFF when the trace is completed.	Read/write
Trace Completed Flag	A50812	ON when sampling of a region of trace memory has been completed during execution of a Trace. OFF when the next time the Sampling Start Bit (A50815) is turned from OFF to ON.	Read/write
Trace Trigger Monitor Flag	A50811	ON when a trigger condition is established by the Trace Start Bit (A50814). OFF when the next Data Trace is started by the Sampling Start bit (A50815).	Read/write

Program Error Information

Name	Address	Description	Access
Program Error Flag (Fatal error)	A40109	ON when program contents are incorrect. With a Single CPU System, CPU Unit operation will stop. With a Duplex CPU System in Duplex Mode, operation will switch to the standby CPU Unit and operation will continue. With a Duplex CPU System in Simplex Mode, CPU Unit operation will stop.	Read-only
Program Error Task	A294	Provides the type and number of the tack that was being executed when program execution stops as a result of a program error.	Read-only

Name	Address	Description	Access
Instruction Processing Error Flag	A29508	This flag and the Error Flag (ER) will be turned ON when an instruction processing error has occurred and the PLC Setup has been set to stop operation for an instruction error.	Read-only
Indirect DM/EM BCD Error Flag	A29509	This flag and the Access Error Flag (AER) will be turned ON when an indirect DM/EM BCD error has occurred and the PLC Setup has been set to stop operation an indirect DM/EM BCD error.	Read-only
Illegal Access Error Flag	A29510	This flag and the Access Error Flag (AER) will be turned ON when an illegal access error has occurred and the PLC Setup has been set to stop operation an illegal access error.	Read-only
No END Error Flag	A29511	ON when there isn't an END(001) instruction in each program within a task.	Read-only
Task Error Flag	A29512	ON when a task error has occurred. The following conditions will generate a task error. 1) There isn't an executable cyclic task. 2) There isn't a program allocated to the task.	Read-only
Differentiation Overflow Error Flag	A29513	ON when the specified Differentiation Flag Number exceeds the allowed value.	Read-only
Illegal Instruction Error Flag	A29514	ON when a program that cannot be executed has been stored.	Read-only
UM Overflow Error Flag	A29515	ON when the last address in UM (user program memory) has been exceeded.	Read-only
Program Address Where Program Stopped	A298 and A299	These words contain the 8-digit hexadecimal program address of the instruction where program execution was stopped due to a program error. (A299 contains the leftmost digits.)	Read-only

Error Information

■ Error Log, Error Code

Name	Address	Description	Access
Error Log Area	A100 to A199	When an error has occurred, the error code, error contents, and error's time and date are stored in the Error Log Area.	Read-only
Error Log Pointer	A300	When an error occurs, the Error Log Pointer is incremented by 1 to indicate the location where the next error record will be recorded as an offset from the beginning of the Error Log Area (A100).	Read-only
Error Log Pointer Reset Bit	A50014	Turn this bit ON to reset the Error Log Pointer (A300) to 00.	Read/write
Error Code	A400	When a non-fatal error (user-defined FALS(006) or system error) or a fatal error (user-defined FALS(007) or system error) occurs, the 4-digit hexadecimal error code is written to this word.	Read-only

■ **FAL/FALS Error Information**

Name	Address	Description	Access
FAL Error Flag (Non-fatal error)	A40215	ON when a non-fatal error is generated by executing FAL(006).	Read-only
Executed FAL Number Flags	A360 to A391	The flag corresponding to the specified FAL number will be turned ON when FAL(006) is executed. Bits A36001 to A39115 correspond to FAL numbers 001 to 511.	Read-only
FALS Error Flag (Fatal error)	A40106	ON when a fatal error is generated by the FALS(007) instruction. With a Single CPU System, CPU Unit operation will stop. With a Duplex CPU System in Duplex Mode, operation will switch to the standby CPU Unit and operation will continue. With a Duplex CPU System in Simplex Mode, CPU Unit operation will stop.	Read-only
FAL/FALS Number for System Error Simulation	A529	Set a dummy FAL/FALS number to use to simulate the system error using FAL(006) or FALS(007). 0001 to 01FF hex: FAL/FALS numbers 1 to 511 0000 or 0200 to FFFF hex: No FAL/FALS number for system error simulation. (No error will be generated.)	Read/write

■ **Memory Error Information**

Name	Address	Description	Access
Memory Error Flag (Fatal error)	A40115	ON when there was an error in automatic transfer from the Memory Card or an error occurred in memory when the power was turned ON. With a Single CPU System, CPU Unit operation will stop. With a Duplex CPU System in Duplex Mode, operation will switch to the standby CPU Unit and operation will continue. With a Duplex CPU System in Simplex Mode, CPU Unit operation will stop. The ERR/ALM indicator on the front of the CPU Unit will light. If the automatic data transfer at startup fails, A40309 will be turned ON. If an error occurs in automatic transfer at startup, this error cannot be cleared.	Read-only
Memory Error Location	A40300 to A40308 A40315	When a memory error occurs, the Memory Error Flag (A40115) is turned ON and one of the following flags is turned ON to indicate the memory area where the error occurred. A40300: User program A40304: PLC Setup A40305: Registered I/O Table A40307: Routing Table A40308: CPU Bus Unit Settings A40315: Duplex CPU compatible setting change error	Read-only
Startup Memory Card Transfer Error Flag	A40309	ON when an error occurs in automatically transferring a file from the Memory Card to the CPU Unit at startup, including when a file is missing or a Memory Card is not mounted. The error can be cleared by turning OFF the power. (This error cannot be cleared while the power is ON.)	Read-only
Flash Memory Error	A40310	Turns ON when the flash memory fails.	Read-only

■ **PLC Setup Error Information**

Name	Address	Description	Access
PLC Setup Error Flag (Non-fatal error)	A40210	ON when there is a setting error in the PLC Setup.	Read-only
PLC Setup Error Location	A406	When there is a setting error in the PLC Setup, the location of that error is written to A406 in 4-digit hexadecimal. The location is given as the address set on the Programming Console.	Read-only

■ **Interrupt Task Error Information (Single CPU Systems Only)**

Name	Address	Description	Access
Interrupt Task Error Flag (Non-fatal error)	A40213	ON when the Detect Interrupt Task Errors setting in the PLC Setup is set to “Detect” and one of the following occurs. IORD(222) or IOWR(223) in a cyclic task are competing with IORD(222) or IOWR(223) in an interrupt task. An interrupt task is executed for more than 10 ms during I/O refreshing of a C200H Special I/O Unit or a SYSMAC BUS I/O Unit. IORD(222) or IOWR(223) was executed in an interrupt task when I/O was being refreshed.	Read-only
Interrupt Task Error Cause Flag	A42615	Indicates the cause of an Interrupt Task Error.	Read-only
Interrupt Task Error, Task Number	A42600 to A42611	The function of these bits depends upon the status of A42615 (the Interrupt Task Error Cause Flag). A42615 OFF: Contains the interrupt task number when an interrupt task was executed for more than 10 ms during I/O refreshing of a C200H Special I/O Unit or a SYSMAC BUS Remote I/O Unit. A42615 ON: Contains the Special I/O Unit’s unit number when an attempt was made to refresh a Special I/O Unit’s I/O from an interrupt task with IORF(097) while the Unit’s I/O was being refreshed by cyclic I/O refreshing (duplicate refreshing).	Read-only

■ **I/O Information**

Name	Address	Description	Access
Basic I/O Unit Error Flag (Non-fatal error)	A40212	ON when an error has occurred in a Basic I/O Unit.	Read-only
Basic I/O Unit Error, Slot Number	A40800 to A40807	Contains the binary slot number where the error occurred when an error has occurred in a Basic I/O Unit.	Read-only
Basic I/O Unit Error, Rack Number	A40808 to A40815	Contains the binary rack number where the error occurred when an error has occurred in a Basic I/O Unit.	Read-only
I/O Setting Error Flag (Fatal error)	A40110	ON when an Input Unit has been installed in an Output Unit’s slot or vice-versa, so the Input and Output Units clash in the registered I/O table.	Read-only
I/O Verification Error Flag (Non-fatal error)	A40209	ON when a Basic I/O Unit registered in the I/O Table does not match the Basic I/O Unit actually installed in the PLC because a Unit was added or removed.	Read-only
Expansion I/O Rack Number Duplication Flags	A40900 to A40907	The corresponding flag will be turned ON when an Expansion I/O Rack’s starting word address was set from a Programming Device and two Racks have overlapping word allocations or a Rack’s starting address exceeds CIO 0901. Bits 00 to 07 correspond to Racks 0 to 7.	Read-only
Too Many I/O Points Flag (Fatal error)	A40111	ON when the number of I/O points being used in Basic I/O Units exceeds the maximum allowed for the PLC.	Read-only

Name	Address	Description	Access
Too Many I/O Points, Details	A40700 to A40712	The 2 possible causes of the Too Many I/O Points Error are listed below. The 3-digit binary value in A40713 to A40715 indicates the cause of the error. (The causes corresponding to values 0 to 5 are listed below.) • The number of I/O points will be written here when the total number of I/O points set in the I/O Table exceeds the maximum allowed for the CPU Unit. • The number of Racks will be written here when the number of Expansion I/O Racks exceeds the maximum. • Number of interrupt input points when there are more than 32 (Single CPU Systems only)	Read-only
Too Many I/O Points, Cause	A40713 to A40715	These three bits indicate the cause of the Too Many I/O Points Error. (See A40700 to A40712.) 000 (0): Too many I/O points 001: Too many interrupt input points 101 (5): Too many Expansion Racks connected	Read-only
I/O Bus Error Flag (Fatal error)	A40114	ON when an error occurs in a data transfer between the CPU Unit and a Unit mounted to a slot.	Read-only
I/O Bus Error Slot Number	A40400 to A40407	Contains the 8-bit binary slot number (00 to 08) where an I/O Bus Error occurred in binary (00 to 08 hex).	Read-only
I/O Bus Error Rack Number	A40408 to A40415	Contains the 8-bit binary rack number (00 to 07) where an I/O Bus Error occurred in binary (00 to 07 hex).	Read-only
Duplication Error Flag (Fatal error)	A40113	ON in the following cases: Two CPU Bus Units have been assigned the same unit number. Two Special I/O Units have been assigned the same unit number. Two Basic I/O Units have been allocated the same words. The same rack number is set for more than one Expansion Rack.	Read-only
I/O Table Creation Error Information	A261	Refer to information provided separately in this manual on I/O table creation.	

■ CPU Bus Unit Information

Name	Address	Description	Access
CPU Bus Unit Number Duplication Flags	A41000 to A41015	The Duplication Error Flag (A40113) and the corresponding flag in A410 will be turned ON when a CPU Bus Unit's unit number has been duplicated. Bits 00 to 15 correspond to unit numbers 0 to F.	Read-only
CPU Bus Unit Error, Unit Number Flags	A41700 to A41715	When an error occurs in a data exchange between the CPU Unit and a CPU Bus Unit, the CPU Bus Unit Error Flag (A40207) and the corresponding flag in A417 are turned ON. If the PLC Setup is set to turn ON the corresponding Error Unit Number Flag when a Special Unit (Special I/O Unit or CPU Bus Unit) is being replaced, the corresponding flag will be turned ON when the Unit is being replaced. If a duplexed CLK Unit is being replaced, the corresponding flag will be turned ON during replacement. Bits 00 to 15 correspond to unit numbers 0 to F.	Read-only
CPU Bus Unit Setting Error, Unit Number Flags	A42700 to A42715	When a CPU Bus Unit Setting Error occurs, A40203 and the corresponding flag in A27 are turned ON. Bits 00 to 15 correspond to unit numbers 0 to F.	Read-only
CPU Bus Unit Setting Error Flag (Non-fatal error)	A40203	ON when an installed CPU Bus Unit does not match the CPU Bus Unit registered in the I/O table.	Read-only
CPU Bus Unit Error Flag (Non-fatal error)	A40207	ON when an error occurs in a data exchange between the CPU Unit and a CPU Bus Unit (including an error in the CPU Bus Unit itself).	Read-only

■ **Special I/O Unit Information**

Name	Address	Description	Access
Special I/O Unit Number Duplication Flags	A41100 to A41615	The Duplication Error Flag (A40113) and the corresponding flag in A411 through A416 will be turned ON when a Special I/O Unit's unit number has been duplicated. (Bits A41100 to A41615 correspond to unit numbers 0 to 95.)	Read-only
Special I/O Unit Setting Error Flag (Non-fatal error)	A40202	ON when an installed Special I/O Unit does not match the Special I/O Unit registered in the I/O table.	Read-only
Special I/O Unit Setting Error, Unit Number Flags	A42800 to A43315	When a Special I/O Unit Setting Error occurs, A40202 and the corresponding flag in these words are turned ON. (Bits A42800 to A43315 correspond to unit numbers 0 to 95.)	Read-only
Special I/O Unit Error Flag (Non-fatal error)	A40206	ON when an error occurs in a data exchange between the CPU Unit and a Special I/O Unit (including an error in the Special I/O Unit itself).	Read-only
Special I/O Unit Error, Unit Number Flags	A41800 to A42315	When an error occurs in a data exchange between the CPU Unit and a Special I/O Unit, the Special I/O Unit Error Flag (A40206) and the corresponding flag in these words are turned ON. If the PLC Setup is set to turn ON the corresponding Error Unit Number Flag when a Special Unit (Special I/O Unit or CPU Bus Unit) is being replaced, the corresponding flag will be turned ON when the Unit is being replaced.	Read-only

■ **Inner Board Information (Single CPU Systems or Process-control CPU Units Only)**

Name	Address	Description	Access
Inner Board Error Flag (Non-fatal error)	A40208	ON when an error occurs in a data exchange between the CPU Unit and the Inner Board (including an error in the Inner Board itself).	Read-only
Inner Board Error Information	A42400 to A42415	When an error occurs in a data exchange between the CPU Unit and the Inner Board, the Inner Board Error Flag (A40208) and the appropriate error code will be written to A424.	Read-only
Fatal Inner Board Error Flag (Operation switched)	A40112	ON when there is an Inner Board Error (watchdog timer error). With a Single CPU System, CPU Unit operation will stop. With a Duplex CPU System in Duplex Mode, operation will switch to the standby CPU Unit and operation will continue. With a Duplex CPU System in Simplex Mode, CPU Unit operation will stop.	Read-only
Right-side Inner Board Error Flag (Non-fatal error) (Process-control CPU Units only)	A32406	ON when an Inner Board Error has occurred in the Inner Board in the CPU Unit on the right. A40208 will also turn ON.	Read-only
Left-side Inner Board Error Flag (Non-fatal error) (Process-control CPU Units only)	A32407	ON when an Inner Board Error has occurred in the Inner Board in the CPU Unit on the left. A40208 will also turn ON.	Read-only

■ **Other PLC Operating Information**

Name	Address	Description	Access
Cycle Time Overrun Flag (Operation switched)	A40108	ON if the cycle time exceeds the maximum cycle time set in the PLC Setup. (Watch Cycle Time) With a Single CPU System in Parallel Processing Mode, this will be the cycle time for instruction execution. With a Single CPU System, CPU Unit operation will stop. With a Duplex CPU System in Duplex Mode, operation will switch to the standby CPU Unit and operation will continue. With a Duplex CPU System in Simplex Mode, CPU Unit operation will stop.	Read-only
Peripheral Servicing Too Long Flag (Fatal error, Single CPU Systems only)	A40515	Turns ON when the peripheral servicing time exceeds 2 s. This will also cause a cycle time error and operation will stop.	Read-only
FPD Teaching Bit	A59800	Turn this bit ON to set the monitoring time in FPD(269) automatically with the teaching function.	Read/write
Memory Backup Battery Failure Flag	A39511	Data from the I/O memory areas that are maintained when power is turned OFF (HR, DM, etc.) are backed up with a Battery. A39511 turns ON if the Battery voltage drops and the data can no longer be maintained. The data in the I/O memory will not be dependable when this happens.	Read-only

Clock Information

Name	Address	Description	Access
Clock Data	The clock data from the clock built into the CPU Unit is stored here in BCD.		Read-only
	A35100 to A35107	Seconds: 00 to 59 (BCD)	Read-only
	A35108 to A35115	Minutes: 00 to 59 (BCD)	Read-only
	A35200 to A35207	Hour: 00 to 23 (BCD)	Read-only
	A35208 to A35215	Day of the month: 01 to 31 (BCD)	Read-only
	A35300 to A35307	Month: 01 to 12 (BCD)	Read-only
	A35308 to A35315	Year: 00 to 99 (BCD)	Read-only
	A35400 to A35407	Day of the week: 00: Sunday, 01: Monday, 02: Tuesday, 03: Wednesday, 04: Thursday, 05: Friday, 06: Saturday	Read-only

Flash Memory Backup Information

Name	Address	Description	Access
User Program Date	A090 to A093	These words contain in BCD the date and time that the user program was last overwritten. A09000 to A09007: Seconds (00 to 59) A09008 to A09015: Minutes (00 to 59) A09100 to A09107: Hour (00 to 23) A09108 to A09115: Day of month (01 to 31) A09200 to A09207: Month (01 to 12) A09208 to A09215: Year (00 to 99) A09308 to A09307: Day of the week (00: Sunday, 01: Monday, 02: Tuesday, 03: Wednesday, 04: Thursday, 05: Friday, 06: Saturday)	Read-only
Parameter Date	A094 to A0947	These words contain in BCD the date and time that the parameters were last overwritten. A09400 to A09407: Seconds (00 to 59) A09408 to A09415: Minutes (00 to 59) A09500 to A09507: Hour (00 to 23) A09508 to A09515: Day of month (01 to 31) A09600 to A09607: Month (01 to 12) A09608 to A09615: Year (00 to 99) A09708 to A09707: Day of the week (00: Sunday, 01: Monday, 02: Tuesday, 03: Wednesday, 04: Thursday, 05: Friday, 06: Saturday)	Read-only

Information on Read Protection Using a Password (Single CPU Systems Only)

Name	Address	Description	Access
UM Read Protection Flag	A09900	Indicates whether the entire user program in the PLC is read-protected. 0: UM not read-protected. 1: UM read-protected.	Read-only
Task Read Protection Flag	A09901	Indicates whether read protection is set for individual tasks. 0: Tasks not read-protected. 1: Tasks read-protected.	Read-only
Program Write Protection for Read Protection	A09902	Indicates whether the program is write-protected. 0: Write-enabled. 1: Write-protected.	Read-only
Enable/Disable Bit for Program Backup	A09903	Indicates whether creating a backup program file (.OBJ) is enabled or disabled. 0: Enabled. 1: Disabled.	Read-only

Note These bits/flags cannot be used for Duplex CPU Systems.

Communications

■ **Network Communications Information**

Name	Address	Description	Access
Communications Port Enabled Flags	A20200 to A20207	ON when a network instruction (SEND, RECV, CMND, or PMCR) or background processing (see note) can be executed with the corresponding port number. Bits 00 to 07 correspond to communications ports 0 to 7. When the simple backup operation is used to performed a write or compare operation for a Memory Card on a CS1D CPU Unit, a communications port will be automatically allocated, and the corresponding flag will be turned ON during the operation and turned OFF when the operation has been completed. **Note:** Background processing is supported by Single CPU Systems only.	Read-only
Communications Port Completion Codes	A203 to A210	These words contain the completion codes for the corresponding port numbers when network instructions (SEND, RECV, CMND, or PMCR) have been executed. Words A203 to A210 correspond to communications ports 0 to 7. When the simple backup operation is used to performed a write or compare operation for a Memory Card on a CS1D CPU Unit, a communications port will be automatically allocated, and a completion code will be stored in the corresponding word.	Read-only
Communications Port Error Flags	A21900 to A21907	ON when an error occurred during execution of a network instruction (SEND, RECV, CMND, or PMCR). Turns OFF then execution has been finished normally. Bits 00 to 07 correspond to communications ports 0 to 7. When the simple backup operation is used to performed a write or compare operation for a Memory Card on a CS1D CPU Unit, a communications port will be automatically allocated. The corresponding flag will be turned ON if an error occurs and will be turned OFF if the simple backup operation ends normally.	Read-only

■ **Information on Communications Instruction Execution with Automatic Allocation of Communications Ports**

Name	Address	Description	Access
Network Communications Port Allocation Enabled Flag	A20215	ON when a communications instruction can be executed with automatic port allocation and there is a communications port available for automatic allocation. **Note:** When 9 or more communications instructions are being used simultaneously, use this flag to confirm that a communications port is available for automatic allocation before executing the communications instructions.	Read-only
First Cycle Flags after Network Communications Finished	A21400 to A21407	When a communications instruction is executed with automatic port allocation, the corresponding flag is turned ON for just one cycle after communications have been completed. Bits 00 to 07 correspond to ports 0 to 7. Use the Used Communications Port Number stored in A218 to determine which flag to access. **Note:** These flags are not effective until the next cycle after the communications instruction is executed. Delay accessing them for at least one cycle.	Read-only
First Cycle Flags after Network Communications Error Flags	A21500 to A21507	When a communications instruction was executed with automatic port allocation and an error occurred, the corresponding flag is turned ON for just one cycle. Bits 00 to 07 correspond to ports 0 to 7. The cause of the error can be determined with the Communications Port Completion Codes stored in A203 to A210. Use the Used Communications Port Number stored in A218 to determine which flag to access. **Note:** These flags are not effective until the next cycle after the communications instruction is executed. Delay accessing them for at least one cycle.	Read-only
Network Communications Completion Code Storage Address	A216 to A217	When a communications instruction was executed with automatic port allocation, the response (completion) code for the communications instruction is automatically stored in the word with the PLC memory address specified in these words. **Note:** The PLC memory address specified here can be transferred to an index register in order to indirectly address the specified word and read the code.	Read-only
Used Communications Port Numbers	A218	When a communications instruction is executed with automatic port allocation, the allocated communications port number is stored in this word. Values 0000 to 0007 hex correspond to ports 0 to 7.	Read-only

■ **Information on Explicit Message Instructions (Single CPU Systems Only)**

Name	Address	Description	Access
Explicit Communications Error Flag	A21300 to A21307	Turn ON when an error occurs in executing an Explicit Message Instruction (EXPLT, EGATR, ESATR, ECHRD, or ECHWR). Bits 00 to 07 correspond to communications ports 0 to 7. The corresponding bit will turn ON both when the explicit message cannot be sent and when an error response is returned for the explicit message. The status will be maintained until the next explicit message communication is executed. The bit will always turn OFF when the next Explicit Message Instruction is executed.	Read-only
Network Communications Error Flag	A21900 to A21907	Turn ON if the explicit message cannot be sent when executing an Explicit Message Instruction (EXPLT, EGATR, ESATR, ECHRD, or ECHWR). Bits 00 to 07 correspond to communications ports 0 to 7. The corresponding bit will turn ON when the explicit message cannot be sent. The status will be maintained until the next explicit message communication is executed. The bit will always turn OFF when the next Explicit Message Instruction is executed.	Read-only
Network Communications Response Code	A203 to A210	The following codes will be stored when an Explicit Message Instruction (EXPLT, EGATR, ESATR, ECHRD, or ECHWR) has been executed. A203 to A210 correspond to communications ports 0 to 7. If the Explicit Communications Error Flag turns OFF, 0000 hex is stored. If the Explicit Communications Error Flag is ON and the Network Communications Error Flag is ON, the FINS end code is stored. If the Explicit Communications Error Flag is ON and the Network Communications Error Flag is OFF, the explicit message end code is stored. During communications, 0000 hex will be stored and the suitable code will be stored when execution has been completed. The code will be cleared when operation is started.	Read-only

■ **Peripheral Port Communications Information**

Name	Address	Description	Access
Peripheral Port Communications Error Flag	A39212	ON when a communications error has occurred at the peripheral port.	Read-only
Peripheral Port Restart Bit	A52601	Turn this bit ON to restart the peripheral port.	Read/write
Peripheral Port Settings Change Bit	A61901	ON while the peripheral port's communications settings are being changed.	Read/write
Peripheral Port Error Flags	A52808 to A52815	These flags indicate what kind of error has occurred at the peripheral port.	Read/write
Peripheral Port PT Communications Flags	A39400 to A39407	The corresponding bit will be ON when the peripheral port is communicating with a PT in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	Read-only
Peripheral Port PT Priority Registered Flags	A39408 to A39415	The corresponding bit will be ON for the PT that has priority when the peripheral port is communicating in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	Read-only

■ **RS-232C Port Communications Information**

Name	Address	Description	Access
RS-232C Port Communications Error Flag	A39204	ON when a communications error has occurred at the RS-232C port.	Read-only
RS-232C Port Restart Bit	A52600	Turn this bit ON to restart the RS-232C port.	Read/write
RS-232C Port Settings Change Bit	A61902	ON while the RS-232C port's communications settings are being changed.	Read/write
RS-232C Port Error Flags	A52800 to A52807	These flags indicate what kind of error has occurred at the RS-232C port.	Read/write
RS-232C Port Send Ready Flag (No-protocol mode)	A39205	ON when the RS-232C port is able to send data in no-protocol mode.	Read-only
RS-232C Port Reception Completed Flag (No-protocol mode)	A39206	ON when the RS-232C port has completed the reception in no-protocol mode.	Read-only
RS-232C Port Reception Overflow Flag (No-protocol mode)	A39207	ON when a data overflow occurred during reception through the RS-232C port in no-protocol mode.	Read-only
RS-232C Port PT Communications Flags	A39300 to A39307	The corresponding bit will be ON when the RS-232C port is communicating with a PT in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	Read-only
RS-232C Port PT Priority Registered Flags	A39308 to A39315	The corresponding bit will be ON for the PT that has priority when the RS-232C port is communicating in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	Read-only
RS-232C Port Reception Counter (No-protocol mode)	A39300 to A39315	Indicates (in binary) the number of bytes of data received when the RS-232C port is in no-protocol mode.	Read-only

■ **Serial Device Communications Information**

Name	Address	Description	Access
Communications Units 0 to 15, Ports 1 to 4 Settings Change Bits	A62001 to A63504	The corresponding flag will be ON when the settings for that port are being changed. (Bits 1 to 4 in A620 to A635 correspond to ports 1 to 4 in Communications Units 0 to 15.)	Read/write
Communications Board Ports 1 to 4 Settings Change Bits	A63601 to A63604	The corresponding flag will be ON when the settings for that port are being changed. (Bits 1 to 4 correspond to ports 1 to 4.)	Read/write

Instruction Information

Name	Address	Description	Access
Step Flag	A20012	ON for one cycle when step execution is started with STEP(008).	Read-only
Current EM Bank	A301	This word contains the current EM bank number in 4-digit hexadecimal.	Read-only
Macro Area Input Words	A600 to A603	When MCRO(099) is executed, it copies the input data from the specified source words (input parameter words) to A600 through A603.	Read/write
Macro Area Output Words	A604 to A607	After the subroutine specified in MCRO(099) has been executed, the results of the subroutine are transferred from A604 through A607 to the specified destination words (output parameter words).	Read/write
Differentiated Flag Number Maximum Value	A339 to A340	This word contains the value of the largest Differentiated Flag number used in the differentiated instructions.	Read-only

Background Execution Information (Single CPU Systems Only)

Name	Address	Description	Access
DR00 Output for Background Execution	A597	When a data register is specified as the output for an instruction processed in the background, A597 receives the output instead of DR00. 0000 to FFFF hex	Read-only
IR00 Output for Background Execution	A595 and A596	When an Index Register is specified as the output for an instruction processed in the background, A595 and A596 receive the output instead of IR00. 0000 0000 to FFFF FFFF hex (A596 contains the leftmost digits.)	Read-only
Equals Flag for Background Execution	A59801	Turns ON if matching data is found for an SRCH(181) instruction executed in the background.	Read-only
ER/AER Flag for Background Execution	A39510	Turns ON if an error or illegal access occurs during background execution. Turns OFF when power is turned ON or operation is started.	Read-only

Function Blocks Information (Unit version 4.0 or later)

Function Block Memory Information

Name	Address	Description	Access
FB Program Data Flag	A34500	Turns ON if the FB program memory contains FB program data. 0: No data 1: Data present	Read-only

OMRON FB Library Information (See note)

Name	Address	Description	Access
FB Communications Instruction Response Required	A58015	0: Not required 1: Required	Read-only
FB Communications Instruction Port No.	A58008 to A58011	0 to 7 hex: Communications port No. 0 to 7 F hex: Automatic allocation	Read-only
FB Communications Instruction Retries	A58000 to A58003	Automatically stores the number of retries in the FB communications instruction settings specified in the PLC Setup.	Read-only
FB Communications Instruction Response Monitoring Time	A581	Automatically stores the FB communications instruction response monitoring time set in the PLC Setup. 0001 to FFFF hex (Unit: 0.1 s; Range: 0.1 to 6553.5) 0000 hex: 2 s	Read-only
FB DeviceNet Communications Instruction Response Monitoring Time	A582	Automatically stores the FB DeviceNet communications instruction response monitoring time set in the PLC Setup. 0001 to FFFF hex (Unit: 0.1 s; Range: 0.1 to 6553.5) 0000 hex: 2 s	Read-only

Note These Auxiliary Area bits/words are not to be written by the user. The number of resends and response monitoring time must be set by the user in the FB communications instructions settings in the PLC Setup, particularly when using function blocks from the OMRON FB Library to execute FINS messages or DeviceNet explicit messages communications. The values set in the Settings for OMRON FB Library in the PLC Setup will be automatically stored in the related Auxiliary Area words A580 to A582 and used by the function blocks from the OMRON FB Library.

Duplex CPU Compatible Setting Information (CS1D-CPU67HA only)

Name	Address	Description	Access
CPU Unit Model Verification Error Flag	A31707	1 (ON) when the model of the two CPU Units does not match in the Duplex mode, or when the combination of the Duplex CPU compatible setting and CPU model is wrong.	Read-only
Duplex CPU Compatible Setting Operating Mode	A32700 to A32703	Indicates the mode in which the CPU Unit is currently operating in the Duplex CPU compatible setting. 0 hex: CPU model which does not support Duplex CPU compatible setting 1 hex: Not set 2 hex: CPU65H mode 3 hex: CPU67H mode	Read-only
Duplex CPU Compatible Setting DIP Switch Setting	A32704 to A32707	The Duplex CPU compatible setting made by the DIP switches is saved. 0 hex: CPU model which does not support Duplex CPU compatible setting 1 hex: Not set 2 hex: CPU65H mode 3 hex: CPU67H mode	Read-only
Duplex CPU Compatible Setting Change Error	A40315	1 (ON) when the Duplex CPU compatible setting is changed without executing Memory All Clear.	Read-only

8-12 TR (Temporary Relay) Area

The TR Area contains 16 bits with addresses ranging from TR0 to TR15. These temporarily store the ON/OFF status of an instruction block for branching. TR bits are useful when there are several output branches and interlocks cannot be used.

It is not necessary to consider TR bits when displaying ladder diagrams on the CX-Programmer.

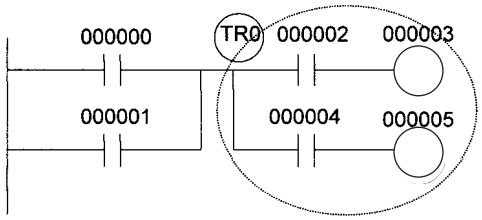
The TR bits can be used as many times as required and in any order required as long as the same TR bit is not used twice in the same instruction block.

TR bits can be used only with the OUT and LD instructions. OUT instructions (OUT TR0 to OUT TR15) store the ON OFF status of a branch point and LD instructions recall the stored ON OFF status of the branch point.

TR bits cannot be changed from a Programming Device.

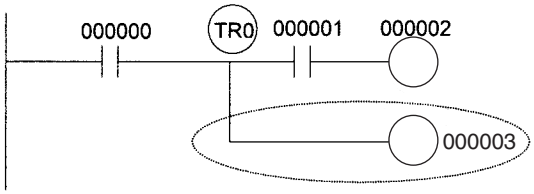
Examples

In this example, a TR bit is used when two outputs have been directly connected to a branch point.



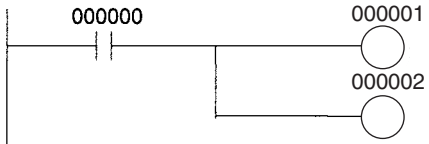
Instruction	Operand
LD	000000
OR	000001
OUT	TR 0
AND	000002
OUT	000003
LD	TR 0
AND	000004
OUT	000005

In this example, a TR bit is used when an output is connected to a branch point without a separate execution condition.

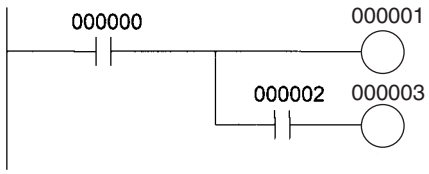


Instruction	Operand
LD	000000
OUT	TR 0
AND	000001
OUT	000002
LD	TR 0
OUT	000003

Note A TR bit is not required when there are no execution conditions after the branch point or there is an execution condition only in the last line of the instruction block.



Instruction	Operand
LD	000000
OUT	000001
OUT	000002



Instruction	Operand
LD	000000
OUT	000001
AND	000002
OUT	000003

8-13 Timer Area

The 4,096 timer numbers (T0000 to T4095) are shared by the TIM, TIMX, TIMH(015), TIMHX(551), TMHH(540), TMHHX(552), TTIM(087), TTIMX(555), TIMW(813), TIMWX(816), TMHW(815), and TMHWX(817) instructions. Timer Completion Flags and present values (PVs) for these instructions are accessed with the timer numbers. (The TIML(542), TIMLX(553), MTIM(543), and MTIMX(554) instructions do not use timer numbers.)

When a timer number is used in an operand that requires bit data, the timer number accesses the Completion Flag of the timer. When a timer number is used in an operand that requires word data, the timer number accesses the PV of the timer. Timer Completion Flags can be used as often as necessary as normally open and normally closed conditions and the values of timer PVs can be read as normal word data.

With CS1D CPU Units, the refresh method for timer PVs can be set from the CX-Programmer to either BCD or binary.

Note It is not recommended to use the same timer number in two timer instructions because the timers will not operate correctly if they are timing simultaneously. (If two or more timer instructions use the same timer number, an error will be generated during the program check, but the timers will operate as long as the instructions are not executed in the same cycle.)

The following table shows when timer PVs and Completion Flags will be reset.

Instruction name	Effect on PV and Completion Flag			Operation in Jumps and Interlocks	
	Mode change[1]	PLC start-up[2]	CNR(545) or CNRX(547)	Jumps (JMP-JME) or Tasks on standby[4]	Interlocks (IL-ILC)
TIMER: TIM or TIMX	PV → 0 Flag → OFF	PV → 0 Flag → OFF	PV → 9999 Flag → OFF	PV Maintained	PV → SV (Reset to SV.) Flag → OFF
HIGH-SPEED TIMER: TIMH(015) or TIMHX(551)					
ONE-MS TIMER: TMHH(540) or TMHHX(552)					
ACCUMULATIVE TIMER: TTIM(087) or TTIMX(555)					PV Maintained
TIMER WAIT: TIMW(813) or TIMWX(816)					---
HIGH-SPEED TIMER WAIT: TMHW(815) or TMHWX(817)					---

Note

1. If the IOM Hold BIt (A50012) is ON, the PV and Completion Flag will be retained when a fatal error occurs or the operating mode is changed from PROGRAM mode to RUN or MONITOR mode or vice-versa. The PV and Completion Flag will be cleared when power is cycled.
2. If the IOM Hold BIt (A50012) is ON and the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, the PV and Completion Flag will be retained when the PLC's power is cycled.
3. Since the TIML(542), TIMLX(553), MTIM(543), and MTIMX(554) instructions do not use timer numbers, they are reset under different conditions. Refer to the descriptions of these instructions for details.
4. The present value of TIM, TIMX, TIMH(015), TIMHX(551), TMHH(540), TMHHX(552), TIMW(813), TIMWX(816), TMHW(815), and TMHWX(817) timers are held when the timer is jumped between JMP and JME instructions or when in a task that is on standby.

Forcing Bit Status

Timer Completion Flags can be force-set and force-reset.

Timer PVs cannot be force-set or force-reset, although the PVs can be refreshed indirectly by force-setting/resetting the Completion Flag.

Timer Accuracy

CPU Units for Duplex Systems

Accuracy in Normal Operation

The following table shows the timer accuracy in normal operation.

Timer	Accuracy
TIMER: TIM or TIMX	−10 ms to Cycle time
HIGH-SPEED TIMER: TIMH(015) or TIMHX(551)	
ONE-MS TIMER: TMHH(540) or TMHHX(552)	
ACCUMULATIVE TIMER: TTIM(087) or TTIMX(555)	
MULTI-OUTPUT TIMER: MTIM(543) or MTIMX(554)	
TIMER WAIT: TIMW(813) or TIMWX(816)	
HIGH-SPEED TIMER WAIT: TMHW(815) or TMHWX(817)	

Accuracy when Switching from Duplex to Simplex Operation

The accuracy of timers may be longer in the first cycle after switching from duplex to simplex operation. The following table shows the timer accuracy in the first cycle after switching.

Timer	Accuracy
TIMER: TIM or TIMX	–20 ms to Cycle time
HIGH-SPEED TIMER: TIMH(015) or TIMHX(551)	
ONE-MS TIMER: TMHH(540) or TMHHX(552)	
ACCUMULATIVE TIMER: TTIM(087) or TTIMX(555)	
MULTI-OUTPUT TIMER: MTIM(543) or MTIMX(554)	
TIMER WAIT: TIMW(813) or TIMWX(816)	
HIGH-SPEED TIMER WAIT: TMHW(815) or TMHWX(817)	

CPU Units for Simplex Systems

The timer accuracy is the same as for the CS1-H CPU Units, as shown below.

Instructions	Timer error
TIM or TIMX	–10 to 0 ms
TIMH(015) or TIMHX(551)	
TMHH(540) or TMHHX(552)	–1 to 0 ms
TTIM(087) or TTIMX(555)	–10 to 0 ms
TIML(542) or TIMLX(553)	
MTIM(543) or MTIMX(554)	
TIMW(813) or TIMWX(816)	
TMHW(815) or TMHWX(817)	

8-14 Counter Area

The 4,096 counter numbers (C0000 to C4095) are shared by the CNT, CNTX, CNTR(012), CNTRX(548), CNTW(814), and CNTWX(818) instructions. Counter Completion Flags and present values (PVs) for these instructions are accessed with the counter numbers. The counter numbers are independent from the timer numbers used by timer instructions.

When a counter number is used in an operand that requires bit data, the counter number accesses the Completion Flag of the counter. When a counter number is used in an operand that requires word data, the counter number accesses the PV of the counter.

With CS1D CPU Units, the refresh method for counter PVs can be set from the CX-Programmer to either BCD or binary.

It is not recommended to use the same counter number in two counter instructions because the counters will not operate correctly if they are counting simultaneously. If two or more counter instructions use the same counter number, an error will be generated during the program check, but the counters will operate as long as the instructions are not executed in the same cycle.

The following table shows when counter PVs and Completion Flags will be reset.

Instruction name	Effect on PV and Completion Flag					
	Reset	Mode change	PLC startup	Reset Input	CNR(545) or CNRX(548)	Interlocks (IL-ILC)
COUNTER: CNT or CNTX	PV → 0000 Flag → OFF	Maintained	Maintained	Reset	Reset	Maintained
REVERSIBLE COUNTER: CNTR(012) or CNTRX(548)						
COUNTER WAIT: CNTW(814) or CNTWX(818)						

8-15 Data Memory (DM) Area

The DM Area contains 32,768 words with addresses ranging from D00000 to D32767. This data area is used for general data storage and manipulation and is accessible only by word.

Data in the DM Area is retained when the PLC's power is cycled or the PLC's operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

Although bits in the DM Area cannot be accessed directly, the status of these bits can be accessed with the BIT TEST instructions, TST(350) and TSTN(351).

Forcing Bit Status

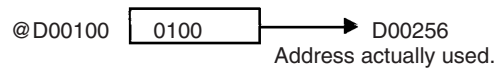
Bits in the DM Area cannot be force-set or force-reset.

Indirect Addressing

Words in the DM Area can be indirectly addressed in two ways: binary-mode and BCD-mode.

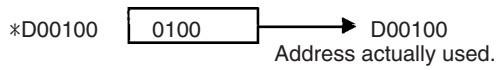
Binary-mode Addressing (@D)

When a "@" character is input before a DM address, the content of that DM word is treated as binary and the instruction will operate on the DM word at that binary address. The entire DM Area (D00000 to D32767) can be indirectly addressed with hexadecimal values 0000 to 7FFF.



BCD-mode Addressing (*D)

When a "*" character is input before a DM address, the content of that DM word is treated as BCD and the instruction will operate on the DM word at that BCD address. Only part of the DM Area (D00000 to D09999) can be indirectly addressed with BCD values 0000 to 9999.



DM Area Allocation to Special Units Inner Board

Parts of the DM Area are allocated to Special I/O Units, CPU Bus Units, and Inner Boards for functions such as initial Unit settings. The timing for data transfers is different for these Units, but may occur at any of the three following times.

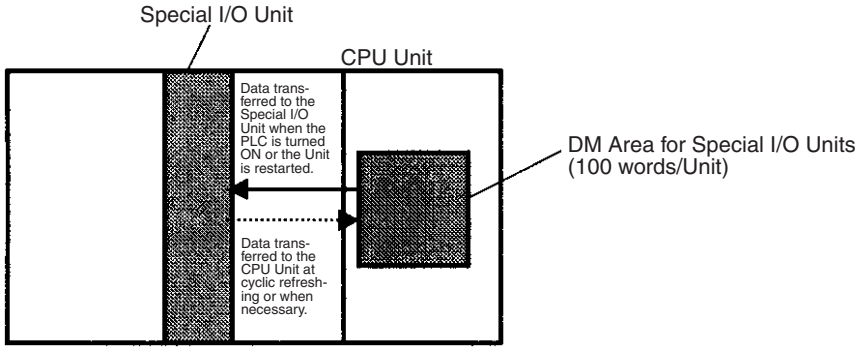
1,2,3...

1. Transfer data when the PLC's power is turned on or the Unit is restarted.
2. Transfer data once each cycle.
3. Transfer data when required.

Refer to the Unit's Operation Manual for details on data transfer timing.

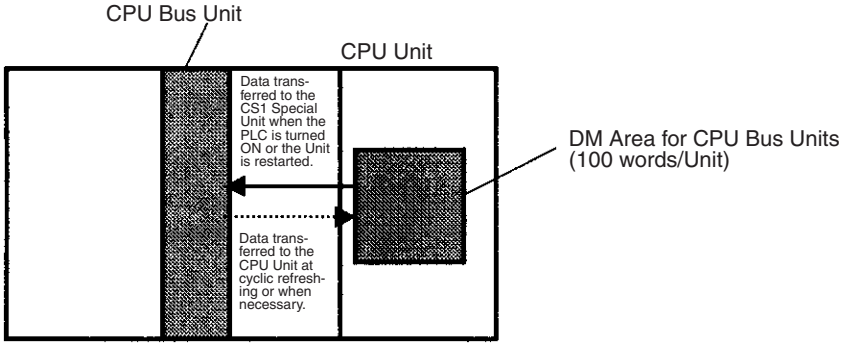
Special I/O Units (D20000 to D29599)

Each Special I/O Unit is allocated 100 words (based on unit numbers 0 to 95). Refer to the Unit's Operation Manual for details on the function of these words.



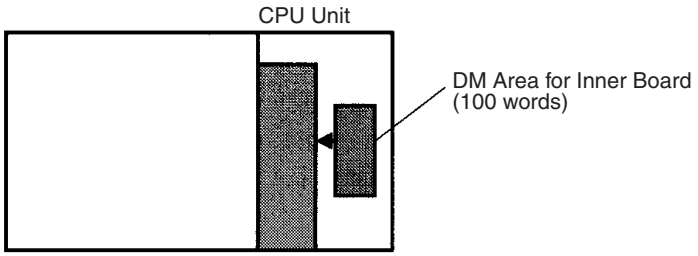
CPU Bus Units (D30000 to D31599)

Each CPU Bus Unit is allocated 100 words (based on unit numbers 0 to F). Refer to the Unit's Operation Manual for details on the function of these words. With some CPU Bus Units such as Ethernet Units, initial settings must be registered in the CPU Unit's Parameter Area; this data can be registered with a Programming Device other than a Programming Console.



Inner Board (D32000 to D32099)

The Inner Board is allocated 100 words. Refer to the Board's Operation Manual for details on the function of these words.



Note Inner Boards are supported for Single CPU Systems and Process-control CPU Units only.

8-16 Extended Data Memory (E18) Area

The EM Area is divided into 13 banks (0 to C) that each contain 32,768 words. EM Area addresses range from E0_00000 to E18_32767. This data area is used for general data storage and manipulation and is accessible only by word.

Data in the EM Area is retained when the PLC's power is cycled or the PLC's operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

Although bits in the EM Area cannot be accessed directly, the status of these bits can be accessed with the BIT TEST instructions, TST(350) and TSTN(351).

Forcing Bit Status

Bits in the EM Area cannot be force-set or force-reset.

Specifying EM Addresses

There are two ways to specify an EM address: the bank and address can be specified at the same time or an address in the current bank can be specified (after changing the current bank, if necessary). In general, we recommend specifying the bank and address simultaneously.

1,2,3...

1. Bank and Address Specification
   With this method, the bank number is specified just before the EM address. For example, E2_00010 specifies EM address 00010 in bank 2.
2. Current Bank Address Specification
   With this method, just the EM address is specified. For example, E00010 specifies EM address 00010 in the current bank. (The current bank must be changed with EMBC(281) to access data in another bank. A301 contains the current EM bank number.)

   The current bank will be reset to 0 when the operating mode is changed from PROGRAM mode to RUN/MONITOR mode, unless the IOM Hold Bit (A50012) is ON. The current bank is not changed as the program proceeds through cyclic tasks.

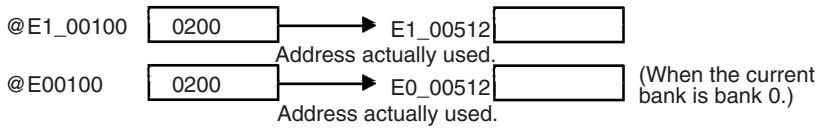
Indirect Addressing

Words in the EM Area can be indirectly addressed in two ways: binary-mode and BCD-mode.

Binary-mode Addressing (@E)

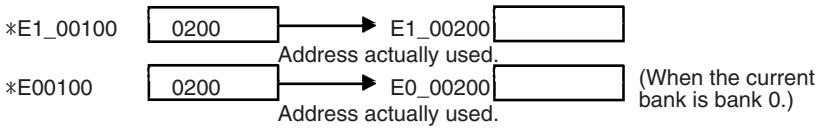
When a "@" character is input before a EM address, the content of that EM word is treated as binary and the instruction will operate on the EM word in the same bank at that binary address. All of the words in the same EM bank (E00000 to E32767) can be indirectly addressed with hexadecimal values

0000 to 7FFF and words in the next EM bank (E00000 to E32767) can be addressed with hexadecimal values 8000 to FFFF.



BCD-mode Addressing (*E)

When a "*" character is input before a EM address, the content of that EM word is treated as BCD and the instruction will operate on the EM word in the same bank at that BCD address. Only part of the EM bank (E00000 to E09999) can be indirectly addressed with BCD values 0000 to 9999.

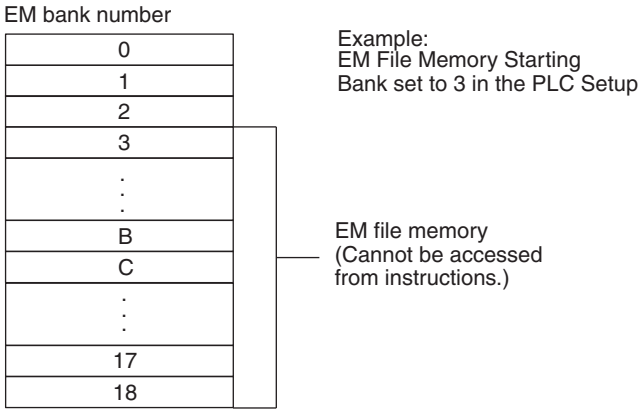


File Memory Conversion

Part of the EM Area can be converted for use as file memory with settings in the PLC Setup. All EM banks from the specified bank (EM File Memory Starting Bank) to the last EM bank will be converted to file memory.

Once EM banks have been converted to file memory, they cannot be accessed (read or written) by instructions. An Illegal Access Error will occur if a file-memory bank is specified as an operand in an instruction.

The following example shows EM file memory when the EM File Memory Starting Bank has been set to 3 in the PLC Setup.



8-17 Index Registers

The sixteen Index Registers (IR0 to IR15) are used for indirect addressing. Each Index Register can hold a single PLC memory address, which is the absolute memory address of a word in I/O memory. Use MOVR(560) to convert a regular data area address to its equivalent PLC memory address and write that value to the specified Index Register. (Use MOVRW(561) to set the PLC memory address of a timer/counter PV in an Index Register.)

Bits in Index Registers cannot be force-set or force-reset.

Note Refer to *Appendix E Memory Map* for more details on PLC memory addresses.

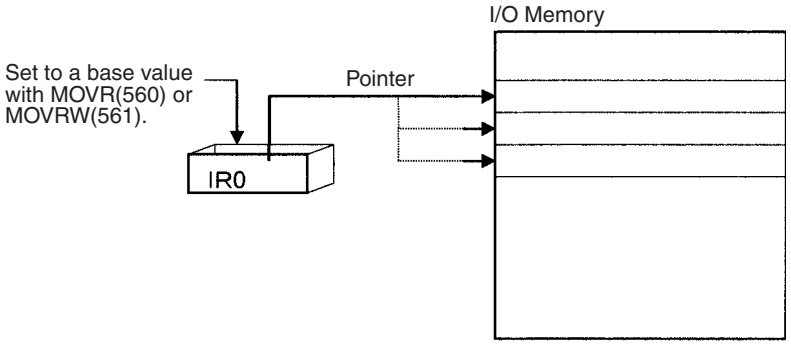
Indirect Addressing

When an Index Register is used as an operand with a "," prefix, the instruction will operate on the word indicated by the PLC memory address in the Index

Register, not the Index Register itself. Basically, the Index Registers are I/O memory pointers.

- All addresses in I/O memory (except Index Registers, Data Registers, and Condition Flags) can be specified seamlessly with PLC memory addresses. It isn't necessary to specify the data area.
- In addition to basic indirect addressing, the PLC memory address in an Index Register can be offset with a constant or Data Register, auto-incremented, or auto-decremented. These functions can be used in loops to read or write data while incrementing or decrementing the address by one each time that the instruction is executed.

With the offset and increment/decrement variations, the Index Registers can be set to base values with MOVR(560) or MOVRW(561) and then modified as pointers in each instruction.



Note It is possible to specify regions outside of I/O memory and generate an Illegal Access Error when indirectly addressing memory with Index Registers. Refer to *Appendix E Memory Map* for details on the limits of PLC memory addresses.

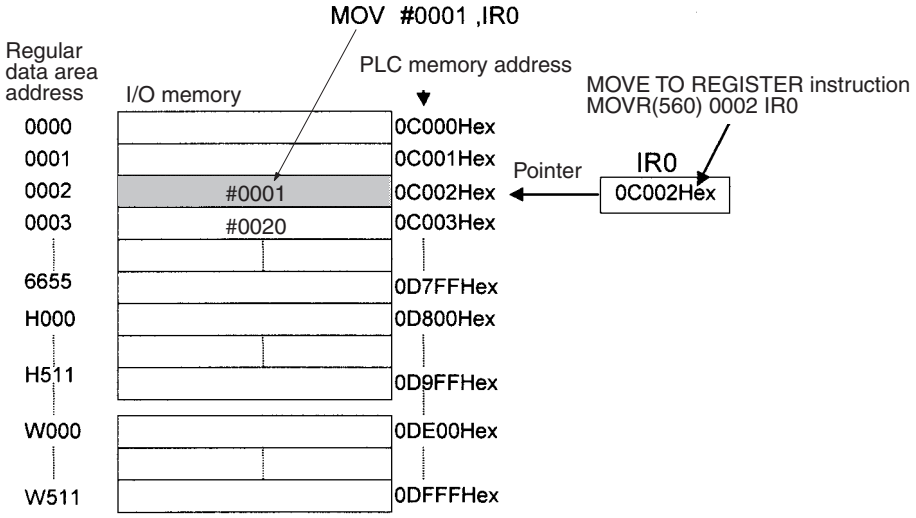
The following table shows the variations available when indirectly addressing I/O memory with Index Registers. (IR□ represents an Index Register from IR0 to IR15.)

Variation	Function	Syntax	Example	
Indirect addressing	The content of IR□ is treated as the PLC memory address of a bit or word.	,IR□	LD ,IR0	Loads the bit at the PLC memory address contained in IR0.
Indirect addressing with constant offset	The constant prefix is added to the content of IR□ and the result is treated as the PLC memory address of a bit or word. The constant may be any integer from –2,048 to 2,047.	Constant ,IR□ (Include a + or – in the constant.)	LD +5,IR0	Adds 5 to the contents of IR0 and loads the bit at that PLC memory address.
Indirect addressing with DR offset	The content of the Data Register is added to the content of IR□ and the result is treated as the PLC memory address of a bit or word.	DR□,IR□	LD DR0,IR0	Adds the contents of DR0 to the contents of IR0 and loads the bit at that PLC memory address.
Indirect addressing with auto-increment	After referencing the content of IR□ as the PLC memory address of a bit or word, the content is incremented by 1 or 2.	Increment by 1: ,IR□+ Increment by 2: ,IR□++	LD , IR0++	Loads the bit at the PLC memory address contained in IR0 and then increments the content of IR0 by 2.
Indirect addressing with auto-decrement	The content of IR□ is decremented by 1 or 2 and the result is treated as the PLC memory address of a bit or word.	Decrement by 1: ,–IR□ Decrement by 2: ,– –IR□	LD , – –IR0	Decrements the content of IR0 by 2 and then loads the bit at that PLC memory address.

Example

This example shows how to store the PLC memory address of a word (CIO 0002) in an Index Register (IR0), use the Index Register in an instruction, and use the auto-increment variation.

MOVR(560)	0002	IR0	Stores the PLC memory address of CIO 0002 in IR0.
MOV(021)	#0001	,IR0	Writes #0001 to the PLC memory address contained in IR0.
MOV(021)	#0020	+1,IR0	Reads the content of IR0, adds 1, and writes #0020 to that PLC memory address.



Note

1. The PLC memory addresses are listed in the diagram above, but it isn't necessary to know the PLC memory addresses when using Index Registers.
2. Auto-incrementing and auto-decrementing is performed when the instruction is executed. Caution is required when using instructions like OUT that are constantly executed. (Refer to *1-1 Operands* in *SYSMAC CS/CJ-series Programmable Controllers Instructions Reference Manual* (W474) for details.)

   Example:

   ```
   MOVR(560)    000013    IR0
   LD           P_Off
   OUT          ,IR0+
   ```

   Above, OUT turns OFF CIO 000013 and IR0 is incremented to indicate CIO 000014.

   ```
   MOVR(560)    000013    IR0
   LD           P_Off
   SET          ,IR0+
   ```

   SET is executed only when the input condition is ON. Thus SET is not executed above and IR0 is not incremented.

Since some operands are treated as word data and others are treated as bit data, the meaning of the data in an Index Register will differ depending on the operand in which it is used.

1,2,3...

1. Word Operand:

   ```
   MOVR(560)    0000      IR2
   MOV(021)     D00000    IR2
   ```

When the operand is treated as a word, the contents of the Index Register are used "as is" as the PLC memory address of a word.
In this example MOVR(560) sets the PLC memory address of CIO 0002 in IR2 and the MOV(021) instruction copies the contents of D00000 to CIO 0002.

2. Bit Operand:

```
MOVR(560)    000013    IR2
SET          +5,IR2
```

When the operand is treated as a bit, the leftmost 7 digits of the Index Register specify the word address and the rightmost digit specifies the bit number. In this example, MOVR(560) sets the PLC memory address of CIO 000013 (0C000D hex) in IR2. The SET instruction adds +5 from bit 13 to this PLC memory address, so it turns ON bit CIO 000102.

Index Register Initialization

The Index Registers will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa and the IOM Hold Bit is OFF.
2. The PLC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PLC Setup.

IOM Hold Bit Operation

If the IOM Hold Bit (A50012) is ON, the Index Registers won't be cleared when a FALS error occurs, when the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa, or when power supply recovers after a power interruption.

If the IOM Hold Bit (A50012) is ON, and the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, and if the Index Registers are not set to be shared between tasks (default setting), Index Registers will be held in the following way when power is interrupted. For tasks that were completed before power was interrupted, the values for the cycle during which power was interrupted will be held. For tasks that were not completed before power was interrupted, the values for the cycle before the cycle during which power was interrupted will be held. For example, in a program with three tasks, tasks 0, 1, and 2, if power is interrupted in the nth cycle during execution of task 1, then the execution result for the nth cycle of task 0 and the execution results for the (n–1)th cycle of tasks 1 and 2 will be held.

If the IOM Hold Bit (A50012) is ON, the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, and the Index Registers are set to be shared between tasks, Index Registers will not be held when the PLC's power supply is reset (ON →OFF →ON). The Index Registers may take undefined values. Be sure to set the values before continuing.

Direct Addressing

When an Index Register is used as an operand without a "," prefix, the instruction will operate on the contents of the Index Register itself (a two-word or "double" value). Index Registers can be directly addressed only in the instructions shown in the following table. Use these instructions to operate on the Index Registers as pointers.

With Single CPU Systems, the values of Index Registers are not stable when a interrupt task is started. When using Index Registers inside interrupt tasks, always MOVR (for all values except timer/counter PV) and MOVRW (for timer/counter PV) inside the interrupt tasks to set the values of the Index Registers.

The Index Registers cannot be directly addressed in any other instructions, although they can usually be used for indirect addressing.

Instruction group	Instruction name	Mnemonic
Data Movement Instructions	MOVE TO REGISTER	MOVR(560)
	MOVE TIMER/COUNTER PV TO REGISTER	MOVRW(561)
	DOUBLE MOVE	MOVL(498)
	DOUBLE DATA EXCHANGE	XCGL(562)
Table Data Processing Instructions	SET RECORD LOCATION	SETR(635)
	GET RECORD NUMBER	GETR(636)
Increment/Decrement Instructions	DOUBLE INCREMENT BINARY	++L(591)
	DOUBLE DECREMENT BINARY	– –L(593)
Comparison Instructions	DOUBLE EQUAL	=L(301)
	DOUBLE NOT EQUAL	< >L(306)
	DOUBLE LESS THAN	< L(311)
	DOUBLE LESS THAN OR EQUAL	< =L(316)
	DOUBLE GREATER THAN	> L(321)
	DOUBLE GREATER THAN OR EQUAL	> =L(326)
	DOUBLE COMPARE	CMPL(060)
Symbol Math Instructions	DOUBLE SIGNED BINARY ADD WITHOUT CARRY	+L(401)
	DOUBLE SIGNED BINARY SUBTRACT WITHOUT CARRY	–L(411)

The SRCH(181), MAX(182), and MIN(183) instructions can output the PLC memory address of the word with the desired value (search value, maximum, or minimum) to IR0. In this case, IR0 can be used in later instructions to access the contents of that word.

Precautions

Do not use Index Registers until a PLC memory address has been set in the register. The pointer operation will be unreliable if the registers are used without setting their values.

Each Index Register task is processed independently, so they do not affect each other. For example, IR0 used in Task 1 and IR0 used in Task 2 are different. Consequently, each Index Register task has 16 Index Registers.

Limitations when Using Index Registers

1,2,3...

1. It is only possible to read the Index Register for the last task executed within the cycle from the Programming Devices. If using Index Registers with the same number to perform multiple tasks, it is only possible with the Programming Devices to read the Index Register value for the last task performed within the cycle from the multiple tasks. Nor is it possible to write the Index Register value from the Programming Devices.
2. It is not possible to either read or write to the Index Registers using Host Link commands or FINS commands.

Index Registers can be shared between all tasks.

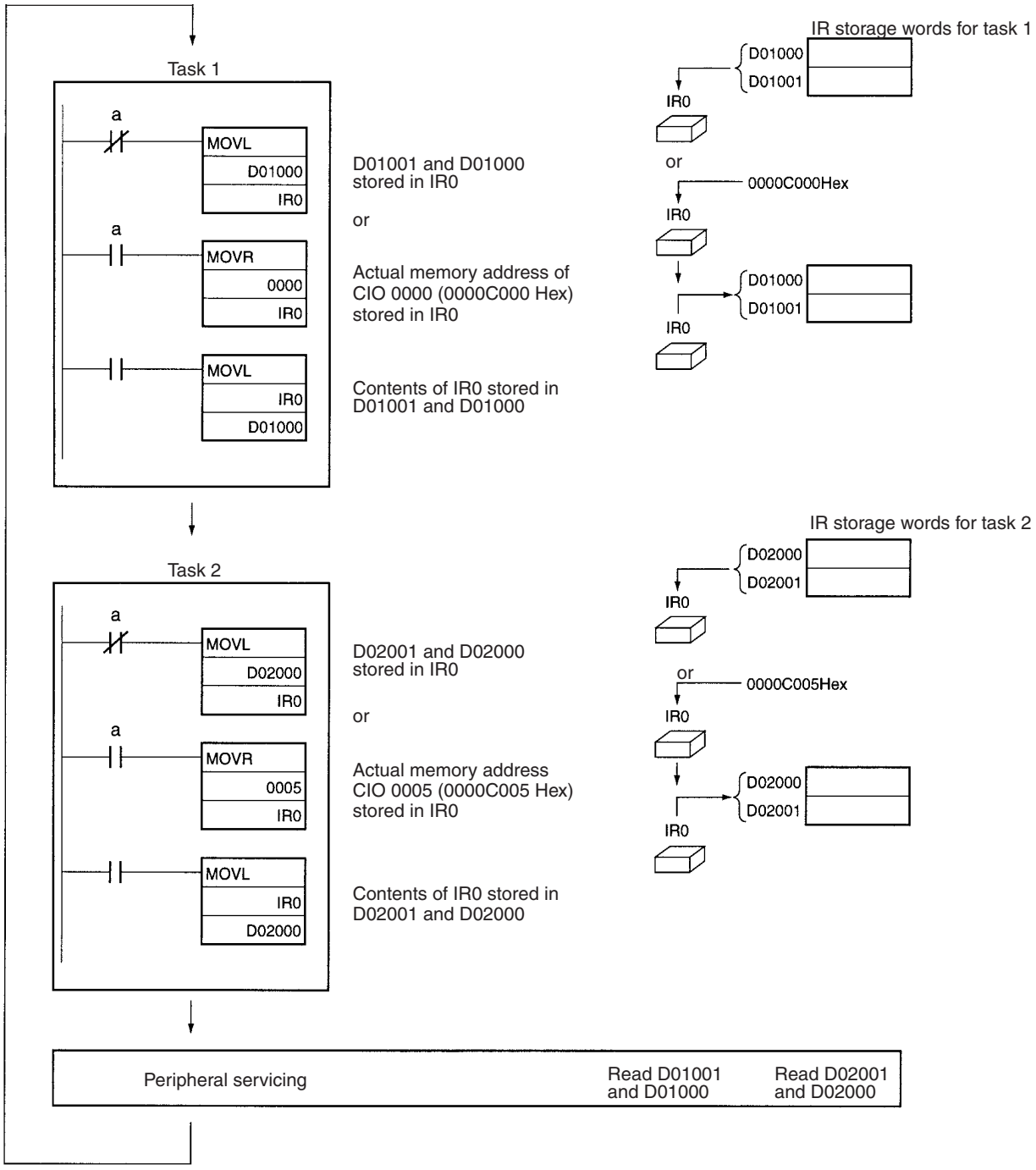
Monitoring and Sharing Index Registers

It is possible to monitor or share Index Registers as follows:

To use the Programming Devices to monitor the final Index Register values for each task, or to monitor the Index Register values using Host Link commands or FINS commands, write a program to store Index Register values from each task to another area (e.g., DM area) at the end of each task, and to

read Index Register values from the storage words (e.g., DM area) at the beginning of each task. The values stored for each task in other areas (e.g., DM area) can then be edited using the Programming Devices, Host Link commands, or FINS commands.

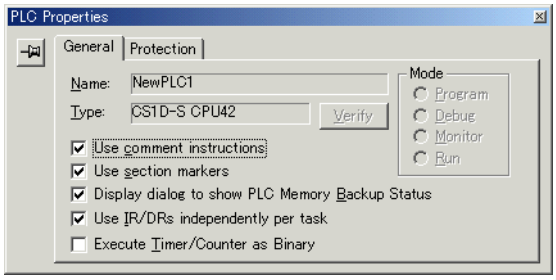
Note Be sure to use PLC memory addresses in Index Registers.



Sharing Index Registers

This setting can be made from the CX-Programmer.

To share Index Registers among tasks, remove the check from (deselect) the *Use IRs/DRs independently per task* Option.



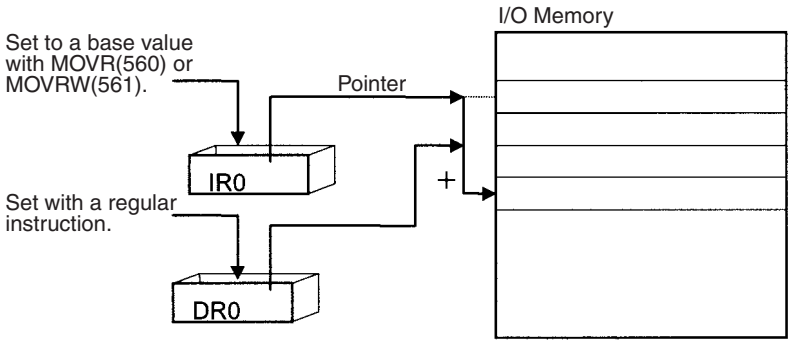
8-18 Data Registers

The sixteen Data Registers (DR0 to DR15) are used to offset the PLC memory addresses in Index Registers when addressing words indirectly.

The value in a Data Register can be added to the PLC memory address in an Index Register to specify the absolute memory address of a bit or word in I/O memory. Data Registers contain signed binary data, so the content of an Index Register can be offset to a lower or higher address.

Bits in Data Registers cannot be force-set or force-reset.

Regular instructions can be used to store data in Data Registers.



Examples

The following examples show how Data Registers are used to offset the PLC memory addresses in Index Registers.

LD DR0 ,IR0	Adds the contents of DR0 to the contents of IR0 and loads the bit at that PLC memory address.
MOV(021) #0001 DR0 ,IR1	Adds the contents of DR0 to the contents of IR1 and writes #0001 to that PLC memory address.

Range of Values

The contents of data registers are treated as signed binary data and thus have a range of –32,768 to 32,767.

Hexadecimal content	Decimal equivalent
8000 to FFFF	–32,768 to –1
0000 to 7FFF	0 to 32,767

Data Register Initialization

The Data Registers will be cleared in the following cases:

1,2,3...

1. The operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa and the IOM Hold Bit is OFF.

2. The PLC's power supply is cycled and the IOM Hold Bit is OFF or not protected in the PLC Setup.

IOM Hold Bit Operation

By default, data registers are cleared when power is interrupted or the CPU Unit is restarted.

If the IOM Hold Bit (A50012) is ON, the Data Registers won't be cleared when a FALS error occurs or the operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.

If the IOM Hold Bit (A50012) is ON, and the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, and if the Data Registers are not set to be shared between tasks (default setting), Data Registers will be held in the following way when power is interrupted. For tasks that were completed before power was interrupted, the values for the cycle during which power was interrupted will be held. For tasks that were not completed before power was interrupted, the values for the cycle before the cycle during which power was interrupted will be held. For example, in a program with three tasks, tasks 0, 1, and 2, if power is interrupted in the nth cycle during execution of task 1, then the execution result for the nth cycle of task 0 and the execution results for the (n–1)th cycle of tasks 1 and 2 will be held.

If the IOM Hold Bit (A50012) is ON, the PLC Setup's "IOM Hold Bit Status at Startup" setting is set to protect the IOM Hold Bit, and the Data Registers are set to be shared between tasks, Data Registers will not be held when the PLC's power supply is reset (ON →OFF →ON). The Data Registers may take undefined values. Be sure to set the values before continuing.

Forcing Bit Status

Bits in Data Registers **cannot** be force-set and force-reset.

Precautions

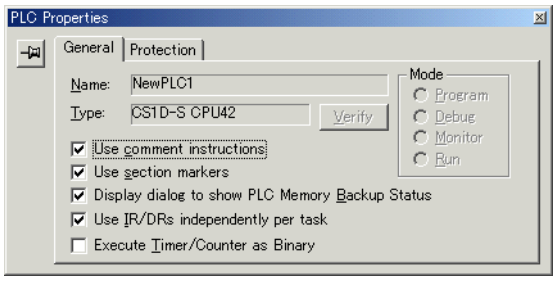
Data Registers are normally local to each task. For example, DR0 used in task 1 is different from DR0 used in task 2. A PLC Setup setting can be made from the CX-Programmer to share Data Registers between tasks.

The content of Data Registers cannot be accessed (read or written) from a Programming Device.

Do not use Data Registers until a value has been set in the register. The register's operation will be unreliable if they are used without setting their values.

Sharing Data Registers

The following setting can be made from the PLC properties dialog box on the CX-Programmer to control sharing index and data registers between tasks.



8-19 Task Flags

Task Flags range from TK00 to TK31 and correspond to cyclic tasks 0 to 31. A Task Flag will be ON when the corresponding cyclic task is in executable (RUN) status and OFF when the cyclic task hasn't been executed (INI) or is in standby (WAIT) status.

Note These flags indicate the status of cyclic tasks (including extra cyclic tasks).

Task Flag Initialization The Task Flags will be cleared in the following cases, regardless of the status of the IOM Hold Bit.

1,2,3...

1. The operating mode is changed from PROGRAM mode to RUN/MONITOR mode or vice-versa.
2. The PLC's power supply is cycled.

Forcing Bit Status The Task Flags **cannot** be force-set and force-reset.

8-20 Condition Flags

These flags include the Arithmetic Flags such as the Error Flag and Equals Flag which indicate the results of instruction execution. In earlier PLCs, these flags were in the SR Area.

The Condition Flags are specified with labels, such as CY and ER, or with symbols, such as P_Carry and P_Instr_Error, rather than addresses. The status of these flags reflects the results of instruction execution, but the flags are read-only; they cannot be written directly from instructions or Programming Devices.

Note The CX-Programmer treats condition flags as global symbols beginning with P_.

All Condition Flags are cleared when the program switches tasks, so the status of the ER and AER flags are maintained only in the task in which the error occurred.

Forcing Bit Status The Condition Flags **cannot** be force-set and force-reset.

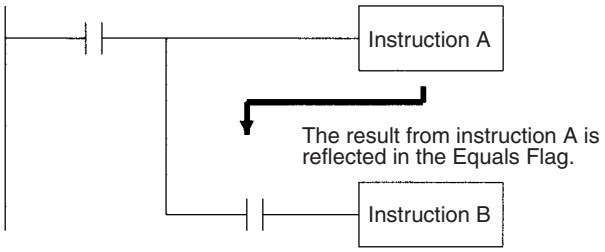
Summary of the Condition Flags The following table summarizes the functions of the Condition Flags, although the functions of these flags will vary slightly from instruction to instruction.

Refer to the description of the instruction for complete details on the operation of the Condition Flags for a particular instruction.

Name	Symbol	Label	Function
Error Flag	P_ER	ER	Turned ON when the operand data in an instruction is incorrect (an instruction processing error) to indicate that an instruction ended because of an error. When the PLC Setup is set to stop operation for an instruction error (Instruction Error Operation), program execution will be stopped and the Instruction Processing Error Flag (A29508) will be turned ON when the Error Flag is turned ON.
Access Error Flag	P_AER	AER	Turned ON when an Illegal Access Error occurs. The Illegal Access Error indicates that an instruction attempted to access an area of memory that should not be accessed. When the PLC Setup is set to stop operation for an instruction error (Instruction Error Operation), program execution will be stopped and the Instruction Processing Error Flag (A429510) will be turned ON when the Access Error Flag is turned ON.
Carry Flag	P_CY	CY	Turned ON when there is a carry in the result of an arithmetic operation or a "1" is shifted to the Carry Flag by a Data Shift instruction. The Carry Flag is part of the result of some Data Shift and Symbol Math instructions.
Greater Than Flag	P_GT	>	Turned ON when the first operand of a Comparison Instruction is greater than the second or a value exceeds a specified range.
Equals Flag	P_EQ	=	Turned ON when the two operands of a Comparison Instruction are equal the result of a calculation is 0.
Less Than Flag	P_LT	<	Turned ON when the first operand of a Comparison Instruction is less than the second or a value is below a specified range.
Negative Flag	P_N	N	Turned ON when the most significant bit (sign bit) of a result is ON.
Overflow Flag	P_OF	OF	Turned ON when the result of calculation overflows the capacity of the result word(s).
Underflow Flag	P_UF	UF	Turned ON when the result of calculation underflows the capacity of the result word(s).
Greater Than or Equals Flag	P_GE	>=	Turned ON when the first operand of a Comparison Instruction is greater than or equal to the second.
Not Equal Flag	P_NE	< >	Turned ON when the two operands of a Comparison Instruction are not equal.
Less Than or Equals Flag	P_LE	< =	Turned ON when the first operand of a Comparison Instruction is less than or equal to the second.
Always ON Flag	P_On	ON	Always ON. (Always 1.)
Always OFF Flag	P_Off	OFF	Always OFF. (Always 0.)

Using the Condition Flags

The Condition Flags are shared by all of the instructions, so their status may change often in a single cycle. Be sure to read the Condition Flags immediately after the execution of instruction, preferably in a branch from the same execution condition.



Instruction	Operand
LD	
Instruction A	
AND	=
Instruction B	

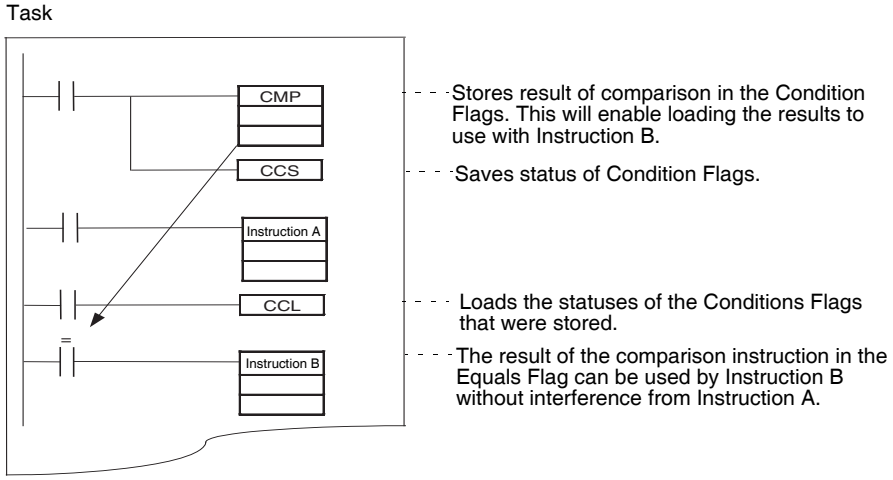
⚠ **Caution** Condition Flags can be tricky to use. They are manipulated by essentially all instructions and if they are not used with the proper timing, the wrong status may be read, leading to unexpected operation. Program Condition Flags with caution.

The Condition Flags are cleared when the program switches tasks, so the status of a Condition Flag cannot be passed to another task. For example the status of a flag in task 1 cannot be read in task 2. (The flag's status must be transferred to a bit.)

Saving and Loading Condition Flag Status

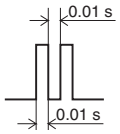
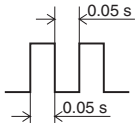
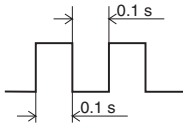
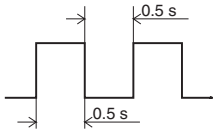
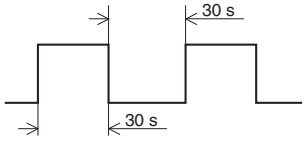
The CS1D CPU Units support instructions to save and load the Condition Flag status (CCS(282) and CCL(283)). These can be used to access the status of the Condition Flags at other locations in a task or in a different task.

The following example shows how the Equals Flag is used at a different location in the same task.



8-21 Clock Pulses

The Clock Pulses are flags that are turned ON and OFF at regular intervals by the system.

Name	Label	Symbol	Operation	
0.02 s Clock Pulse	0.02s	P_0_02_s		ON for 0.01 s OFF for 0.01 s
0.1 s Clock Pulse	0.1s	P_0_1s		ON for 0.05 s OFF for 0.05 s
0.2 s Clock Pulse	0.2s	P_0_2s		ON for 0.1 s OFF for 0.1 s
1 s Clock Pulse	1s	P_1s		ON for 0.5 s OFF for 0.5 s
1 min Clock Pulse	1min	P_1min		ON for 30 s OFF for 30 s

The Clock Pulses are specified with labels (or symbols) rather than addresses.

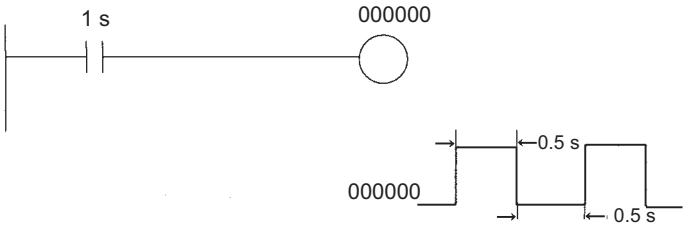
Note The CX-Programmer treats condition flags as global symbols beginning with P_.

The Clock Pulses are read-only; they cannot be overwritten from instructions or Programming Devices.

The Clock Pulses are cleared at the start of operation.

Using the Clock Pulses

The following example turns CIO 000000 ON and OFF at 0.5 s intervals.



Instruction	Operand
LD	1 s
OUT	000000

Clock Pulse Accuracy

The accuracy of the clock pulses is different for Duplex CPU Systems than for Single CPU Systems or CS1-H CPU Units.

Accuracy in Normal Operation

The following table shows the clock pulse accuracy in normal operation.

Timer	Accuracy
0.02 s Clock Pulse	±(10 ms + cycle time)
0.1 s Clock Pulse	
0.2 s Clock Pulse	
1 s Clock Pulse	
1 min Clock Pulse	

Accuracy when Switching from Duplex to Simplex Operation

The accuracy of the clock pulses may be longer in the first cycle after switching from duplex to simplex operation. The following table shows the clock pulse accuracy in the first cycle after switching.

Timer	Accuracy
0.02 s Clock Pulse	±(10 ms + cycle time) ±10 ms
0.1 s Clock Pulse	
0.2 s Clock Pulse	
1 s Clock Pulse	
1 min Clock Pulse	

8-22 Parameter Areas

Unlike the data areas in I/O memory which can be used in instruction operands, the Parameter Area can be accessed only from a Programming Device. The Parameter Area is made up of the following parts.

- The PLC Setup
- The Registered I/O Tables
- The Routing Table
- The CPU Bus Unit Settings

8-22-1 PLC Setup

The user can customize the basic specifications of the CPU Unit with the settings in the PLC Setup. The PLC Setup contains settings such as the serial port communications settings and minimum cycle time setting.

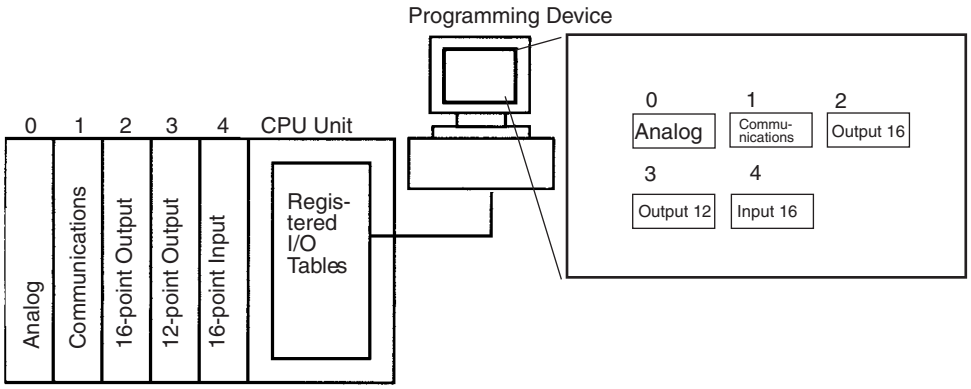
Refer to *SECTION 6 PLC Setup* for details on the PLC Setup settings and refer to the Programming Device's Operation Manual for details on changing these settings.

8-22-2 Registered I/O Tables

The Registered I/O Tables are tables in the CPU Unit that contain the information on the model and slot location of all of the Units mounted to the CPU Rack and Expansion I/O Racks. The I/O Tables are written to the CPU Unit with a Programming Device operation.

The CPU Unit allocates I/O memory to actual I/O points (on Basic I/O Units or Remote I/O Units) and CPU Bus Units based on the information in the Regis-

tered I/O Tables. Refer to the Programming Device's Operation Manual for details on registering the I/O Tables.

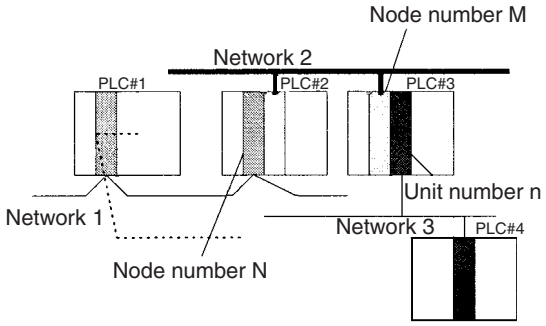


The I/O Verification Error Flag (A40209) will be turned ON if the models and locations of the Units actually mounted to the PLC (CPU Rack and Expansion I/O Racks) do not match the information in the Registered I/O Tables.

8-22-3 Routing Tables

When transferring data between networks, it is necessary to create a table in each CPU Unit that shows the communications route from the local PLC's Communications Unit to the other networks. These tables of communications routes are called "Routing Tables."

Create the Routing Tables with a Programming Device or the Controller Link Support Software and transfer the tables to each CPU Unit. The following diagram shows the Routing Tables used for a data transfer from PLC #1 to PLC #4.



1,2,3... 1. Relay Network Table of PLC #1:

Destination network	Relay network	Relay node
3	1	N

2. Relay Network Table of PLC #2:

Destination network	Relay network	Relay node
3	2	M

3. Local Network Table of PLC #3:

Local network	Unit number
3	n

Relay Network Table

This table lists the network address and node number of the first relay node to contact in order to reach the destination network. The destination network is reached through these relay nodes.

Local Network Table

This table lists the network address and unit number of the Communications Unit connected to the local PLC.

These are settings for the CPU Bus Units which are controlled by the CPU Unit. The actual settings depend on the model of CPU Bus Unit being used; refer to the Unit's Operation Manual for details.

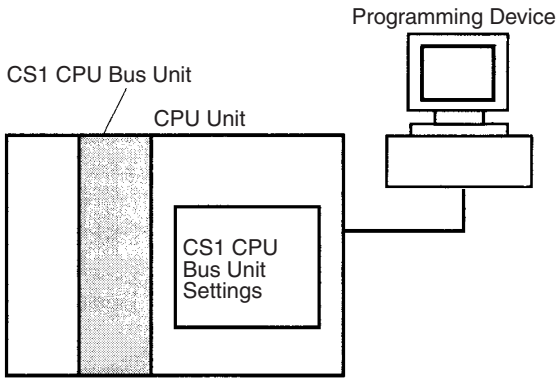
8-22-4 CPU Bus Unit Settings

These settings are not managed directly like the I/O memory's data areas, but are set from a Programming Device like the Registered I/O Tables.

Example 1: For Controller Link Units, user-set data link parameters and network parameters are managed as CPU Bus Unit settings.

Example 2: For Ethernet Units, the settings required to operate as an Ethernet node, such as the IP address table, are managed as CPU Bus Unit settings.

Refer to the Programming Device's Operation Manual for details on changing these settings.



SECTION 9
CPU Unit Operation and the Cycle Time

This section describes the internal operation of the CPU Unit and the cycle used to perform internal processing.

9-1 CPU Unit Operation

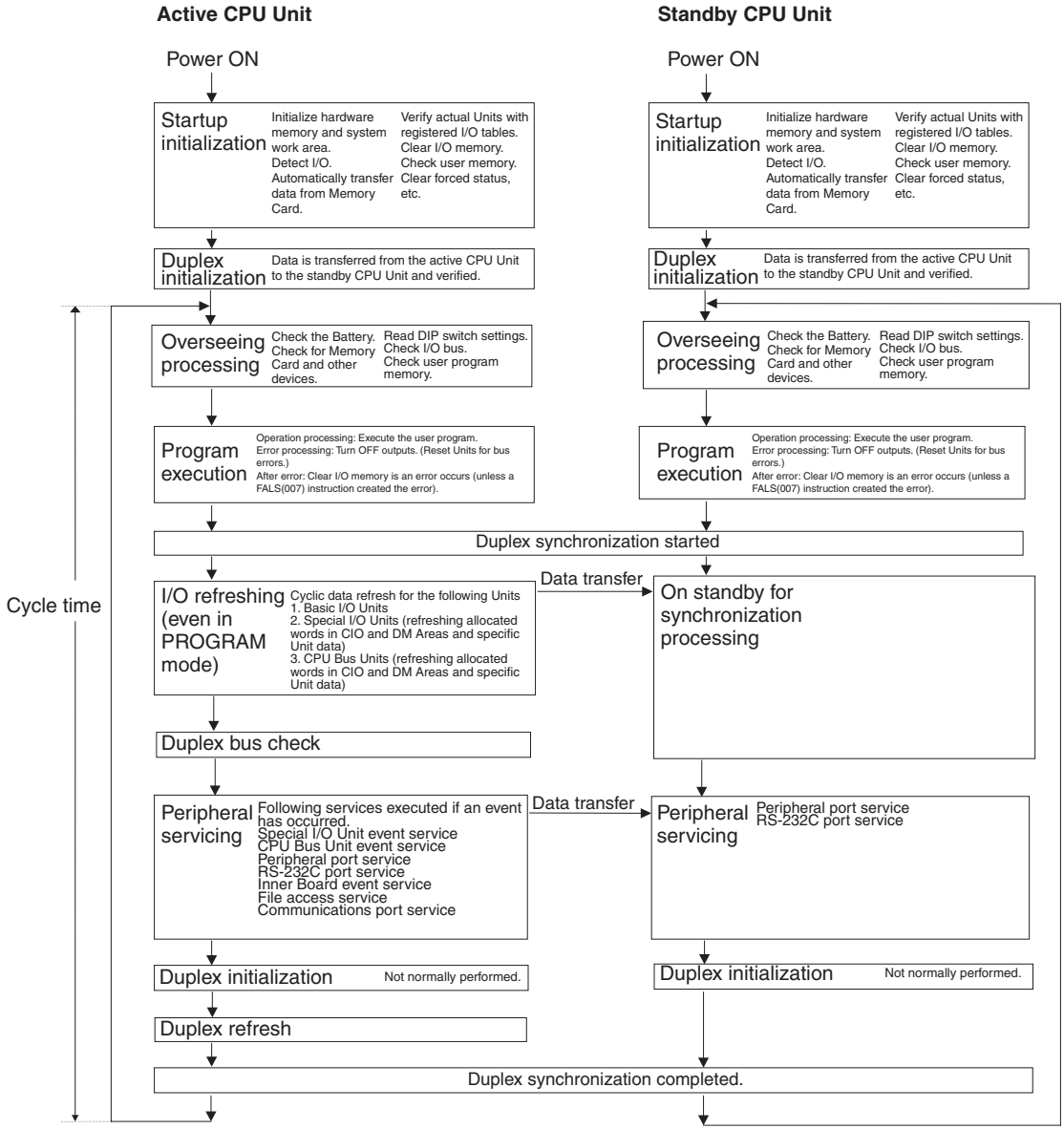
9-1-1 General Flow for Duplex CPU Systems

The following flowchart shows the overall operation of the CPU Units in a Duplex CPU System.

CPU Unit Operation Flow

This section describes the internal operation of the CPU Unit and the cycle used to perform internal processing. After the instructions in the user program have been executed, I/O is refreshed and peripherals are services. These operations are then repeated cyclically.

Note The CPU Units for Duplex CPU Systems do not support parallel processing modes.



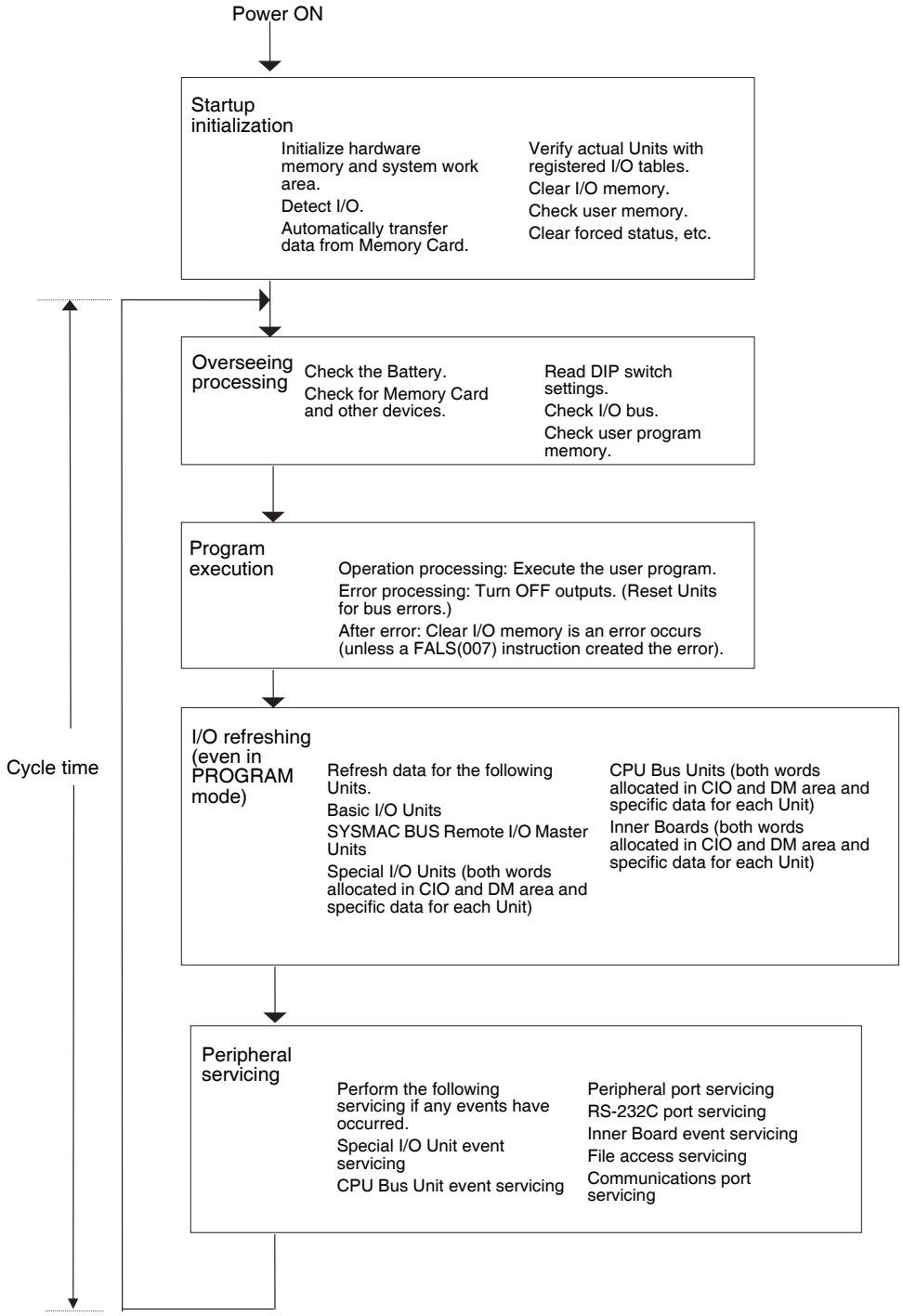
9-1-2 General Flow for Single CPU Systems

The following flowchart shows the overall operation of the CPU Unit.

Note The CPU Unit's processing mode is set to Normal Mode, Parallel Processing with Synchronous Memory Access, or Parallel Processing with Asynchronous Memory Access in the PLC Setup (Programming Console address 219, bits 08 to 15). This setting is also possible from the CX-Programmer.

Normal Mode for Single CPU Systems

In the normal mode, the program is executed before I/O is refreshed and peripherals are serviced. This cycle is executed repeatedly.



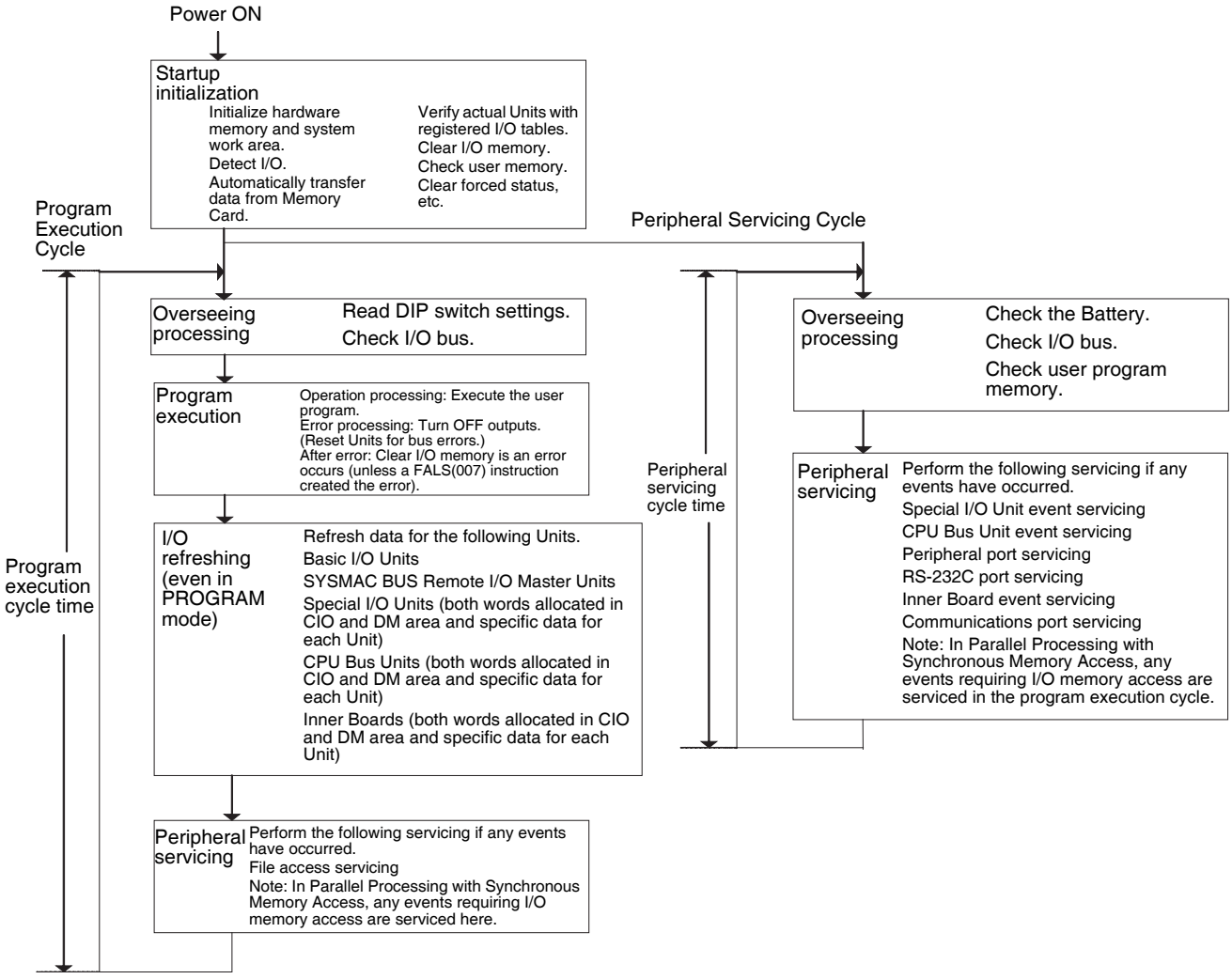
Parallel Processing (Single CPU Systems Only)

The following two types of processing are performed in parallel in either of the Parallel Processing Modes.

1,2,3... 1. Program execution: Includes user program execution and I/O refreshing. It is this cycle time that is monitored from a Programming Device.

2. Peripheral servicing: Programming Devices and events from Special I/O Units and CPU Bus Units are serviced when they occur.

There are two different Parallel Processing Modes. Parallel Processing with Synchronous Memory Access refreshes I/O memory in the program execution cycle and Parallel Processing with Asynchronous Memory Access refreshes I/O memory in the peripheral servicing cycle.



Note Always disconnect the Programming Console from the peripheral port during actual system operation in a Parallel Processing Mode. If the Programming Console is left attached, excess time will be allocated to increase key response for the Programming Console, adversely affecting performance.

9-1-3 I/O Refreshing and Peripheral Servicing

I/O Refreshing

I/O refreshing involves cyclically transferring data with external devices using preset words in memory. I/O refreshing includes the following:

- Refreshing the CIO Area for Basic I/O Units
- Refreshing Special I/O Units, CPU Bus Units, and Inner Boards, and the words allocated to these in the CIO Area (and for CPU Bus Units, words allocated in the DM Area)
- Refreshing specific data for the Special I/O Units, CPU Bus Units, and Inner Boards, such as data links and remote I/O communications.

All I/O refreshing is completed each cycle without time slicing. I/O is always refreshed after the instructions in the user program are executed.

Units			Max. data exchange	Data exchange area
Basic I/O Units			Depends on the Unit.	I/O Bit Area
Special I/O Units	Words allocated in CIO Area		10 words/Unit (Depends on the Unit.)	Special I/O Unit Area
CPU Bus Units	Words allocated in CIO Area		25 words/Unit	CPU Bus Unit Area
	Words allocated in DM Area		100 words/Unit	Words in DM Area allocated to CPU Bus Units
	Unit-specific data	Controller Link Unit and SYSMAC LINK Unit	Depends on the Unit.	Words set for data links (for either fixed or user-set allocations)
		CS-series DeviceNet Unit	Depends on the Unit.	Words set for remote I/O communications (for either fixed or user-set allocations)
		Serial Communications Unit	Depends on the protocol macros.	Communications data set for protocol macros
		Ethernet Unit	Depends on the Unit.	Communications data for socket services initiated by specific control bit operations.
Inner Boards (Single CPU Systems or Process-control CPU Units only)	Words allocated in CIO Area		100 words/Unit	Inner Board Area
	Unit-specific data	Inner Boards	Depends on the Board being used.	Depends on the Board being used.

Peripheral Servicing

Peripheral servicing involves servicing non-scheduled events for external devices. This includes both events from external devices and service requests to external devices.

Most peripheral servicing for CS1D PLCs involved FINS commands. The specific amount of time set in the system is allocated to each type of servicing

and executed every cycle. If all servicing cannot be completed within the allocated time, the remaining servicing is performed the next cycle.

Units	Servicing
Event servicing for Special I/O Units	Non-scheduled servicing for FINS commands from Special I/O Units, CPU Bus Units, and Inner Boards Non-scheduled servicing for FINS commands from the CPU Unit to the above Units
Event servicing for CPU Bus Units	
Event servicing for Inner Boards (Single CPU Systems or Process-control CPU Units only)	
Peripheral port servicing	Non-scheduled servicing for FINS or Host Link commands received via the peripheral or RS-232C ports from Programming Devices, PTs, or host computers (e.g., requests to transfer programming, monitoring, forced-set/reset operations, or online editing Non-scheduled servicing from the CPU Unit transmitted from the peripheral or RS-232C port (non-solicited communications)
RS-232C port servicing	
Communications port servicing	Servicing to execute network communications, serial communications, or file memory access for the SEND, RECV, CMND or PMCR instructions using communications ports 0 to 7 (internal logical ports)
File access servicing	File read/write operations for Memory Cards or EM file memory

Note

1. Special I/O Units, CPU Bus Units, RS-232C communications ports, Inner Boards, and file servicing is allocated 4% of the cycle time by default (the default can be changed). If servicing is separated over many cycles, delaying completion of the servicing, set the same allocated time (same time for all services) rather than a percentage under execute time settings in the PLC Setup.
2. In either of the Parallel Processing Modes for a Single CPU System, all peripheral servicing except for file access is performed in the peripheral servicing cycle.
3. If the cycle time is long and the response time from the CPU Unit exceeds the response monitoring time of the CX-Programmer, you may not be able to connect to the CX-Programmer. If you cannot connect to the CX-Programmer, increase the setting of the response monitoring time in the CX-Programmer. Right-click the PLC on the CX-Programmer and select ***Change***. The Change PLC Dialog Box will be displayed. Click the **Setting** Button for the network type and increase the response monitoring time on the Network Tab Page.

9-1-4 Initialization at Startup

The following initializing processes will be performed once each time the power is turned ON.

- Detect mounted Units.
- Compare the registered I/O tables and the actual Units.
- Clear the non-holding areas of I/O memory according to the status of the IOM Hold Bit. (See note 1.)
- Clear forced status according to the status of the Forced Status Hold Bit. (See note 2.)

- Autoboot using the autotransfer files in the Memory Card if one is inserted.
- Perform self-diagnosis (user memory check).
- Restore the user program (See note 3.)

Note 1. The I/O memory is held or cleared according to the status of the IOM Host Bit and the setting for IOM Hold Bit Status at Startup in the PLC Setup (read only when power is turned ON).

Auxiliary bit / PLC Setup setting		IOM Hold Bit (A50012)	
		Clear (OFF)	Hold (ON)
IOM Hold Bit Status at Startup (Programming Console address: Word 80, bit 15)	Clear (OFF)	At power ON: Clear At mode change: Clear	At power ON: Clear At mode change: Hold
	Hold (ON)		At power ON: Hold At mode change: Hold

Note I/O memory treatment depends on the status of the IOM Hold Bit at the time the operating mode is changed (to or from PROGRAM mode).

2. The forced status held or cleared according to the status of the Force Status Hold Bit and the setting for Forced Status Hold Bit Status at Startup in the PLC Setup.

Auxiliary bit / PLC Setup setting		Forced Status Hold Bit (A50013)	
		Clear (OFF)	Hold (ON)
Forced Status Hold Bit Status at Startup (Programming Console address: Word 80, bit 14)	Clear (OFF)	At power ON: Clear At mode change: Clear	At power ON: Clear At mode change: Hold
	Hold (ON)		At power ON: Hold At mode change: Hold

Note Force status treatment depends on the status of the Forced Status Hold Bit at the time the operating mode is changed (to or from PROGRAM mode).

3. If online editing is performed, but the power supply to the CPU Unit is turned OFF before the CPU Unit has completed backup processing, the user program will require restoring when the power supply is turned ON again. The BKUP indicator will light to indicate this. Refer to *6-6-10 Flash Memory* in the *Programming Manual* (W394) for details.

9-1-5 Duplex Initialization (Duplex CPU Systems Only)

The Duplex System is initialized when the power supply is turned ON, when operation is started, when the user program or PLC Setup is transferred, etc. It involves transferring data from the active CPU Unit to the standby CPU Unit and verifying that both CPU Units contain the same data. Duplex initialization is performed only in Duplex Mode.

Execution Timing and Processed Items

The following tables lists the items that are processed for duplex initialization and when each item is processed.

Event		Item								
		System verification (CPU models and Inner Boards)	**Program transfer**	**Program verification**	**Parameter area transfer**	**Parameter area verification**	**Inner Board setting transfer (Process-control CPU Units only)**	**Inner Board setting verification (Process-control CPU Units only)**	**I/O memory transfer (including EM Area)**	**Inner Board variable area transfer (Process-control CPU Units only)**
Power turned ON in Duplex Mode		Initialized	---	Initialized	---	Initialized	---	Initialized	Initialized	Initialized
Initialization button pressed in Duplex Mode		Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized
Operation started in Duplex Mode		Initialized	---	Initialized	---	Initialized	---	Initialized	Initialized	Initialized
FINS command executed	0202 hex: PARAMETER AREA WRITE	Initialized	---	---	Initialized	Initialized	---	---	Initialized	Initialized
	0203 hex: PARAMETER AREA CLEAR	Initialized	---	---	Initialized	Initialized	---	---	Initialized	Initialized
	0307 hex: PROGRAM AREA WRITE	Initialized	Initialized	Initialized	---	---	---	---	Initialized	Initialized
	0308 hex: PROGRAM AREA CLEAR	Initialized	Initialized	Initialized	---	---	---	---	Initialized	Initialized
	0321 hex: PROGRAM REPLACE/ DELETE	Initialized	Initialized	Initialized	---	---	---	---	Initialized	Initialized
	2104 hex: ONLINE UNIT REPLACEMENT	Initialized	---	---	Initialized	Initialized	---	---	Initialized	Initialized
	220B hex: PARAMETER AREA–FILE TRANSFER	Initialized	---	---	Initialized	Initialized	---	---	Initialized	Initialized
	220C hex: PROGRAM AREA–FILE TRANSFER	Initialized	Initialized	Initialized	---	---	---	---	Initialized	Initialized
CX-Programmer operations	PLC Setup transfer	Initialized	---	---	Initialized	Initialized	---	---	Initialized	Initialized
	I/O table transfer	Initialized	---	---	Initialized	Initialized	---	---	Initialized	Initialized
	Program transfer	Initialized	Initialized	Initialized	---	---	---	---	Initialized	Initialized
	Online editing	Initialized	Initialized	Initialized	---	---	---	---	Initialized	Initialized
	Unit online replacement	Initialized	---	---	Initialized	Initialized	---	---	Initialized	Initialized
Automatic transfer at startup (program and PLC Setup transfer)		Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized
Program replacement used during operation		Initialized	Initialized	Initialized	---	---	---	---	Initialized	Initialized
Inner Board settings changed (Process-control CPU Units only)		Initialized	---	---	---	---	Initialized	Initialized	Initialized	Initialized

Duplex operating status does not exist during duplex initialization (i.e., duplex initialization is performed in simplex operating status). This means that the active CPU Unit will not be switched. Because of this, operation will not continue if an error that would cause the CPU Unit to be switched occurs during duplex initialization, including CPU errors, memory errors, fatal Inner Board errors, program errors, exceeding the cycle time limit, and execution of FALS instructions).

Duplex Refreshing

Duplex refreshing is used to transfer errors detected by the active CPU Unit or the status of special flags and bits changed by the active CPU Unit to the standby CPU Unit. It is performed only in Duplex Mode.

9-2 CPU Unit Operating Modes

9-2-1 Operating Modes

The CPU Unit has three operating modes that control the entire user program and are common to all tasks.

PROGRAM: Programs are not executed and preparations, such as creating I/O tables, initializing the PLC Setup and other settings, transferring programs, checking programs, force-setting and force-resetting can be executed prior to program execution.

MONITOR: Programs are executed, but some operations, such as online editing, forced-set/reset, and changes to present values in I/O memory, are enabled for trial operation and other adjustments.

RUN: Programs are executed and some operations are disabled.

9-2-2 Status and Operations in Each Operating Mode

PROGRAM, RUN, and MONITOR are the three operating modes available in the CPU Unit. The following lists status and operations for each mode.

Overall Operation

Mode	Program (See note)	I/O refresh	External outputs	I/O Memory	
				Non-holding areas	Holding areas
PROGRAM	Stopped	Executed	OFF	Clear	Hold
RUN	Executed	Executed	Controlled by program	Controlled by program	
MONITOR	Executed	Executed	Controlled by program	Controlled by program	

Programming Console Operations

Mode	Monitor I/O Memory	Monitor Program	Transfer Program		Check Program	Create I/O Table
			PLC to Programming Device	Programming Device to PLC		
PROGRAM	**OK**	**OK**	**OK**	**OK**	**OK**	**OK**
MONITOR	**OK**	**OK**	**OK**	X	X	X
RUN	**OK**	**OK**	**OK**	X	X	X

Mode	PLC Setup	Modify program	Force-set/reset	Changing timer/ counter SV	Changing timer/ counter PV	Changing I/O memory PV	Unit online replacement
PROGRAM	**OK**	**OK**	**OK**	**OK**	**OK**	**OK**	**OK**
RUN	X	X	X	X	X	X	**OK**
MONITOR	X	**OK**	**OK**	**OK**	**OK**	**OK**	**OK**

Note The following table shows the relationship of operating modes to tasks.

Mode	Cyclic task status	Interrupt task status (See note.)
PROGRAM	Disabled status (INI)	Stopped
RUN MONITOR	• Any task that has not yet been executed, will be in disabled status (INI). • A task will go to READY status if the task is set to go to READY status at startup or the TASK ON (TKON) instruction has been executed for it. • A task in READY status will be executed (RUN status) when it obtains the right to execute. • A status will go to standby (WAIT) status if a READY task is put into Standby status by a TASK OFF (TKOF) instruction.	Executed if interrupt condition is met.

Note Interrupt tasks are supported only by Single CPU Systems and cannot be used in Duplex CPU Systems.

9-2-3 Operating Mode Changes and I/O Memory

Mode Changes	Non-holding areas	Holding Areas
	• I/O bits • Data Link bits • CPU Bus Unit bits • Special I/O Unit bits • Inner Board bits • DeviceNet bits • Work bits • Timer PV/Completion Flags • Index Registers • Data Registers • Task Flags (Auxiliary Area bits/words are holding or non-holding depending on the address.)	• HR Area • DM Area • EM Area Counter PV and Completion Flags (Auxiliary Area bits/words are holding or non-holding depending on the address.)
RUN or MONITOR to PROGRAM	Cleared (See note 1.)	Held
PROGRAM to RUN or MONITOR	Cleared (See note 1.)	Held
RUN to MONITOR or MONITOR to RUN	Held (See note 2.)	Held

Note 1. The following processing is performed depending on the status of the I/O Memory Hold Bit. Output from Output Units will be turned OFF when operation stops even if I/O bit status is held in the CPU Unit.

2. The cycle time will increase by approximately 10 ms when the operating mode is changed from MONITOR to RUN mode. This will not, however, cause an error for exceeding the maximum cycle time limit.

I/O Memory Hold Bit status (A50012)	I/O Memory			Output bits allocated to Output Units		
	Mode changed between PROGRAM and RUN/ MONITOR	Operation stopped		Mode changed between PROGRAM and RUN/ MONITOR	Operation stopped	
		Fatal error other than FALS	FALS executed		Fatal error other than FALS	FALS executed
OFF	Cleared	Cleared	Held	OFF	OFF	OFF
ON	Held	Held	Held	Held	OFF	OFF

Refer to *8-2 I/O Memory Areas* for more details on I/O Memory.

9-3 Power OFF Operation

The following processing is performed if CPU Unit power is turned OFF. Power OFF processing will be performed if the power supply falls below 85% of the rated voltage while the CPU Unit is in RUN or MONITOR mode.

1,2,3... 1. The CPU Unit will stop.

2. Outputs from all Output Units will be turned OFF.

Note All output will turn OFF despite an I/O Memory Hold Bit or I/O Memory Hold Bit at power ON settings in the PLC Setup.

85% of the rated voltage:
AC power: 85 V for a 100 V AC system and 170 V for a 200 V AC system

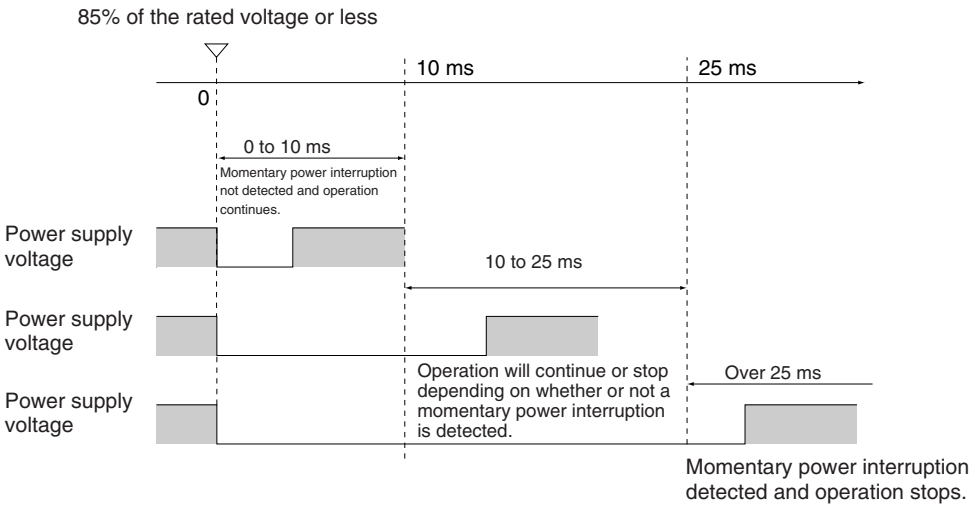
The following processing will be performed if power drops only momentarily (momentary power interruption).

1,2,3... 1. The system will continue to run unconditionally if the momentary power interruption lasts less than 10 ms, i.e., the time it takes the rated voltage at 85% or less to return to 85% or higher is less than 10 ms.

2. A momentary power interruption that lasts more than 10 ms but less than 25 ms is difficult to determine and a power interruption may or may not be detected.

3. The system will stop unconditionally if the momentary power interruption lasts more than 25 ms.

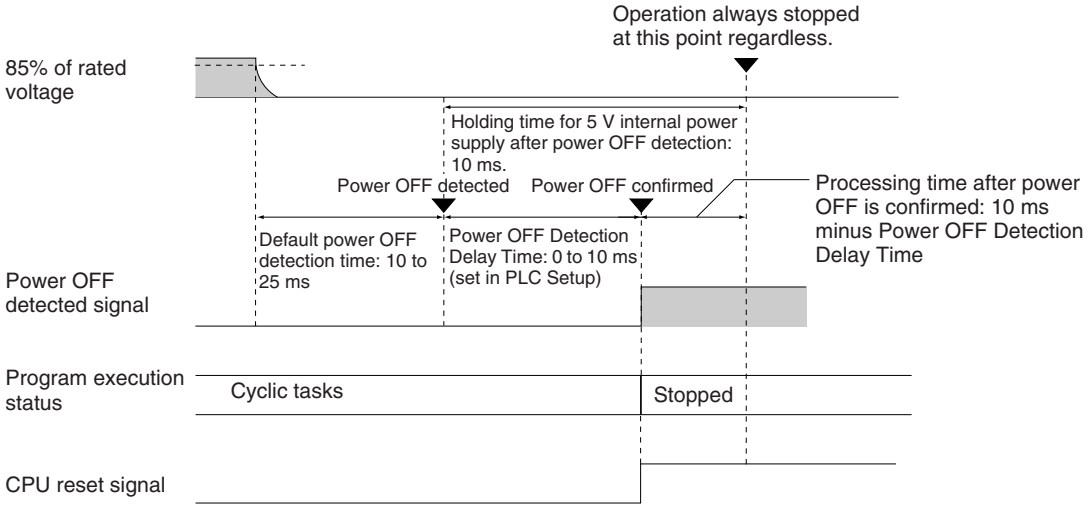
If operation stops under the conditions given in items 2 and 3 above, the timing used to stop operation can be delayed by setting the Power OFF Detection Delay Time (0 to 10 ms) in the PLC Setup. Operation, however, will always be stopped 10 to 25 ms after detecting a momentary power interruption regardless of the setting in the PLC Setup.



Note The above timing chart shows an example when the power OFF detection time is set to 0 ms (the default value).

The following timing chart shows the CPU Unit power OFF operation in more detail.

Power OFF Timing Chart



Power OFF Detection Time
The time it takes to detect power OFF after the power supply falls below 85% of the rated voltage.

Power OFF Detection Delay Time
The delay time after power OFF is detected until it is confirmed. This can be set in the PLC Setup within a range from 0 to 10 ms. (The default is 0 ms.)

Power Holding Time
The maximum amount of time (fixed at 10 ms) that 5 V will be held internally after power shuts OFF.

Description of Operation

1,2,3... 1. Power OFF will be detected if the 100 to 120 V AC or 200 to 240 V AC power supply falls below 85% of the rated voltage for the power OFF detection time (somewhere between 10 to 25 ms).

2. If the Power OFF Detection Delay Time is set (0 to 10 ms in 1-ms increments) in the PLC Setup, the CPU reset signal will turn ON while the internal power supply is maintained and the CPU Unit will be reset.

   Note a) Power OFF interrupt tasks cannot be used in Duplex CPU Systems.

   b) Power OFF interrupt tasks are supported only by Single CPU Systems. However, the CPU reset signal will turn ON and the CPU will be reset after the power OFF interrupt task has been executed. Make sure that the power OFF interrupt task will finish executing within 10 ms minus the Power OFF Detection Delay Time = processing time after power OFF. The 5-V internal power supply will be maintained only for 10 ms after power OFF is detected.

Note If you use an uninterruptible power supply (UPS), use one with a sine wave output. Do not use one with a rectangular wave output. Also, make sure that the UPS switching time for a power interruption is shorter than the power OFF detection time of the PLC. If the PLC's power OFF detection time is shorter than the UPS switching time, the PLC will detect the power interruption and stop operation before the UPS supplies backup power. You can delay the PLC's power OFF detection time by setting the Power OFF Detection Delay Time in the PLC Setup.

9-3-1 Instruction Execution for Power Interruptions

If power is interrupted and the interruption is confirmed when the CPU Unit is operating in RUN or MONITOR mode, the instruction currently being executed will be completed (see note) and the following power interruption processing will be performed.

- If the power OFF interrupt task has not been enabled, the CPU Unit will be reset immediately.
- If the power OFF interrupt task has been enabled, the task will be executed and then the CPU Unit will be reset immediately.

Note

1. The current instruction can be completed only when the time required to complete execution is less than or equal to the processing time after power interruption detection (10 ms – power interruption detection delay time). If the instruction is not completed within this time, it will be interrupted and the above processing will be performed.
2. Power OFF interrupt tasks are supported only by Single CPU Systems and cannot be used in Duplex CPU Systems.

Disabling Power Interruption Processing in the Program

Areas of the program can be protected from power interruptions so that the instructions will be executed before the CPU Unit even if the power supply is interrupted. This is achieved by using the DISABLE INTERRUPTS (DI(693)) and ENABLE INTERRUPTS (EI(694)) instructions. Using these instructions must be enabled in the PLC Setup.

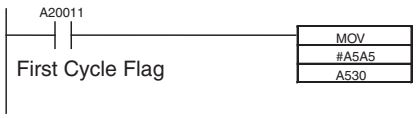
The following procedure is used.

1,2,3...

1. Insert DI(693) before the program section to be protected to disable interrupts and then place EI(694) after the section to enable interrupts.
2. Set the Disable Setting for Power OFF Interrupts in A530 to A5A5 hex to enable disabling power interruption processing.

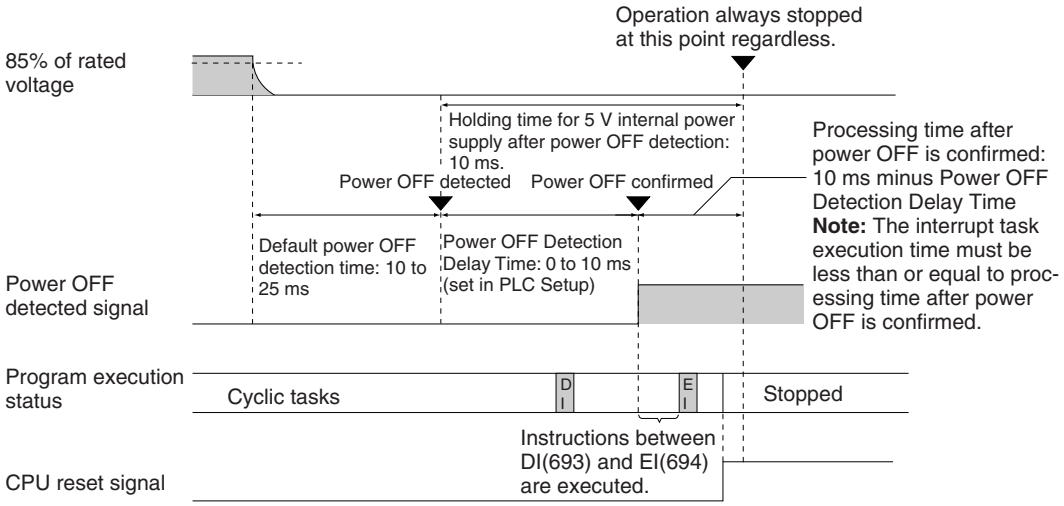
   Note A530 is normally cleared when power is turned OFF. To prevent this, the IOM Hold Bit (A50012) must be turned ON and the PLC Setup

must be set to maintain the setting of the IOM Hold Bit at Startup, or the following type of instruction must be included at the beginning of the program to set A530 to A5A5 hex.



Note If the power interruption becomes finalized during execution of DI(693), the instructions through EI(694) or END(001) will not be executed and the CPU Unit will be reset.

The following illustration is for a CS1D CPU Unit with A530 set to A5A5 hex to enable prohibiting power interrupt processing.



If A530 is not set to A5A5 hex, i.e., if prohibiting power interruption processing is not enabled, only the current instruction will be executed and then power interruption processing will be performed.

Power interruption processing is performed according to the contents of A530.

Duplex CPU Systems

A530 = A5A5 hex (disabling power interrupt processing)	A530 = Any value except A5A5 hex
All instructions between DI(693) and EI(694) are executed and the CPU Unit is reset.	Execution of the current instruction is completed and the CPU Unit is reset.

Single CPU Systems

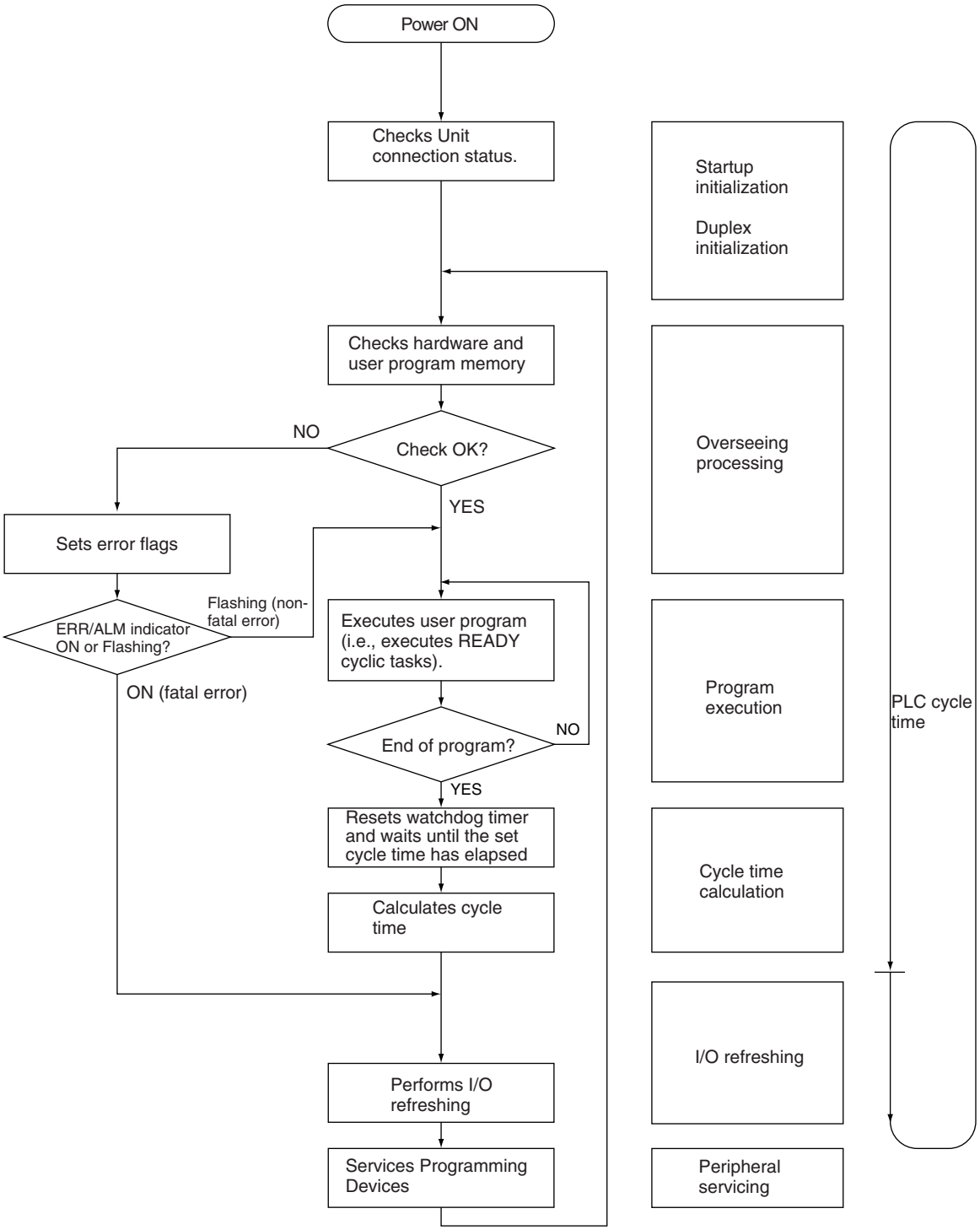
A530		A5A5 hex (disabling power interrupt processing)	Other
Power OFF Interrupt Task (PLC Setup)	Disabled	All instructions between DI(693) and EI(694) are executed and the CPU Unit is reset.	Execution of the current instruction is completed and the CPU Unit is reset.
	Enabled	Execution of the current instruction is completed, the Power OFF Interrupt Task is executed, and the CPU Unit is reset.	

9-4 Computing the Cycle Time

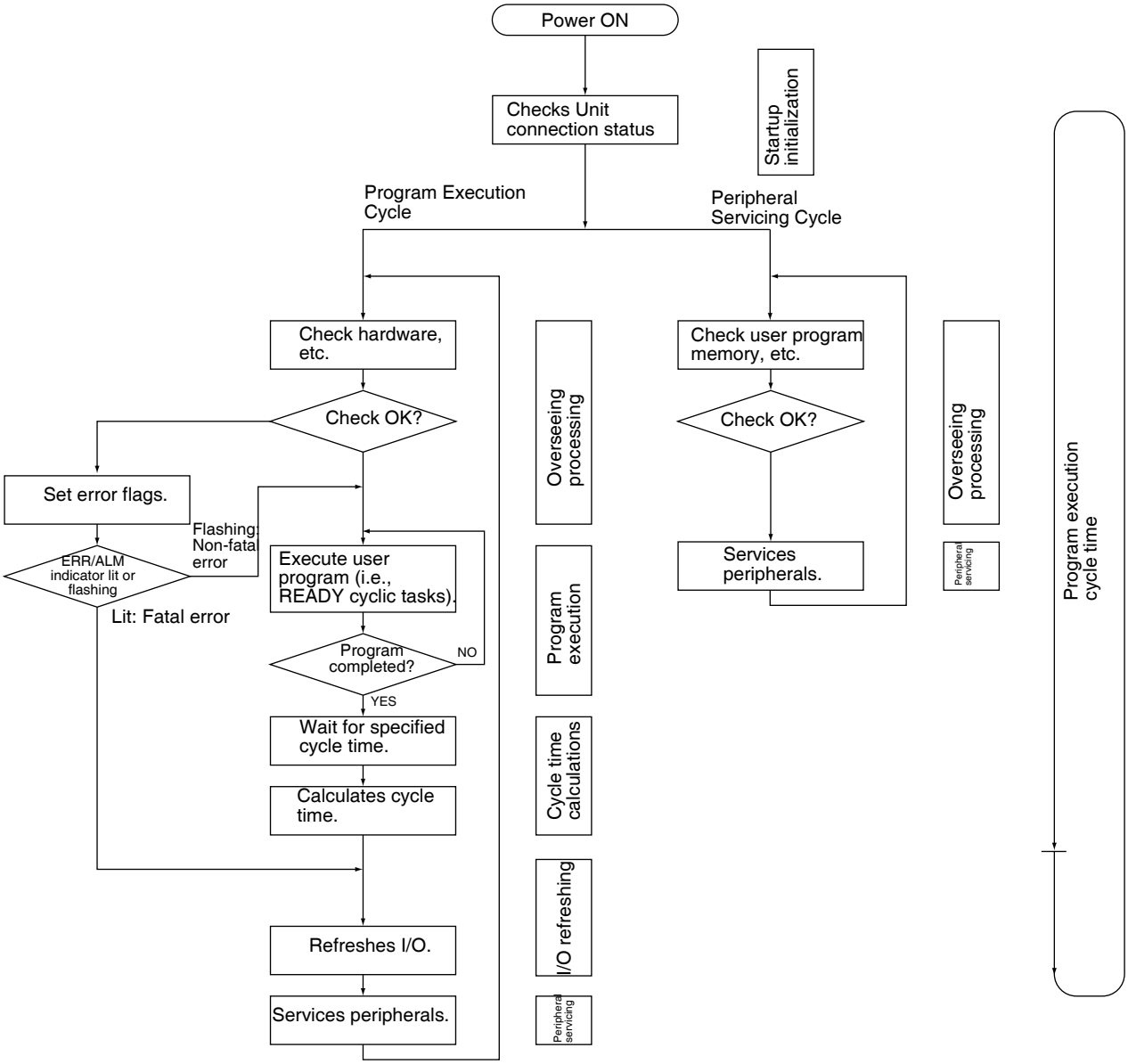
9-4-1 CPU Unit Operation Flowchart

The CS1D CPU Units process data in repeating cycles from the overseeing processing up to peripheral servicing as shown in the following diagram.

Normal Processing Mode



Parallel Processing Mode



9-4-2 Cycle Time Overview

Normal Processing Mode

The cycle time depends on the following conditions.

- Type and number of instructions in the user program (in all cyclic tasks that are executed during a cycle, including additional cyclic tasks).
- Type and number of Basic I/O Units
- Type and number of Special I/O Units, CPU Bus Units, Inner Boards, and type of services being executed.
- Specific servicing for the following Units/Boards
  - Data link refreshing and the number of data link words for Controller Link and SYSMAC LINK Units
  - Remote I/O for DeviceNet (Master) Units and the number of remote I/O words
  - Use of protocol macros and the largest communications message
  - Socket services for specific control bits for Ethernet Units and the number of send/receive words
- Fixed cycle time setting in the PLC Setup
- File access in file memory, and the amount of data transferred to/from file memory
- Event servicing for Special I/O Units, CPU Bus Units, Inner Boards, and communications ports
- Use of peripheral and RS-232C ports
- Fixed peripheral servicing time in the PLC Setup

Note

1. The cycle time is not affected by the number of tasks that are used in the user program. The tasks that affect the cycle time are those cyclic tasks that are READY in the cycle.
2. When the mode is switched from MONITOR mode to RUN mode, the cycle time will be extended by 10 ms (this will not, however, take the cycle time over its limit).

Cycle time = (1) + (2) + (3) + (4) + (5)

1: Overseeing

Details	Processing time and fluctuation cause
Checks the I/O bus and user program memory, checks for battery errors and refreshes the clock.	Duplex CPU Systems: 1.9 ms Single CPU Systems: 0.5 ms

2: Program Execution

Details	Processing time and fluctuation cause
Executes the user program, and calculates the total time taken for the instructions to execute the program.	Total instruction execution time

3: Cycle Time Calculation

Details	Processing time and fluctuation cause
Waits for the specified cycle time to elapse when a minimum (fixed) cycle time has been set in the PLC Setup. Calculates the cycle time.	When the cycle time is not fixed, the time for step 3 is approximately 0. When the cycle time is fixed, the time for step 3 is the preset fixed cycle time minus the actual cycle time ((1) + (2) + (4) + (5)).

4: I/O Refreshing

Details			Processing time and fluctuation cause
Basic I/O Units	Basic I/O Units are refreshed. Outputs from the CPU Unit to the I/O Unit are refreshed first for each Unit, and then inputs.		I/O refresh time for each Unit multiplied by the number of Units used
Special I/O Units	Words allocated in CIO Area		I/O refresh time for each Unit multiplied by the number of Units used
CPU Bus Units	Words allocated in CIO and DM Areas		I/O refresh time for each Unit multiplied by the number of Units used
	Unit-specific data	Data links for Controller Link and SYSMAC LINK Units, DeviceNet remote I/O for CS-series DeviceNet Units, send/receive data for protocol macros, and socket services for specific control bits for Ethernet Units	
Inner Boards (Single CPU Systems or Process-control CPU Units only)	Words allocated in Inner Board Area		Inner Board I/O refresh time
	Unit-specific data		

5: Peripheral Servicing

Details	Processing time and fluctuation cause
Services events for Special I/O Units. **Note** Peripheral servicing does not include I/O refreshing.	If a uniform peripheral servicing time hasn't been set in the PLC Setup for this servicing, 4% of the previous cycle's cycle time (calculated in step (3)) will be allowed for peripheral servicing. If a uniform peripheral servicing time has been set in the PLC Setup, servicing will be performed for the set time. At least 0.1 ms, however, will be serviced whether the peripheral servicing time is set or not. If no Units are mounted, the servicing time is 0 ms.
Services events for CPU Bus Units. **Note** Peripheral servicing does not include I/O refreshing.	
Services events for peripheral ports.	If a uniform peripheral servicing time hasn't been set in the PLC Setup for this servicing, 4% of the previous cycle's cycle time (calculated in step (3)) will be allowed for peripheral servicing. If a uniform peripheral servicing time has been set in the PLC Setup, servicing will be performed for the set time. At least 0.1 ms, however, will be serviced whether the peripheral servicing time is set or not. If the ports are not connected, the servicing time is 0 ms.
Services RS-232C ports.	

Details	Processing time and fluctuation cause
Services Inner Board events (Single CPU Systems or Process-control CPU Units only)	If a uniform peripheral servicing time hasn't been set in the PLC Setup for this servicing, 4% of the previous cycle's cycle time (calculated in step (3)) will be allowed for peripheral servicing. If a uniform peripheral servicing time has been set in the PLC Setup, servicing will be performed for the set time. At least 0.1 ms, however, will be serviced whether the peripheral servicing time is set or not. If no Inner Boards are mounted, the servicing time is 0 ms.
Services file access (Memory Card or EM file memory)	If a uniform peripheral servicing time hasn't been set in the PLC Setup for this servicing, 4% of the previous cycle's cycle time (calculated in step (3)) will be allowed for peripheral servicing. If a uniform peripheral servicing time has been set in the PLC Setup, servicing will be performed for the set time. At least 0.1 ms, however, will be serviced whether the peripheral servicing time is set or not. If there is no file access, the servicing time is 0 ms.
Services communications ports	If a uniform peripheral servicing time hasn't been set in the PLC Setup for this servicing, 4% of the previous cycle's cycle time (calculated in step (3)) will be allowed for peripheral servicing. If a uniform peripheral servicing time has been set in the PLC Setup, servicing will be performed for the set time. At least 0.1 ms, however, will be serviced whether the peripheral servicing time is set or not. If no communications ports are used, the servicing time is 0 ms.

Parallel Processing with Asynchronous Memory Access (Single CPU Systems Only)

Program Execution Cycle

The program execution cycle time depends on the following conditions.

- Type and number of instructions in the user program (in all cyclic tasks that are executed during a cycle, and within interrupt tasks for which the execution conditions have been satisfied).
- Type and number of Basic I/O Units
- Number of SYSMAC BUS Remote I/O Master Units and number of I/O points on the Slaves
- Type and number of Special I/O Units, CS-series CPU Bus Units, Inner Boards, and type of services being executed.
- Specific servicing for the following Units/Boards
  - Data link refreshing and the number of data link words for Controller Link and SYSMAC LINK Units
  - Remote I/O for DeviceNet (Master) Units and the number of remote I/O words
  - Use of protocol macros and the largest communications message

- Socket services for specific control bits for Ethernet Units and the number of send/receive words

- Fixed cycle time setting in the PLC Setup
- File access in file memory, and the amount of data transferred to/from file memory
- Fixed peripheral servicing time in the PLC Setup

The program execution cycle time is the total time required for the PLC to perform the 5 operations shown in the following tables.

Cycle time = (1) + (2) + (3) + (4) + (5)

Details			Processing time and fluctuation cause
(1)	Overseeing	I/O bus check, etc.	0.3 ms
(2)	Program execution	Same as for Normal Mode.	Same as for Normal Mode.
(3)	Cycle time calculation	Waits for the specified cycle time.	Same as for Normal Mode.
(4)	I/O refreshing	Same as for Normal Processing Mode.	Same as for Normal Processing Mode.
(5)	Partial peripheral servicing	Servicing file access	Same as for Normal Processing Mode.

Peripheral Servicing Cycle Time

The peripheral servicing execution cycle time depends on the following conditions.

- Type and number of Special I/O Units, CS-series CPU Bus Units, Inner Boards, and type of services being executed.
- Type and frequency of event servicing requiring communications ports.
- Use of peripheral and RS-232C ports

The peripheral servicing cycle time is the total time required for the PLC to perform the 5 operations shown in the following tables.

Cycle time = (1) + (2)

Name		Processing		Processing time and fluctuation cause
(1)	Overseeing processing	Checks user program memory, checks for battery errors, etc.		0.4 ms
(2)	Peripheral servicing	Performs services for the events give at the right, including I/O memory access.	Events with CS-series Special I/O Units (does not include I/O refreshing)	1.0 ms for each type of service If servicing ends before 1 ms has expired, the next type of servicing will be started immediately without waiting.
			Events with CS-series CPU Bus Units (does not include I/O refreshing)	
			Peripheral port events	
			RS-232C port events	
			Events with Inner Boards	
			Events using communications ports	

Note

1. The cycle time display on a Programming Device is the Program Execution Cycle Time.
2. The peripheral service cycle time varies with the event load and number of Units that are mounted. In a Parallel Processing Mode, however, this variation will not affect the program execution cycle time.

Parallel Processing with Synchronous Memory Access (Single CPU Systems Only)

Program Execution Cycle

The program execution cycle time depends on the same conditions as the Normal Mode. Partial peripheral servicing ((5) below), however, is restricted to servicing for file and I/O memory access.

The program execution cycle time is the total time required for the PLC to perform the 5 operations shown in the following tables.

Cycle time = (1) + (2) + (3) + (4) + (5)

Details				Processing time and fluctuation cause
(1)	Overseeing	I/O bus check, etc.		0.3 ms
(2)	Program execution	Same as for Normal Mode.		Same as for Normal Mode.
(3)	Cycle time calculation	Waits for the specified cycle time.		Same as for Normal Mode.
(4)	I/O refreshing	Same as for Normal Processing Mode.		Same as for Normal Mode.
(5)	Partial peripheral servicing	Servicing file access (Memory Card or EM file memory)		Same as for Normal Mode.
		Performs services for the events give at the right that requires I/O memory access	Events with CS-series Special I/O Units (does not include I/O refreshing)	
			Events with CS-series CPU Bus Units (does not include I/O refreshing)	
			Peripheral port events	
			RS-232C port events	
			Events with Inner Boards	
			Events using communications ports	

Peripheral Servicing Cycle Time

The peripheral servicing execution cycle time depends on the same conditions as the Parallel Processing with Asynchronous Memory Access. Peripheral servicing ((2) below), however, is restricted to servicing that does not access I/O memory.

The peripheral servicing cycle time is the total time required for the PLC to perform the 2 operations shown in the following tables.

Cycle time = (1) + (2)

Name		Processing		Processing time and fluctuation cause
(1)	Overseeing processing	Checks user program memory, checks for battery errors, etc.		0.4 ms
(2)	Peripheral servicing	Performs services for the events give at the right, excluding those that require I/O memory access.	Events with CS-series Special I/O Units (does not include I/O refreshing)	1.0 ms for each type of service If servicing ends before 1 ms has expired, the next type of servicing will be started immediately without waiting.
			Events with CS-series CPU Bus Units (does not include I/O refreshing)	
			Peripheral port events	
			RS-232C port events	
			Events with Inner Boards	
			Events using communications ports	

Note

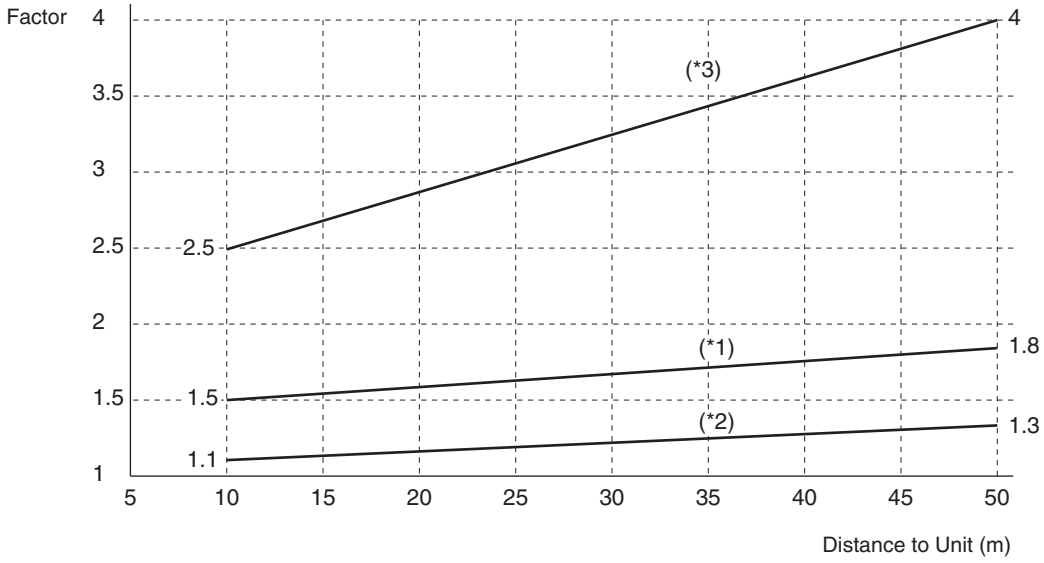
1. The cycle time display on a Programming Device is the Program Execution Cycle Time.
2. The peripheral service cycle time varies with the event load and number of Units that are mounted. In a Parallel Processing Mode, however, this variation will not affect the program execution cycle time.

9-4-3 I/O Unit Refresh Times for Individual Units and Boards

Basic I/O Unit Refresh

Unit	Name	Model	I/O refresh time per Unit
CS-series Basic I/O Units	16-point DC Input Unit	CS1W-ID211	0.004 ms (See note.)
	16-point AC Input Unit	CS1W-IA111/211	0.004 ms (See note.)
	8/16-point Relay Output Unit	CS1W-OC201/211	0.004 ms (See note.)
	8/16-point Triac Output Unit	CS1W-OA201/211	0.004 ms (See note.)
	16-point Transistor Output Unit, sinking outputs	CS1W-OD211	0.004 ms (See note.)
	16-point Transistor Output Unit, sourcing outputs	CS1W-OD212	0.004 ms (See note.)
	16-point Interrupt Input Unit	CS1W-INT01	0.004 ms (See note.)
	16-point High-speed Input Unit	CS1W-IDP01	0.004 ms (See note.)
	32-point DC Input Unit	CS1W-ID231	0.007 ms (See note.)
	64-point DC Input Unit	CS1W-ID261	0.014 ms (See note.)
	96-point DC Input Unit	CS1W-ID291	0.02 ms (See note.)
	32-point Transistor Output Unit, sinking outputs	CS1W-OD231	0.008 ms (See note.)
	32-point Transistor Output Unit, sourcing outputs	CS1W-OD232	0.008 ms (See note.)
	64-point Transistor Output Unit, sinking outputs	CS1W-OD261	0.016 ms (See note.)
	64-point Transistor Output Unit, sourcing outputs	CS1W-OD262	0.016 ms (See note.)
	96-point Transistor Output Unit, sinking outputs	CS1W-OD291	0.02 ms (See note.)
	96-point Transistor Output Unit, sourcing outputs	CS1W-OD292	0.02 ms (See note.)
	32-point DC Input/32-point Transistor Output Unit, sourcing outputs	CS1W-MD261	0.015 ms (See note.)
	32-point DC Input/32-point Transistor Output Unit, sinking outputs	CS1W-MD262	0.015 ms (See note.)
	48-point DC Input/48-point Transistor Output Unit, sinking outputs	CS1W-MD291	0.02 ms (See note.)
	48-point DC Input/48-point Transistor Output Unit, sourcing outputs	CS1W-MD292	0.02 ms (See note.)

Note Longer I/O refresh times will be required according to the distance from the CPU Rack to the Unit when these Units are mounted to Long-distance Expansion Racks. Multiply the values given in the table by the factors on line *1 in the following graph.



Unit	Name	Model	I/O refresh time per Unit	
			Normal	Mounted on Long-distance Expansion Rack (See note.)
CS-series Special I/O Units	Analog I/O Unit	CS1W-MAD44	0.12 ms	0.2 ms × *2
	Analog Input Unit	CS1W-AD041/081	0.12 ms	0.2 ms × *2
	Analog Output Unit	CS1W-DA041/08V/08C	0.12 ms	0.2 ms × *2
	Isolated Thermocouple Input Unit	CS1W-PTS01-V1	0.16 ms	0.3 ms × *2
	Isolated Resistance Thermometer Input Unit	CS1W-PTS02	0.16 ms	0.3 ms × *2
	Isolated Ni508Ω Resistance Thermometer Input Unit	CS1W-PTS03	0.16 ms	0.3 ms × *2
	Isolated 2-wire Transmission Device Input Unit	CS1W-PTW01	0.16 ms	0.3 ms × *2
	Isolated DC Input Unit	CS1W-PDC01	0.16 ms	0.3 ms × *2
	Isolated Control Output Unit (Analog Output Unit)	CS1W-PMV01	0.16 ms	0.3 ms × *2
	Power Transducer Input Unit	CS1W-PTR01	0.16 ms	0.3 ms × *2
	DC Input Unit (100 mV)	CS1W-PTR02	0.16 ms	0.3 ms × *2
	Isolated Pulse Input Unit	CS1W-PPS01	0.16 ms	0.3 ms × *2
	Position Control Unit	CS1W-NC113/133	0.29 ms × *2 (+ 0.7 ms for each instruction (IOWR/ IORD) used to transfer data)	
		CS1W-NC213/233	0.32 ms × *2 (+ 0.7 ms for each instruction (IOWR/ IORD) used to transfer data)	
		CS1W-NC413/433	0.41 ms × *2 (+ 0.6 ms for each instruction (IOWR/ IORD) used to transfer data)	
	High-speed Counter Unit	CS1W-CT021/041	0.14 ms	0.2 ms × *2
	Motion Control Unit	CS1W-MC221(-V1)	0.32 ms	0.8 ms × *2
		CS1W-MC421(-V1)	0.42 ms	0.85 ms × *2
	Customizable Counter Unit	CS1W-HIO01-V1	0.2 ms × *2 (+ 0.3 ms if DM Area or LR Area is used for data exchange with CPU Unit)	
		CS1W-HCP22-V1		
		CS1W-HCA22-V1		
	GPIB Interface Unit	CS1W-GPI01		

Note Longer increases in the cycle time will occur according to the distance from the CPU Rack to the Unit when these Units are mounted to Long-distance Expansion Racks. Multiply the values given in the table by the factors on line *2 in the graph on page 364 for the increases for data link words and send/receive words.

Increase in Cycle Time Caused by CPU Bus Units

Unit	Name	Model	Increase	Remarks
CPU Bus Units	Controller Link Unit	CS1W-CLK11 CS1W-CLK21-V1	0.1 ms With Long-distance Expansion Rack: 0.2 ms × factor *2	There will be an increase of 0.1 ms + 0.7 μs x number of data link words. (*3) With Long-distance Expansion Rack: (1.5 ms + (number of send words × 1 μs)) × factor *3 There will be an additional increase of the event execution times when message services are used.
		CS1W-CLK12/52-V1 CS1W-CLK13/53	0.1 ms With Long-distance Expansion Rack: 0.2 ms × factor *2	
	SYSMAC LINK	CS1W-SLK11/21	0.1 ms With Long-distance Expansion Rack: 0.2 ms × factor *2	
	Serial Communications Unit	CS1W-SCU21	0.22 ms With Long-distance Expansion Rack: 0.25 ms × factor *2	There will be an increase of up to the following time when a protocol macro is executed: 0.1 ms + 0.7 μs x maximum number of data words sent or received (0 to 500 words) With Long-distance Expansion Rack: (1.3 ms + (max. number of send/receive words × 1 μs)) × factor *3 There will be an increase of the event execution times when Host Links or 1:N NT Links are used.
	DeviceNet Unit	CS1W-DRM21-V1	0.4 ms + 0.7 μs for each allocated word With Long-distance Expansion Rack: (0.7 ms + (number of allocated words × 1 μs)) × factor *3	---
	Ethernet Unit	CS1W-ETN21 CS1D-ETN21D	0.1 ms With Long-distance Expansion Rack: 0.25 ms × factor *2	If socket services are executed with software switches, there will be an increase of 1.4 μs x the number of bytes sent/received. With Long-distance Expansion Rack: (number of send or receive bytes × 2 μs) × factor *3 There will be an increase of the event execution times when FINS communications services, socket services for CMND instructions, or FTP services are performed.

Note
1. Performance is given for the CS1D-CPU6□H/HA and CS1D-CPU6□S/SA.
2. Longer increases in the cycle time will occur according to the distance from the CPU Rack to the Unit when these Units are mounted to Long-distance Expansion Racks. Multiply the values given in the table by the factors on line *2 in the graph on page 364 for the increases and by the factors on line *3 for the additional increases for data link words and send/receive words.

Increase in Cycle Time Caused by Inner Board

Name	Model	Increase	Remarks
Serial Communications Board	CS1W-SCB21-V1/41-V1	0.22 ms	There will be an increase of up to the following time when a protocol macro is executed: 0.1 ms +maximum number of data words sent or received (0 to 500 words) x 0.7 μs There will be an increase of the event execution times when Host Links or 1:N NT Links are used.

9-4-4 Cycle Time Calculation Example

The following example shows the method used to calculate the cycle time when Basic I/O Units only are mounted to the PLC with a CS1D-CPU6□H.

Conditions

Item	Details	
CPU Rack (8 slots)	CS1W-ID291 96-point Input Units	4 Units
	CS1W-OD291 96-point Output Units	4 Units
Expansion Rack (8 slots) x 1 Unit	CS1W-ID291 96-point Input Units	4 Units
	CS1W-OD291 96-point Output Units	4 Units
User program	5 Ksteps	LD instruction 2.5 Ksteps, OUT instruction 2.5 Ksteps
Peripheral port connection	Yes and no	
Fixed cycle time processing	No	
RS-232C port connection	No	
Peripheral servicing with other devices (Special I/O Units, CS-series CPU Bus Units, Inner Boards, and file access)	No	

Calculation Example

Process name	Calculation	Processing time	
		With Programming Device	Without Programming Device
(1) Overseeing	---	1.9 ms	1.9 ms
(2) Program execution	0.04 μs × 2,500 + 0.04 μs × 2,500	0.2 ms	0.2 ms
(3) Cycle time calculation	(Fixed cycle time not set)	0 ms	0 ms
(4) I/O refreshing	0.02 ms × 8 + 0.02 ms × 8	0.32 ms	0.32 ms
(5) Peripheral servicing	(Peripheral port connected only)	0.1 ms	0 ms
Cycle time	(1) + (2) + (3) + (4) + (5)	2.52 ms	2.42 ms

9-4-5 Online Editing Cycle Time Extension

When online editing is executed from a Programming Device (such as Programming Console or CX-Programmer) while the CPU Unit is operating in MONITOR mode to change the program, the CPU Unit will momentarily suspend operation while the program is being changed. The period of time that the cycle time is extended is determined by the following conditions.

- Number of steps changed
- Editing operations (insert/delete/overwrite)
- Types of instructions used

The time increase for online editing is affected very little by the size of the largest program in the tasks.

If the maximum program size for each task is 64 Ksteps, the online editing cycle time extension will be as follows (See note.):

CPU Unit	Increase in cycle time for online editing
CS1D-CPU6□HA/H CPU Units for Duplex CPU Systems	Maximum: 55 ms, Normal: 8 ms
CS1D-CPU□□SA/6□S CPU Units for Single CPU Systems	Maximum: 55 ms, Normal: 8 ms
CS1D-CPU4□S CPU Units for Single CPU Systems	Maximum: 75 ms, Normal: 11 ms

When editing online, the cycle time will be extended by the time that operation is stopped.

Note

1. When there is one task, online editing is processed all in the cycle time following the cycle in which online editing is executed (written). When there are multiple tasks (cyclic tasks), online editing is separated, so that for n tasks, processing is executed over n to n ×2 cycles max.
2. The above cycle time extensions assume that a lot of instructions requiring time are being used in the program. The cycle time extension would be as follows for most programs:
   CS1D CPU Units: 12 ms max.

9-4-6 Affects of Duplex and Simplex Operation on the Cycle Time (Duplex CPU Systems Only)

If operation switches from Duplex Mode to Simplex Mode, processing to synchronize the active and standby CPU Units will no longer be performed, resulting in a shorter cycle time. The more instructions requiring synchronization (such as IORF, DLNK, IORD, IOWR, PID, RXD, FREAD, FWRIT, and TWRIT) are used, the greater the difference between Duplex Mode and Simplex Mode operation will be (with Duplex Mode having the longer cycle time). Confirm that the system will operate correctly and safely even for the cycle time in both Simplex and Duplex Modes.

9-4-7 Duplex Processing Cycle Time Extension (Duplex CPU Systems Only)

The cycle time for a Duplex CPU System can be extended at various times as described below. Enter actual system operation only after verifying that the system operates correctly for the maximum possible cycle time.

Cycle Time Extension for Duplex Initialization

The cycle time will be increased over the normal cycle time whenever duplex operation is initialized, including when power is turned ON, when the initialization button is pressed, when operation is started, and when data is transferred. The maximum increases are listed in the following table. The maximum cycle time would thus be the normal cycle time plus the increase in the cycle time for duplex initialization shown in the following table.

CPU Unit model	Increase in cycle time
CS1D-CPU65H	190 ms +A
CS1D-CPU67HA/H	520 ms +A
CS1D-CPU68HA	900 ms +A

A is the time added when duplex Inner Boards are mounted. Refer to the Inner Board Operation Manual for the value of A.

Example: The maximum cycle times would be as shown in the following table if the normal cycle time was 20 ms.

CPU Unit model	Maximum cycle time
CS1D-CPU65H	20 ms + 190 ms = 210 ms
CS1D-CPU67HA/H	20 ms + 520 ms = 540 ms
CS1D-CPU68HA	20 ms + 900 ms = 920 ms

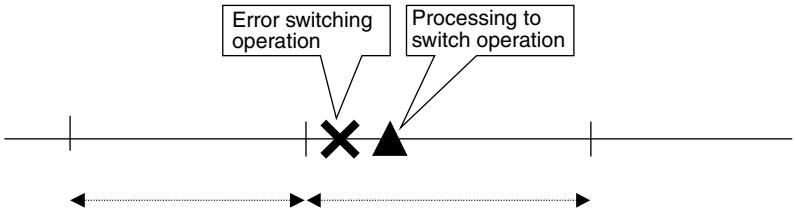
Set the monitoring time (10 to 40,000 ms, default: 1 s) +B (*1) +C (*2) for the cycle time high enough to allow for this increase. Also, confirm that the system will operate correctly and safely even for the maximum cycle time, including the increase for duplex initialization.

*1: B is the time added to the cycle-time monitoring time only for duplex initialization when duplex Inner Boards are mounted. Refer to the Inner Board Operation Manual for the value of B.

*2: When using the CS1D-CPU68HA, C is the time added to the cycle time monitoring time only during duplex initialization, and is 800 ms.

Cycle Time Extension when Switching to Standby CPU Unit

The cycle time will be extended if an error occurs in the active CPU Unit that causes operation to be switched to the standby CPU Unit.



There are two factors involved in the cycle time extension:

- Time required to detect the error causing operation to switch
- Time required to actually switch operation to the standby CPU Unit.

The following table list the time by which the cycle time will be extended depending on the error that caused operation to be switched.

Error switching operation	Cycle time extension	Remarks
Switch with CPU Unit switch setting	11.5 ms	Time required to detect switch setting: 11 ms Operation switching time: 0.5 ms
CPU error (WDT error)	125.5 ms	Time required to detect microcomputer WDT error in the CS1D: 125 ms Operation switching time: 0.5 ms
FALS error (when executed in only active CPU Unit)	0.5 ms	FALS errors are detected when the FALS instruction is executed, so no time is required to detect the error. Only the operation switching time (0.5 ms) is required.
Maximum cycle time exceeded	Maximum cycle time + 0.5 ms	Time required by the CS1D to detect the long cycle time (depends on the setting of the maximum cycle time) plus the operation switching time (0.5 ms).
Program error	0.5 ms	Program error detection is performed constantly, so no time is required to detect the error. Only the operation switching time (0.5 ms) is required.
Inner Board error (Process-control CPU Units only)	0.5 ms	Inner Board error detection is performed constantly, so no time is required to detect the error. Only the operation switching time (0.5 ms) is required.
Memory error	0.5 ms	Memory error detection is performed constantly, so no time is required to detect the error. Only the operation switching time (0.5 ms) is required.

9-4-8 I/O Response Time

The I/O response time is the time it takes from when an Input Unit's input turns ON, the data is recognized by the CPU Unit, and the user program is executed, up to the time for the result to be output to an Output Unit's output terminals.

The length of the I/O response time depends on the following conditions.

- Timing of Input Bit turning ON.
- Cycle time.
- Type of Rack to which Input and Output Units are mounted (CPU Rack or Expansion Rack).

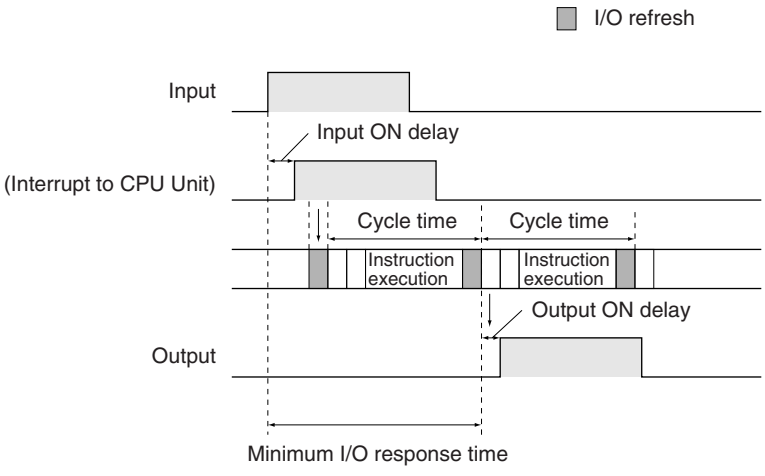
Basic I/O Units

Minimum I/O Response Time

The I/O response time is shortest when data is retrieved immediately before I/O refresh of the CPU Unit.

The minimum I/O response time is the total of the Input ON delay, the cycle time, and the Output ON delay.

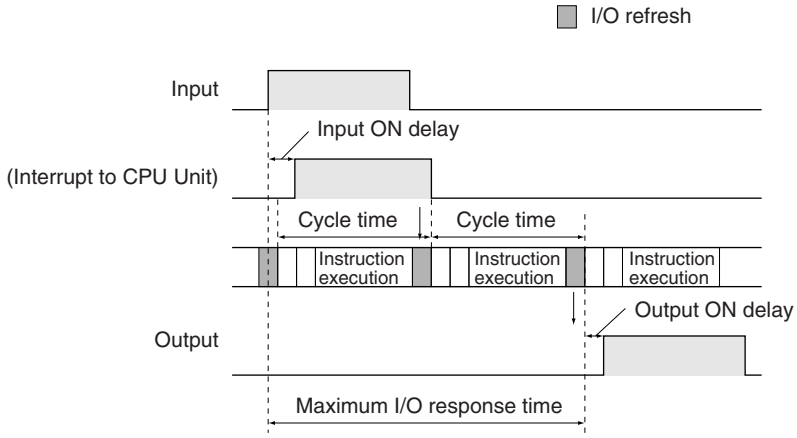
Note The Input and Output ON delay differs according to the Unit used.



Maximum I/O Response Time

The I/O response time is longest when data is retrieved immediately after I/O refresh of the Input Unit.

The maximum I/O response time is the total of the Input ON delay, (the cycle time × 2), and the Output ON delay.



Calculation Example

Conditions:

Input ON delay	1.5 ms
Output ON delay	0.2 ms
Cycle time	20.0 ms

Minimum I/O response time = 1.5 ms + 20 ms + 0.2 ms = 21.7 ms

Maximum I/O response time = 1.5 ms + (20 ms ×2) + 0.2 ms = 41.7 ms

9-4-9 Interrupt Response Times (Single CPU Systems Only)

I/O Interrupt Tasks

The interrupt response time for I/O interrupt tasks is the time taken from when an input from a CS1W-INT01 Interrupt Input Unit has turned ON (or OFF) until the I/O interrupt task has actually been executed.

The length of the interrupt response time for I/O interrupt tasks depends on the following conditions.

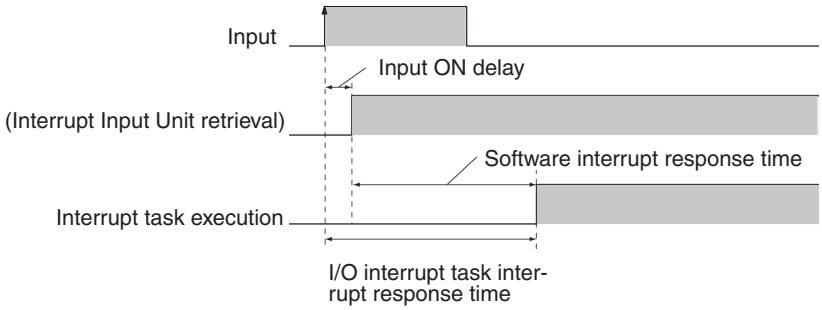
Item	Time
Hardware response	Upward differentiation: 0.1 ms, Downward differentiation: 0.5 ms
Software interrupt response	137 μs

Note

1. The software interrupt response time will be 1 ms if there is a C200H Special I/O Unit in the PLC.
2. I/O interrupt tasks can be executed (while an instruction is being executed, or by stopping the execution of an instruction) during execution of the user program, I/O refresh, peripheral servicing, or overseeing. The interrupt response time is not affected by the Input of the Interrupt Input Unit turning ON during any of the above processing operations.

   Some I/O interrupts, however, are not executed during interrupt tasks even if the I/O interrupt conditions are satisfied. Instead, the I/O interrupts are executed in order of priority after the other interrupt task has completed execution and the software interrupt response time (1 ms max.) has elapsed.

The interrupt response time of I/O interrupt tasks is the sum of the Input ON delay (0.2 ms max.) and the software interrupt response time (1 ms max.).



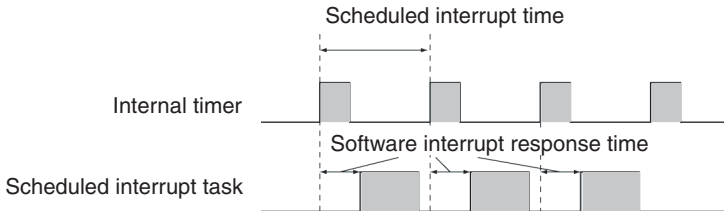
Scheduled Interrupt Tasks

The interrupt response time of scheduled interrupt tasks is the time taken from after the scheduled time specified by the MSKS(690) instruction has elapsed until the interrupt task has actually been executed.

The length of the interrupt response time for scheduled interrupt tasks is 1 ms max.

Note Scheduled interrupt tasks can be executed (while an instruction is being executed, or by stopping the execution of an instruction) during execution of the user program, I/O refresh, peripheral servicing, or overseeing. The interrupt response time is not affected by the scheduled time elapsing during any of the above processing operations.

Some scheduled interrupts, however, are not executed during other interrupt tasks even if the scheduled interrupt conditions are satisfied. Instead, the scheduled interrupts are executed in order of priority after the other interrupt task has completed execution and the software interrupt response time (1 ms max.) has elapsed.



External Interrupt Tasks

The interrupt response time for external interrupt tasks differs depending on the Unit or Board (Special I/O Unit, CS-series CPU Bus Unit, or Inner Board) that is requesting the external interrupt task of the CPU Unit and the type of service requested by the interrupt. For details, refer to the appropriate operation manual for the Unit or Board being used.

Power OFF Interrupt Tasks

Power OFF interrupt tasks are executed within 0.1 ms of the power being confirmed as OFF.

9-5 Instruction Execution Times and Number of Steps

The following table lists the execution times for all instructions that are available for CS1D CPU Units.

The total execution time of instructions within one whole user program (i.e., within all the tasks that are executed in a cycle) is the process time for program execution when calculating the cycle time (See note.).

The conditions (e.g., operands) under which an instruction is executed affect the execution time, as does the model of the CPU Unit. The execution time can also vary when the execution condition is OFF.

The following table also lists the length of each instruction in the *Length (steps)* column. The number of steps required in the user program area for each of the instructions varies from 1 to 7 steps, depending upon the instruction and the operands used with it. The number of steps in a program is not the same as the number of instructions.

Note 1. Program capacity for CS-series PLCs is measured in steps, whereas program capacity for previous OMRON PLCs, such as the C-series and CV-series PLCs, was measured in words. Basically speaking, 1 step is equivalent to 1 word. The amount of memory required for each instruction, however, is different for some of the CS-series instructions, and inaccuracies will occur if the capacity of a user program for another PLC is converted for a CS-series PLC based on the assumption that 1 word is 1 step. Refer to the information at the end of *9-5 Instruction Execution Times and Number of Steps* for guidelines on converting program capacities from previous OMRON PLCs.

Most instructions are supported in differentiated form (indicated with ↑, ↓, @, and %). Specifying differentiation will increase the execution times by the following amounts.

Symbol	CS1D CPU Unit	
	CPU□□HA/H/SA/ CPU6□S (μs)	CPU4□S (μs)
↑ or ↓	+0.24	+0.32
@ or %	+0.24	+0.32

2. When the execution condition for an instruction is OFF, the execution time is given in the following table.

CS1D CPU Unit	
CPU□□HA/H/SA /CPU6□S (μs)	CPU4□S (μs)
Approx. 0.1	Approx. 0.2

9-5-1 Sequence Input Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
LOAD	LD	---	1	0.02	0.02	0.02	0.02	0.04	---
	!LD	---	2	--- (See note 2.)	--- (See note 2.)	12.24	+21.14	+21.16	---
LOAD NOT	LD NOT	---	1	0.02	0.02	0.02	0.02	0.04	---
	!LD NOT	---	2	--- (See note 2.)	--- (See note 2.)	12.24	+21.14	+21.16	---
AND	AND	---	1	0.02	0.02	0.02	0.02	0.04	---
	!AND	---	2	--- (See note 2.)	--- (See note 2.)	12.24	+21.14	+21.16	---
AND NOT	AND NOT	---	1	0.02	0.02	0.02	0.02	0.04	---
	!AND NOT	---	2	--- (See note 2.)	--- (See note 2.)	12.24	+21.14	+21.16	---
OR	OR	---	1	0.02	0.02	0.02	0.02	0.04	---
	!OR	---	2	--- (See note 2.)	--- (See note 2.)	12.24	+21.14	+21.16	---
OR NOT	OR NOT	---	1	0.02	0.02	0.02	0.02	0.04	---
	!OR NOT	---	2	--- (See note 2.)	--- (See note 2.)	12.24	+21.14	+21.16	---
AND LOAD	AND LD	---	1	0.02	0.02	0.02	0.02	0.04	---
OR LOAD	OR LD	---	1	0.02	0.02	0.02	0.02	0.04	---
NOT	NOT	520	1	0.02	0.02	0.02	0.02	0.04	---
CONDITION ON	UP	521	3	0.40	0.30	0.30	0.30	0.42	---
CONDITION OFF	DOWN	522	4	0.40	0.30	0.30	0.30	0.42	---
LOAD BIT TEST	LD TST	350	4	0.14	0.14	0.14	0.14	0.24	---
LOAD BIT TEST NOT	LDTSTN	351	4	0.14	0.14	0.14	0.14	0.24	---
AND BIT TEST NOT	AND TSTN	351	4	0.14	0.14	0.14	0.14	0.24	---
OR BIT TEST	OR TST	350	4	0.14	0.14	0.14	0.14	0.24	---
OR BIT TEST NOT	OR TSTN	351	4	0.14	0.14	0.14	0.14	0.24	---

Note
1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.
2. Not supported by Duplex CPU Systems.

9-5-2 Sequence Output Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
OUTPUT	OUT	---	1	0.02	0.02	0.02	0.02	0.04	---
	!OUT	---	2	--- (See note 2.)	--- (See note 2.)	12.37	+21.37	+21.37	---
OUTPUT NOT	OUT NOT	---	1	0.02	0.02	0.02	0.02	0.04	---
	!OUT NOT	---	2	--- (See note 2.)	--- (See note 2.)	12.37	+21.37	+21.37	---
KEEP	KEEP	011	1	0.06	0.06	0.06	0.06	0.08	---
DIFFEREN-TIATE UP	DIFU	013	2	0.32	0.24	0.24	0.24	0.40	---
DIFFEREN-TIATE DOWN	DIFD	014	2	0.32	0.24	0.24	0.24	0.40	---
SET	SET	---	1	0.02	0.02	0.02	0.02	0.06	---
	!SET	---	2	--- (See note 2.)	--- (See note 2.)	12.37	+21.37	+21.37	---
RESET	RSET	---	1	0.02	0.02	0.02	0.02	0.06	Word specified
	!RSET	---	2	--- (See note 2.)	--- (See note 2.)	12.37	+21.37	+21.37	---
MULTIPLE BIT SET	SETA	530	4	5.5	5.8	5.5	5.8	6.1	With 1-bit set
				25.2	25.7	25.2	25.7	27.2	With 1,000-bit set
MULTIPLE BIT RESET	RSTA	531	4	5.5	5.7	5.5	5.8	6.1	With 1-bit reset
				25.2	25.8	25.2	25.8	27.2	With 1,000-bit reset
SINGLE BIT SET	SETB	532	2	0.24	0.24	0.24	0.24	0.34	---
	!SETB	532	3	--- (See note 2.)	--- (See note 2.)	12.37	+21.44	+21.54	---
SINGLE BIT RESET	RSTB	534	2	0.24	0.24	0.24	0.24	0.34	---
	!RSTB	534	3	--- (See note 2.)	--- (See note 2.)	12.37	+21.44	+21.54	---
SINGLE BIT OUTPUT	OUTB	534	2	0.22	0.22	0.22	0.22	0.32	---
	!OUTB	534	3	--- (See note 2.)	--- (See note 2.)	12.37	+21.42	+21.52	---

Note
1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.
2. Not supported by Duplex CPU Systems.

9-5-3 Sequence Control Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
END	END	001	1	4.3	5.5	4.3	5.5	6.0	---
NO OPERATION	NOP	000	1	0.02	0.02	0.02	0.02	0.04	---
INTERLOCK	IL	002	1	0.06	0.06	0.06	0.06	0.06	---
INTERLOCK CLEAR	ILC	003	1	0.06	0.06	0.06	0.06	0.06	---
MULTI-INTERLOCK DIFFERENTIATION HOLD	MILH	517	3	--- (See note 2.)	--- (See note 2.)	4.0	6.1	6.5	During interlock
						5.1	7.5	7.9	Not during interlock and interlock not set
						6.4	8.9	9.7	Not during interlock and interlock set
MULTI-INTERLOCK DIFFERENTIATION RELEASE	MILR	518	3	--- (See note 2.)	--- (See note 2.)	3.9	6.1	6.5	During interlock
						5.1	7.5	7.9	Not during interlock and interlock not set
						6.4	8.9	9.7	Not during interlock and interlock set
MULTI-INTERLOCK CLEAR	MILC	519	2	--- (See note 2.)	--- (See note 2.)	2.8	5.0	5.6	Interlock not cleared
						3.7	5.7	6.2	Interlock cleared
JUMP	JMP	004	2	0.47	0.38	0.38	0.38	0.48	---
JUMP END	JME	005	2	---	---	---	---	---	---
CONDITIONAL JUMP	CJP	510	2	0.47	0.38	0.38	0.38	0.48	When JMP condition is satisfied
CONDITIONAL JUMP NOT	CJPN	511	2	0.47	0.38	0.38	0.38	0.48	When JMP condition is satisfied
MULTIPLE JUMP	JMP0	515	1	0.06	0.06	0.06	0.06	0.06	---
MULTIPLE JUMP END	JME0	516	1	0.06	0.06	0.06	0.06	0.06	---
FOR LOOP	FOR	512	2	0.12	0.12	0.12	0.12	0.21	Designating a constant
BREAK LOOP	BREAK	514	1	0.12	0.12	0.12	0.12	0.12	---
NEXT LOOP	NEXT	513	1	0.17	0.17	0.17	0.17	0.17	When loop is continued
				0.12	0.12	0.12	0.12	0.12	When loop is ended

Note
1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.
2. Not supported by Duplex CPU Systems.

9-5-4 Timer and Counter Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
TIMER	TIM	---	3	0.72	0.56	0.56	0.56	0.88	---
	TIMX	550	3	0.72	0.56	0.56	0.56	0.88	---
COUNTER	CNT	---	3	0.72	0.56	0.56	0.56	0.88	---
	CNTX	546	3	0.72	0.56	0.56	0.56	0.88	---
HIGH-SPEED TIMER	TIMH	015	3	0.72	0.88	0.60	0.88	1.14	---
	TIMHX	551	3	0.72	0.88	0.60	0.88	1.14	---
ONE-MS TIMER	TMHH	540	3	12.9	12.5	0.86	0.86	1.12	---
	TMHHX	552	3	12.9	12.5	0.86	0.86	1.12	---
ACCUMU-LATIVE TIMER	TTIM	087	3	13.9	16.1	13.2	16.1	17.0	---
				9.8	10.9	9.4	10.9	11.4	When resetting
				7.4	8.5	7.3	8.5	8.7	When interlock-ing
	TTIMX	555	3	13.9	16.1	13.2	16.1	17.0	---
				9.8	10.9	9.4	10.9	11.4	When resetting
				7.4	8.5	7.3	8.5	8.7	When interlock-ing
LONG TIMER	TIML	542	4	7.4	7.6	7.3	7.6	10.0	---
				6.0	6.2	6.0	6.2	6.5	When interlock-ing
	TIMLX	553	4	7.4	7.6	7.3	7.6	10.0	---
				6.0	6.2	6.0	6.2	6.5	When interlock-ing
MULTI-OUT-PUT TIMER	MTIM	543	4	18.0	20.9	16.2	20.9	23.3	---
				5.6	5.6	5.6	5.6	5.8	When resetting
	MTIMX	554	4	18.0	20.9	16.2	20.9	23.3	---
				5.6	5.6	5.6	5.6	5.8	When resetting
REVERS-IBLE COUNTER	CNTR	012	3	13.6	16.9	13.6	16.9	19.0	---
	CNTRX	548	3	13.6	16.9	13.6	16.9	19.0	---
RESET TIMER/ COUNTER	CNR	545	3	9.4	9.9	8.8	9.9	10.6	When resetting 1 word
				3.92 ms	4.16 ms	3.06 ms	4.16 ms	4.16 ms	When resetting 1,000 words
	CNRX	547	3	9.4	9.9	8.8	9.9	10.6	When resetting 1 word
				3.92 ms	4.16 ms	3.06 ms	4.16 ms	4.16 ms	When resetting 1,000 words

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-5 Comparison Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
Input Comparison Instructions (unsigned)	LD, AND, OR+=	300	4	0.10	0.10	0.10	0.10	0.16	---
	LD, AND, OR+<>	305							
	LD, AND, OR+<	310							
	LD, AND, OR+<=	315							
	LD, AND, OR+>	320							
	LD, AND, OR+>=	325							
Input Comparison Instructions (double, unsigned)	LD, AND, OR+=+L	301	4	0.14	0.10	0.14	0.10	0.16	---
	LD, AND, OR+<>+L	306							
	LD, AND, OR+<+L	311							
	LD, AND, OR+<=+L	316							
	LD, AND, OR+>+L	321							
	LD, AND, OR+>=+L	326							
Input Comparison Instructions (signed)	LD, AND, OR+=+S	302	4	0.10	0.10	0.10	0.10	0.16	---
	LD, AND, OR+<>+S	307							
	LD, AND, OR+<+S	312							
	LD, AND, OR+<=S	317							
	LD, AND, OR+>+S	322							
	LD, AND, OR+>=+S	327							
Input Comparison Instructions (double, signed)	LD, AND, OR+=+SL	303	4	0.14	0.10	0.14	0.10	0.16	---
	LD, AND, OR+<>+SL	308							
	LD, AND, OR+<+SL	313							
	LD, AND, OR+<=+SL	318							
	LD, AND, OR+>+SL	323							
	LD, AND, OR+>=+SL	328							

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
Time Comparison Instructions	LD, AND, OR+=DT	341	4	--- (See note 2.)	--- (See note 2.)	23.0	25.1	36.4	---
	LD, AND, OR+<>DT	342				23.0	25.2		
	LD, AND, OR+<DT	343				23.0	25.2		
	LD, AND, OR+<=DT	344				23.1	25.2		
	LD, AND, OR+>DT	345				23.1	25.1		
	LD, AND, OR+>=DT	346				23.0	25.2		
COMPARE	CMP	020	3	0.04	0.04	0.04	0.04	0.04	---
	!CMP	020	7	--- (See note 2.)	--- (See note 2.)	22.9	+42.1	+42.1	---
DOUBLE COMPARE	CMPL	060	3	0.08	0.08	0.08	0.08	0.08	---
SIGNED BINARY COMPARE	CPS	114	3	0.08	0.08	0.08	0.08	0.08	---
	!CPS	114	7	--- (See note 2.)	--- (See note 2.)	22.9	+35.9	+35.9	---
DOUBLE SIGNED BINARY COMPARE	CPSL	115	3	0.08	0.08	0.08	0.08	0.08	---
TABLE COMPARE	TCMP	085	4	14.2	14.0	13.6	14.0	15.2	---
MULTIPLE COMPARE	MCMP	019	4	20.2	20.5	19.1	20.5	22.8	---
UNSIGNED BLOCK COMPARE	BCMP	068	4	22.0	21.5	20.6	21.5	23.7	---
EXPANDED BLOCK COMPARE	BCMP2	502	4	--- (See note 2.)	--- (See note 2.)	8.0	8.4	9.3	Number of data words: 1
						297.1	313.0	345.3	Number of data words: 255
AREA RANGE COMPARE	ZCP	088	3	5.4	5.3	5.3	5.3	5.4	---
DOUBLE AREA RANGE COMPARE	ZCPL	116	3	5.7	5.5	5.5	5.5	6.7	---

Note 1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.

2. Not supported by Duplex CPU Systems.

9-5-6 Data Movement Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
MOVE	MOV	021	3	0.20	0.18	0.18	0.18	0.20	---
	!MOV	021	7	--- (See note 2.)	--- (See note 2.)	17.8	+21.38	+21.40	---
DOUBLE MOVE	MOVL	498	3	0.35	0.32	0.32	0.32	0.34	---
MOVE NOT	MVN	022	3	0.20	0.18	0.18	0.18	0.20	---
DOUBLE MOVE NOT	MVNL	499	3	0.35	0.32	0.32	0.32	0.34	---
MOVE BIT	MOVB	082	4	0.26	0.24	0.24	0.24	0.34	---
MOVE DIGIT	MOVD	083	4	0.26	0.24	0.24	0.24	0.34	---
MULTIPLE BIT TRANSFER	XFRB	062	4	10.8	10.1	10.2	10.1	10.8	Transferring 1 bit
				164.4	186.4	162.6	186.4	189.8	Transferring 255 bits
BLOCK TRANSFER	XFER	070	4	0.47	0.36	0.36	0.36	0.44	Transferring 1 word
				360.2	300.1	300.1	300.1	380.1	Transferring 1,000 words
BLOCK SET	BSET	071	4	0.29	0.26	0.26	0.26	0.28	Setting 1 word
				220.1	200.1	200.1	200.1	220.1	Setting 1,000 words
DATA EXCHANGE	XCHG	073	3	0.46	0.40	0.40	0.40	0.56	---
DOUBLE DATA EXCHANGE	XCGL	562	3	0.86	0.76	0.76	0.76	1.04	---
SINGLE WORD DISTRIBUTE	DIST	080	4	5.1	5.1	5.1	5.1	5.4	---
DATA COLLECT	COLL	081	4	5.4	5.1	5.3	5.1	5.3	---
MOVE TO REGISTER	MOVR	560	3	0.08	0.08	0.08	0.08	0.08	---
MOVE TIMER/ COUNTER PV TO REGISTER	MOVRW	561	3	0.08	0.42	0.08	0.42	0.50	---

Note
1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.
2. Not supported by Duplex CPU Systems.

9-5-7 Data Shift Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
SHIFT REGISTER	SFT	010	3	5.4	7.4	5.4	7.4	10.4	Shifting 1 word
				369.0	433.2	369.0	433.2	488.0	Shifting 1,000 words

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
REVERSIBLE SHIFT REGISTER	SFTR	084	4	4.3	6.9	4.3	6.9	7.2	Shifting 1 word
				481.6	615.3	481.6	615.3	680.2	Shifting 1,000 words
ASYNCHRONOUS SHIFT REGISTER	ASFT	017	4	5.4	6.2	5.4	6.2	6.4	Shifting 1 word
				1131.7	1.22 ms	1131.7	1.22 ms	1.22 ms	Shifting 1,000 words
WORD SHIFT	WSFT	016	4	5.4	4.5	5.4	4.5	4.7	Shifting 1 word
				183.5	171.5	183.5	171.5	171.7	Shifting 1,000 words
ARITHMETIC SHIFT LEFT	ASL	025	2	0.22	0.22	0.22	0.22	0.32	---
DOUBLE SHIFT LEFT	ASLL	570	2	0.40	0.40	0.40	0.40	0.56	---
ARITHMETIC SHIFT RIGHT	ASR	026	2	0.22	0.22	0.22	0.22	0.32	---
DOUBLE SHIFT RIGHT	ASRL	571	2	0.40	0.40	0.40	0.40	0.56	---
ROTATE LEFT	ROL	027	2	0.22	0.22	0.22	0.22	0.32	---
DOUBLE ROTATE LEFT	ROLL	572	2	0.40	0.40	0.40	0.40	0.56	---
ROTATE LEFT WITHOUT CARRY	RLNC	574	2	0.22	0.22	0.22	0.22	0.32	---
DOUBLE ROTATE LEFT WITHOUT CARRY	RLNL	576	2	0.40	0.40	0.40	0.40	0.56	---
ROTATE RIGHT	ROR	028	2	0.22	0.22	0.22	0.22	0.32	---
DOUBLE ROTATE RIGHT	RORL	573	2	0.40	0.40	0.40	0.40	0.56	---
ROTATE RIGHT WITHOUT CARRY	RRNC	575	2	0.22	0.22	0.22	0.22	0.32	---
DOUBLE ROTATE RIGHT WITHOUT CARRY	RRNL	577	2	0.40	0.40	0.40	0.40	0.56	---
ONE DIGIT SHIFT LEFT	SLD	074	3	3.8	5.9	3.1	5.9	6.1	Shifting 1 word
				587.5	561.1	560.1	561.1	626.3	Shifting 1,000 words
ONE DIGIT SHIFT RIGHT	SRD	075	3	4.9	6.9	4.9	6.9	7.1	Shifting 1 word
				816.1	760.5	737.8	760.5	895.5	Shifting 1,000 words

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
SHIFT N-BIT DATA LEFT	NSFL	578	4	4.3	7.5	4.3	7.5	8.3	Shifting 1 bit
				37.5	40.3	37.5	40.3	45.4	Shifting 1,000 bits
SHIFT N-BIT DATA RIGHT	NSFR	579	4	4.9	7.5	4.9	7.5	8.3	Shifting 1 bit
				74.2	50.5	45.6	50.5	55.3	Shifting 1,000 bits
SHIFT N-BITS LEFT	NASL	580	3	0.19	0.22	0.19	0.22	0.32	---
DOUBLE SHIFT N-BITS LEFT	NSLL	582	3	0.37	0.40	0.37	0.40	0.56	---
SHIFT N-BITS RIGHT	NASR	581	3	0.20	0.22	0.20	0.22	0.32	---
DOUBLE SHIFT N-BITS RIGHT	NSRL	583	3	0.38	0.40	0.38	0.40	0.56	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-8 Increment/Decrement Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
INCREMENT BINARY	++	590	2	0.25	0.22	0.22	0.22	0.32	---
OUBLE INCREMENT BINARY	++L	591	2	0.44	0.40	0.40	0.40	0.56	---
DECREMENT BINARY	––	592	2	0.25	0.22	0.22	0.22	0.32	---
DOUBLE DECREMENT BINARY	––L	593	2	0.44	0.40	0.40	0.40	0.56	---
INCREMENT BCD	++B	594	2	6.5	6.4	6.5	6.4	4.5	---
DOUBLE INCREMENT BCD	++BL	595	2	5.3	5.6	5.2	5.6	4.9	---
DECREMENT BCD	––B	596	2	6.5	6.3	6.5	6.3	4.6	---
DOUBLE DECREMENT BCD	––BL	597	2	5.5	5.3	5.4	5.3	4.7	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-9 Symbol Math Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
SIGNED BINARY ADD WITHOUT CARRY	+	400	4	0.20	0.18	0.18	0.18	0.20	---
DOUBLE SIGNED BINARY ADD WITHOUT CARRY	+L	401	4	0.36	0.32	0.32	0.32	0.34	---
SIGNED BINARY ADD WITH CARRY	+C	402	4	0.20	0.18	0.18	0.18	0.20	---
DOUBLE SIGNED BINARY ADD WITH CARRY	+CL	403	4	0.36	0.32	0.32	0.32	0.34	---
BCD ADD WITHOUT CARRY	+B	404	4	8.0	8.2	8.0	8.2	8.4	---
DOUBLE BCD ADD WITHOUT CARRY	+BL	405	4	11.1	13.3	11.1	13.3	14.5	---
BCD ADD WITH CARRY	+BC	406	4	8.4	8.9	8.4	8.9	9.1	---
DOUBLE BCD ADD WITH CARRY	+BCL	407	4	11.6	13.8	11.6	13.8	15.0	---
SIGNED BINARY SUBTRACT WITHOUT CARRY	−	410	4	0.20	0.18	0.18	0.18	0.20	---
DOUBLE SIGNED BINARY SUBTRACT WITHOUT CARRY	−L	411	4	0.36	0.32	0.32	0.32	0.34	---
SIGNED BINARY SUBTRACT WITH CARRY	−C	412	4	0.20	0.18	0.18	0.18	0.20	---
DOUBLE SIGNED BINARY SUBTRACT WITH CARRY	−CL	413	4	0.36	0.32	0.32	0.32	0.34	---
BCD SUBTRACT WITHOUT CARRY	−B	414	4	8.2	8.0	7.9	8.0	8.2	---

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
DOUBLE BCD SUBTRACT WITHOUT CARRY	–BL	415	4	11.4	12.8	11.4	12.8	14.0	---
BCD SUBTRACT WITH CARRY	–BC	416	4	8.6	8.5	8.4	8.5	8.6	---
DOUBLE BCD SUBTRACT WITH CARRY	–BCL	417	4	11.9	13.4	11.9	13.4	14.7	---
SIGNED BINARY MULTIPLY	*	420	4	0.38	0.38	0.38	0.38	0.40	---
DOUBLE SIGNED BINARY MULTIPLY	*L	421	4	6.90	7.23	6.90	7.23	8.45	---
UNSIGNED BINARY MULTIPLY	*U	422	4	0.38	0.38	0.38	0.38	0.40	---
DOUBLE UNSIGNED BINARY MULTIPLY	*UL	423	4	6.7	7.1	6.5	7.1	8.3	---
BCD MULTIPLY	*B	424	4	9.0	9.0	9.0	9.0	9.2	---
DOUBLE BCD MULTIPLY	*BL	425	4	17.8	23.0	17.8	23.0	24.2	---
SIGNED BINARY DIVIDE	/	430	4	0.44	0.40	0.40	0.40	0.42	---
DOUBLE SIGNED BINARY DIVIDE	/L	431	4	6.6	7.2	6.6	7.2	8.4	---
UNSIGNED BINARY DIVIDE	/U	432	4	0.44	0.40	0.40	0.40	0.42	---
DOUBLE UNSIGNED BINARY DIVIDE	/UL	433	4	6.5	6.9	6.4	6.9	8.1	---
BCD DIVIDE	/B	434	4	9.3	8.6	8.3	8.6	8.8	---
DOUBLE BCD DIVIDE	/BL	435	4	15.1	17.7	13.6	17.7	18.9	-

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-10 Conversion Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
BCD-TO-BINARY	BIN	023	3	0.26	0.22	0.22	0.22	0.24	---
DOUBLE BCD-TO-DOUBLE BINARY	BINL	058	3	6.4	6.5	6.4	6.5	6.8	---
BINARY-TO-BCD	BCD	024	3	0.26	0.24	0.24	0.24	0.26	---
DOUBLE BINARY-TO-DOUBLE BCD	BCDL	059	3	6.5	6.7	6.5	6.7	7.0	---
2'S COMPLEMENT	NEG	160	3	0.20	0.18	0.18	0.18	0.20	---
DOUBLE 2'S COMPLEMENT	NEGL	161	3	0.32	0.32	0.32	0.32	0.34	---
16-BIT TO 32-BIT SIGNED BINARY	SIGN	600	3	0.38	0.32	0.32	0.32	0.34	---
DATA DECODER	MLPX	076	4	0.40	0.32	0.30	0.32	0.42	Decoding 1 digit (4 to 16)
				1.20	0.98	1.00	0.98	1.20	Decoding 4 digits (4 to 16)
				3.7	3.3	3.3	3.30	4.00	Decoding 1 digit 8 to 256
				7.3	6.5	6.6	6.50	7.90	Decoding 2 digits (8 to 256)
DATA ENCODER	DMPX	077	4	7.5	7.5	7.5	7.5	7.9	Encoding 1 digit (16 to 4)
				49.6	49.6	49.6	49.6	50.2	Encoding 4 digits (16 to 4)
				18.2	18.2	18.2	18.2	18.6	Encoding 1 digit (256 to 8)
				55.1	55.1	55.1	55.1	57.4	Encoding 2 digits (256 to 8)
ASCII CONVERT	ASC	086	4	7.1	6.8	7.0	6.8	7.1	Converting 1 digit into ASCII
				10.9	11.2	10.7	11.2	11.7	Converting 4 digits into ASCII
ASCII TO HEX	HEX	162	4	6.6	7.1	6.6	7.1	7.4	Converting 1 digit
COLUMN TO LINE	LINE	063	4	14.5	19.0	13.8	19.0	23.1	---
LINE TO COLUMN	COLM	064	4	23.6	23.2	18.6	23.2	27.5	---

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
SIGNED BCD-TO-BINARY	BINS	470	4	7.3	8.0	7.3	8.0	8.3	Data format setting No. 0
				7.3	8.0	7.3	8.0	8.3	Data format setting No. 1
				7.5	8.3	7.3	8.3	8.6	Data format setting No. 2
				7.5	8.5	7.4	8.5	8.8	Data format setting No. 3
DOUBLE SIGNED BCD-TO-BINARY	BISL	472	4	6.0	9.2	5.9	9.2	9.6	Data format setting No. 0
				8.3	9.2	8.3	9.2	9.6	Data format setting No. 1
				8.4	9.5	8.4	9.5	9.9	Data format setting No. 2
				6.2	9.6	6.0	9.6	10.0	Data format setting No. 3
SIGNED BINARY-TO-BCD	BCDS	471	4	6.2	6.6	5.9	6.6	6.9	Data format setting No. 0
				6.2	6.7	6.2	6.7	7.0	Data format setting No. 1
				6.3	6.8	6.1	6.8	7.1	Data format setting No. 2
				6.4	7.2	6.4	7.2	7.5	Data format setting No. 3
DOUBLE SIGNED BINARY-TO-BCD	BDSL	473	4	7.3	8.1	7.3	8.1	8.4	Data format setting No. 0
				7.3	8.2	7.3	8.2	8.6	Data format setting No. 1
				7.5	8.3	7.5	8.3	8.7	Data format setting No. 2
				7.5	8.8	7.5	8.8	9.2	Data format setting No. 3
GRAY CODE CONVERSION	GRY	474	4	--- (See note 2.)	--- (See note 2.)	41.1	46.9	72.1	8-bit binary
						52.9	49.6	75.2	8-bit BCD
						59.7	57.7	87.7	8-bit angle
						53.4	61.8	96.7	15-bit binary
						65.1	64.5	99.6	15-bit BCD
						72.2	72.8	112.4	15-bit angle
						46.9	52.3	87.2	360° binary
						58.6	55.1	90.4	360° BCD
						64.5	64.8	98.5	360° angle
4-DIGIT NUMBER-TO-ASCII	STR4	601	3	10.4	--- (See note 3.)	10.3	--- (See note 3.)	--- (See note 3.)	
8-DIGIT NUMBER-TO-ASCII	STR8	602	3	12.1		11.5			
16-DIGIT NUMBER-TO-ASCII	STR16	603	3	18.5		18.3			

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
ASCII-TO-4-DIGIT NUMBER	NUM4	604	3	11.4	--- (See note 3.)	11.3	--- (See note 3.)	--- (See note 3.)	
ASCII-TO-8-DIGIT NUMBER	NUM8	605	3	11.7		11.6			
ASCII-TO-16-DIGIT NUMBER	NUM16	606	3	11.5		11.4			

Note
1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.
2. Not supported by Duplex CPU Systems.
3. Not supported by CS1D-CPU□□H/P and CS1D-CPU□□S.

9-5-11 Logic Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
LOGICAL AND	ANDW	034	4	0.20	0.18	0.18	0.18	0.20	---
DOUBLE LOGICAL AND	ANDL	610	4	0.36	0.32	0.32	0.32	0.34	---
LOGICAL OR	ORW	035	4	0.22	0.22	0.22	0.22	0.32	---
DOUBLE LOGICAL OR	ORWL	611	4	0.36	0.32	0.32	0.32	0.34	---
EXCLUSIVE OR	XORW	036	4	0.22	0.22	0.22	0.22	0.32	---
DOUBLE EXCLUSIVE OR	XORL	612	4	0.36	0.32	0.32	0.32	0.34	---
EXCLUSIVE NOR	XNRW	037	4	0.22	0.22	0.22	0.22	0.32	---
DOUBLE EXCLUSIVE NOR	XNRL	613	4	0.36	0.32	0.32	0.32	0.34	---
COMPLEMENT	COM	029	2	0.28	0.22	0.22	0.22	0.32	---
DOUBLE COMPLEMENT	COML	614	2	0.48	0.40	0.40	0.40	0.56	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-12 Special Math Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
BINARY ROOT	ROTB	620	3	41.2	49.6	39.5	49.6	50.0	---
BCD SQUARE ROOT	ROOT	072	3	12.2	13.7	12.1	13.7	13.9	---
ARITHMETIC PROCESS	APR	069	4	6.7	6.7	6.5	6.7	6.9	Designating SIN and COS
				17.2	17.2	17.2	17.2	18.4	Designating line-segment approximation
FLOATING POINT DIVIDE	FDIV	079	4	113.2	116.6	113.2	116.6	176.6	---
BIT COUNTER	BCNT	067	4	0.34	0.30	0.30	0.30	0.38	Counting 1 word

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-13 Floating-point Math Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
FLOATING TO 16-BIT	FIX	450	3	6.2	10.6	5.0	10.6	10.8	---
FLOATING TO 32-BIT	FIXL	451	3	6.8	10.8	6.2	10.8	11.0	---
16-BIT TO FLOATING	FLT	452	3	5.7	8.3	5.6	8.3	8.5	---
32-BIT TO FLOATING	FLTL	453	3	5.7	8.3	5.5	8.3	8.5	---
FLOATING-POINT ADD	+F	454	4	7.0	8.0	6.8	8.0	9.2	---
FLOATING-POINT SUBTRACT	−F	455	4	8.0	8.0	8.0	8.0	9.2	---
FLOATING-POINT DIVIDE	/F	457	4	8.7	8.7	8.7	8.7	9.9	---
FLOATING-POINT MULTIPLY	*F	456	4	6.8	8.0	6.8	8.0	9.2	---
DEGREES TO RADIANS	RAD	458	3	10.0	10.1	10.0	10.1	10.2	---
RADIANS TO DEGREES	DEG	459	3	8.8	9.9	8.8	9.9	10.1	---
SINE	SIN	460	3	42.0	42.0	42.0	42.0	42.2	---
COSINE	COS	461	3	31.5	31.5	31.5	31.5	31.8	---

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
TANGENT	TAN	462	3	16.3	16.3	16.3	16.3	16.6	---
ARC SINE	ASIN	463	3	17.6	17.6	17.6	17.6	17.9	---
ARC COSINE	ACOS	464	3	20.4	20.4	20.4	20.4	20.7	---
ARC TANGENT	ATAN	465	3	16.1	16.1	16.1	16.1	16.4	---
SQUARE ROOT	SQRT	466	3	6.1	19.0	4.6	19.0	19.3	---
EXPONENT	EXP	467	3	6.2	65.9	6.1	65.9	66.2	---
LOGARITHM	LOG	468	3	8.6	12.8	4.7	12.8	13.1	---
EXPONENTIAL POWER	PWR	840	4	92.8	125.4	92.4	125.4	126.0	---
Floating Symbol Comparison	LD, AND, OR+=F	329	3	5.8	6.6	5.6	6.6	8.3	---
	LD, AND, OR+<>F	330							
	LD, AND, OR+<F	331							
	LD, AND, OR+<=F	332							
	LD, AND, OR+>F	333							
	LD, AND, OR+>=F	334							
FLOATING-POINT TO ASCII	FSTR	448	4	48.5	48.5	48.5	48.5	48.9	---
ASCII TO FLOATING-POINT	FVAL	449	3	21.1	21.1	21.1	21.1	21.3	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-14 Double-precision Floating-point Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
DOUBLE SYMBOL COMPARISON	LD, AND, OR+=D	335	3	7.3	8.5	6.9	8.5	10.3	---
	LD, AND, OR+<>D	336							
	LD, AND, OR+<D	337							
	LD, AND, OR+<=D	338							
	LD, AND, OR+>D	339							
	LD, AND, OR+>=D	340							
DOUBLE FLOATING TO 16-BIT BINARY	FIXD	841	3	9.1	11.7	8.9	11.7	12.1	---
DOUBLE FLOATING TO 32-BIT BINARY	FIXLD	842	3	9.1	11.6	8.8	11.6	12.1	---
16-BIT BINARY TO DOUBLE FLOATING	DBL	843	3	8.0	9.9	8.0	9.9	10.0	---
32-BIT BINARY TO DOUBLE FLOATING	DBLL	844	3	7.8	9.8	7.0	9.8	10.0	---
DOUBLE FLOATING-POINT ADD	+D	845	4	10.0	11.2	10.0	11.2	11.9	---
DOUBLE FLOATING-POINT SUBTRACT	−D	846	4	9.8	11.2	9.8	11.2	11.9	---
DOUBLE FLOATING-POINT MULTIPLY	*D	847	4	11.6	12.0	10.1	12.0	12.7	---
DOUBLE FLOATING-POINT DIVIDE	/D	848	4	14.8	23.5	14.8	23.5	24.2	---
DOUBLE DEGREES TO RADIANS	RADD	849	3	16.0	27.4	16.0	27.4	27.8	---
DOUBLE RADIANS TO DEGREES	DEGD	850	3	11.5	11.2	11.5	11.2	11.9	---
DOUBLE SINE	SIND	851	3	34.1	45.4	34.1	45.4	45.8	---

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
DOUBLE COSINE	COSD	852	3	32.9	43.0	32.6	43.0	43.4	---
DOUBLE TANGENT	TAND	853	3	15.2	20.1	15.1	20.1	20.5	---
DOUBLE ARC SINE	ASIND	854	3	15.6	21.5	15.4	21.5	21.9	---
DOUBLE ARC COSINE	ACOSD	855	3	17.1	24.7	17.0	24.7	25.1	---
DOUBLE ARC TAN-GENT	ATAND	856	3	10.8	19.3	10.6	19.3	19.7	---
DOUBLE SQUARE ROOT	SQRTD	857	3	40.8	47.4	40.8	47.4	47.9	---
DOUBLE EXPONENT	EXPD	858	3	94.9	121	94.9	121.0	121.4	---
DOUBLE LOGA-RITHM	LOGD	859	3	11.1	16.0	11.1	16.0	16.4	---
DOUBLE EXPONEN-TIAL POWER	PWRD	860	4	193.5	223.9	193.1	223.9	224.2	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-15 Table Data Processing Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
SET STACK	SSET	630	3	10.6	8.0	10.1	8.0	8.3	Designating 5 words in stack area
				235.4	231.6	235.4	231.6	251.8	Designating 1,000 words in stack area
PUSH ONTO STACK	PUSH	632	3	5.5	6.5	5.3	6.5	8.6	---
FIRST IN FIRST OUT	FIFO	633	3	5.9	6.9	5.0	6.9	8.9	Designating 5 words in stack area
				204.1	352.6	184.1	352.6	434.3	Designating 1,000 words in stack area
LAST IN FIRST OUT	LIFO	634	3	5.2	7.0	5.1	7.0	9.0	---
DIMENSION RECORD TABLE	DIM	631	5	15.1	15.2	15.1	15.2	21.6	---

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
SET RECORD LOCATION	SETR	635	4	4.3	5.4	4.3	5.4	5.9	---
GET RECORD NUMBER	GETR	636	4	4.4	7.8	4.4	7.8	8.4	---
DATA SEARCH	SRCH	181	4	14.5	15.5	14.5	15.5	19.5	Searching for 1 word
				2806.0	2.42 ms	2496.0	2.42 ms	3.34 ms	Searching for 1,000 words
SWAP BYTES	SWAP	637	3	11.7	12.2	11.7	12.2	13.6	Swapping 1 word
				1950.0	1.94 ms	1917.0	1.94 ms	2.82 ms	Swapping 1,000 words
FIND MAXIMUM	MAX	182	4	19.1	19.2	19.1	19.2	24.9	Searching for 1 word
				2331.0	2.39 ms	2331.0	2.39 ms	3.36 ms	Searching for 1,000 words
FIND MINIMUM	MIN	183	4	19.0	19.2	19.0	19.2	25.3	Searching for 1 word
				2330.0	2.39 ms	229.07	2.39 ms	3.33 ms	Searching for 1,000 words
SUM	SUM	184	4	22.5	28.2	12.6	28.2	38.5	Adding 1 word
				1172.0	1.42 ms	1130.0	1.42 ms	1.95 ms	Adding 1,000 words
FRAME CHECKSUM	FCS	180	4	19.0	20.0	19.0	20.0	28.3	For 1-word table length
				1480.0	16.5 ms	1447.0	16.5 ms	2.48 ms	For 1,000-word table length
STACK SIZE READ	SNUM	638	3	6.3	6.0	6.0	6.0	6.3	---
STACK DATA READ	SREAD	639	4	6.6	8.0	5.4	8.0	8.4	---
STACK DATA OVERWRITE	SWRIT	640	4	6.2	7.2	5.0	7.2	7.6	---
STACK DATA INSERT	SINS	641	4	6.3	7.8	5.2	7.8	9.9	For 1,000-word table
				175.5	354	175.5	354.0	434.8	---
STACK DATA DELETE	SDEL	642	4	6.7	8.6	5.4	8.6	10.6	---
				404.1	354	362.8	354.0	436.0	For 1,000-word table

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-16 Data Control Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
PID CONTROL	PID	190	4	416.0 (simplex) 840.0 (duplex)	436.2 (simplex) 676.2 (duplex)	410.0	436.2	678.2	Initial execution
				324.0 (simplex) 487.6 (duplex)	332.3 (simplex) 572.3 (duplex)	308.0	308.0	474.9	Sampling
				88.2 (simplex) 490.3 (duplex)	97.3 (simplex) 337.3 (duplex)	82.2	82.2	141.3	Not sampling
LIMIT CONTROL	LMT	680	4	13.6	16.1	13.6	16.1	22.1	---
DEAD BAND CONTROL	BAND	681	4	14.2	17.0	14.2	17.0	22.5	---
DEAD ZONE CONTROL	ZONE	682	4	8.6	15.4	8.6	15.4	20.5	---
TIME-PROPORTIONAL OUTPUT	TPO	685	4	--- (See note 2.)	--- (See note 2.)	7.8	10.6	14.8	OFF execution time
						47.4	54.5	82.0	ON execution time with duty designation or displayed output limit
						48.4	61.0	91.9	ON execution time with manipulated variable designation and output limit enabled
SCALING	SCL	194	4	11.4	37.1	11.4	37.1	53.0	---
SCALING 2	SCL2	486	4	10.4	28.5	10.4	28.5	40.2	---
SCALING 3	SCL3	487	4	12.3	33.4	12.3	33.4	47.0	---
AVERAGE	AVG	195	4	31.6	36.3	31.6	36.3	52.6	Average of an operation
				266.7	291.0	263.0	291.0	419.9	Average of 64 operations
PID CONTROL WITH AUTOTUNING	PIDAT	191	4	412.0	446.3	412.0	446.3	712.5	Initial execution
				314.0	339.4	314.0	339.4	533.9	Sampling
				83.0	100.7	79.8	100.7	147.1	Not sampling
				164.0	189.2	161.0	189.2	281.6	Initial execution of autotuning
				410.0	535.2	406.0	535.2	709.8	Autotuning when sampling

Note 1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.

2. Not supported by Duplex CPU Systems.

9-5-17 Subroutine Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
SUBROUTINE CALL	SBS	091	2	5.40	1.26	5.40	1.26	1.96	---
SUBROUTINE ENTRY	SBN	092	2	---	---	---	---	---	---
SUBROUTINE RETURN	RET	093	1	0.86	0.86	0.86	0.86	1.60	---
MACRO	MCRO	099	4	21.7	23.3	21.7	23.3	23.3	---
GLOBAL SUBROUTINE CALL	GSBN	751	2	---	---	---	---	---	---
GLOBAL SUBROUTINE ENTRY	GRET	752	1	0.86	0.86	0.86	0.86	1.60	---
GLOBAL SUBROUTINE RETURN	GSBS	750	2	1.26	1.26	1.26	1.26	1.96	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-18 Interrupt Control Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
SET INTERRUPT MASK	MSKS	690	3	--- (See note 2.)	--- (See note 2.)	26.2	25.6	38.4	---
READ INTERRUPT MASK	MSKR	692	3	--- (See note 2.)	--- (See note 2.)	11.4	11.9	11.9	---
CLEAR INTERRUPT	CLI	691	3	--- (See note 2.)	--- (See note 2.)	31.1	27.4	41.3	---
DISABLE INTERRUPTS	DI	693	1	15.3	15.0	15.3	15.0	16.8	---
ENABLE INTERRUPTS	EI	694	1	15.0	19.5	15.0	19.5	21.8	---

Note
1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.
2. Not supported by Duplex CPU Systems.

9-5-19 Step Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
STEP DEFINE	STEP	008	2	12.6	17.4	12.6	17.4	20.7	Step control bit ON
				13.4	11.8	13.4	11.8	13.7	Step control bit OFF
STEP START	SNXT	009	2	6.4	6.6	6.1	6.6	7.3	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-20 Basic I/O Unit Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
I/O REFRESH	IORF	097	3	39.2 (simplex) 447.4 (duplex)	15.5 (simplex) 255.5 (duplex)	14.4	15.5	16.4	1-word refresh for input words
				41.3 (simplex) 440.3 (duplex)	17.2 (simplex) 257.2 (duplex)	15.9	17.2	18.4	1-word refresh output words
				384.1 (simplex) 800.7 (duplex)	319.9 (simplex) 559.9 (duplex)	278.4	319.9	320.7	60-word refresh input words
				430.5 (simplex) 815.7 (duplex)	358.0 (simplex) 598.0 (duplex)	314.7	358.0	354.4	60-word refresh output words
7-SEG-MENT DECODER	SDEC	078	4	6.6	6.5	6.6	6.5	6.9	---
DIGITAL SWITCH INPUT	DSW	210	6	--- (See note 2.)	--- (See note 2.)	17.0	50.7	73.5	4 digits, data input value: 0
						17.0	51.5	73.4	4 digits, data input value: F
						17.0	51.3	73.5	8 digits, data input value: 0
						17.0	50.7	73.4	8 digits, data input value: F
TEN KEY INPUT	TKY	211	4	--- (See note 2.)	--- (See note 2.)	9.5	9.7	13.2	Data input value: 0
						10.0	10.7	14.8	Data input value: F
HEXADECI-MAL KEY INPUT	HKY	212	5	--- (See note 2.)	--- (See note 2.)	16.8	50.3	70.9	Data input value: 0
						16.8	50.1	71.2	Data input value: F

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
MATRIX INPUT	MTR	213	5	--- (See note 2.)	--- (See note 2.)	17.0	47.8	68.1	Data input value: 0
						17.0	48.0	68.0	Data input value: F
7-SEGMENT DISPLAY OUTPUT	7SEG	214	5	--- (See note 2.)	--- (See note 2.)	17.6	58.1	83.3	4 digits
						17.6	63.3	90.3	8 digits
INTELLIGENT I/O READ	IORD	222	4	--- (See note 3.)	--- (See note 3.)	--- (See note 3.)	--- (See note 3.)	--- (See note 3.)	---
	IOWR	223	4	--- (See note 3.)	--- (See note 3.)	--- (See note 3.)	--- (See note 3.)	--- (See note 3.)	---
	DLNK	226	4	270.0 (simplex) 672.0 (duplex)	287.8 (simplex) 527.8 (duplex)	206.0	287.8	315.5	Allocated 1 word

Note
1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.
2. Not supported by Duplex CPU Systems.
3. Read/write times depend on the Special I/O Unit for which the instruction is being executed.

9-5-21 Serial Communications Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
PROTOCOL MACRO	PMCR	260	5	140.0	100.1	140.0	100.1	142.1	Sending 0 words, receiving 0 words
				140.0	134.2	140.0	134.2	189.6	Sending 249 words, receiving 249 words
TRANSMIT	TXD	236	4	55.7	68.5	55.7	68.5	98.8	Sending 1 byte
				670.0	734.3	640.0	734.3	1.10 ms	Sending 256 bytes
RECEIVE	RXD	235	4	116.7 (simplex) 492.1 (duplex)	89.6 (simplex) 329.6 (duplex)	86.5	89.6	131.1	Storing 1 byte
				630.0 (simplex) 1005.4 (duplex)	724.2 (simplex) 964.2 (duplex)	630.0	724.2	1.11 ms	Storing 256 bytes

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
Serial Communications Unit serial port output	TXDU	256	4	--- (See note 2.)	--- (See note 2.)	139.0	--- (See note 2.)	--- (See note 2.)	
Serial Communications Unit serial port input	RXDU	255	4			141.0			
CHANGE SERIAL PORT SETUP	STUP	237	3	306.0	341.2	189.0	341.2	400.0	---

Note
1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.
2. Not supported by CS1D Duplex-CPU Systems and CS1D-CPU□□S.

9-5-22 Network Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
NETWORK SEND	SEND	090	4	110.0	84.4	103.0	84.4	123.9	---
NETWORK RECEIVE	RECV	098	4	111.0	85.4	105.0	85.4	124.7	---
DELIVER COMMAND	CMND	490	4	128.0	106.8	122.0	106.8	136.8	---
EXPLICIT MESSAGE SEND	EXPLT	720	4	--- (See note 2.)	--- (See note 2.)	125.2	127.6	190.0	---
EXPLICIT GET ATTRIBUTE	EGATR	721	4	--- (See note 2.)	--- (See note 2.)	121.6	123.9	185.0	---
EXPLICIT SET ATTRIBUTE	ESATR	722	3	--- (See note 2.)	--- (See note 2.)	111.1	110.0	164.4	---
EXPLICIT WORD READ	ECHRD	723	4	--- (See note 2.)	--- (See note 2.)	106.7	106.8	158.9	---
EXPLICIT WORD WRITE	ECHWR	724	4	--- (See note 2.)	--- (See note 2.)	107.1	106.0	158.3	---

Note
1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.
2. Not supported by Duplex CPU Systems.

9-5-23 File Memory Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
READ DATA FILE	FREAD	700	5	328.0 (simplex) 452.0 (duplex)	391.4 (simplex) 631.4 (duplex)	298.0	391.4	632.4	Binary data
									2-character directory + file name in binary
				628.0 (simplex) 990.0 (duplex)	836.1 (simplex) 1,076.1 (duplex)	592.0	836.1	1.33 ms	Binary data
									73-character directory + file name in binary
WRITE DATA FILE	FWRIT	701	5	340.0 (simplex) 484.0 (duplex)	387.8 (simplex) 627.8 (duplex)	300.0	387.8	627.0	Binary data
									2-character directory + file name in binary
				636.0 (simplex) 1030.0 (duplex)	833.3 (simplex) 1,073.3 (duplex)	584.0	833.3	1.32 ms	Binary data
									73-character directory + file name in binary
WRITE TEXT FILE	TWRIT	704	5	323.1 (simplex) 744.5 (duplex)	--- (See note 2.)	276.9	--- (See note 2.)	--- (See note 2.)	2-character directory + file name
				638.0 (simplex) 1068.1 (duplex)		602.2			73-character directory + file name

Note
1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.
2. Not supported by CS1D-CPU6□H and CS1D-CPU□□S.

9-5-24 Display Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
DISPLAY MESSAGE	MSG	046	3	10.2	10.1	9.5	10.1	14.2	Displaying message
				9.3	8.4	8.8	8.4	11.3	Deleting displayed message

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-25 Clock Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
CALENDAR ADD	CADD	730	4	94.1	38.3	93.7	38.3	201.9	---
CALENDAR SUBTRACT	CSUB	731	4	81.9	38.6	81.8	38.6	170.4	---
HOURS TO SECONDS	SEC	065	3	19.7	21.4	19.7	21.4	29.3	---
SECONDS TO HOURS	HMS	066	3	19.5	22.2	19.4	22.2	30.9	---
CLOCK ADJUST-MENT	DATE	735	2	39.3	60.5	39.3	60.5	87.4	---

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-26 Debugging Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
Trace Mem-ory Sampling	TRSM	045	1	123.1	80.4	123.1	80.4	120.0	Sampling 1 bit and 0 words
				547.1	848.1	547.1	848.1	1.06 ms	Sampling 31 bits and 6 words

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-27 Failure Diagnosis Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
FAILURE ALARM	FAL	006	3	244.4	15.4	231.9	15.4	16.7	Recording errors
				178.2	179.8	178.2	179.8	244.8	Deleting errors (in order of priority)
				396.3	432.4	320.9	432.4	657.1	Deleting errors (all errors)
				156.5	161.5	117.9	161.5	219.4	Deleting errors (individually)
SEVERE FAILURE ALARM	FALS	007	3	---	---	---	---	---	---
FAILURE POINT DETECTION	FPD	269	4	237.8	140.9	237.8	140.9	202.3	Bit address output, time monitored
				482.2	163.4	468.6	163.4	217.6	Bit address output, first error detection
				265.0	185.2	265.0	185.2	268.9	Message characters output, time monitored
				509.3	207.5	495.8	207.5	283.6	Message characters output, first error detection

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-28 Other Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
SET CARRY	STC	040	1	0.06	0.06	0.06	0.06	0.06	---
CLEAR CARRY	CLC	041	1	0.06	0.06	0.06	0.06	0.06	---
SELECT EM BANK	EMBC	281	2	14.6	14.0	14.5	14.0	15.1	---
EXTEND MAXIMUM CYCLE TIME	WDT	094	2	15.1	15.0	15.1	15.0	19.7	---
SAVE CONDITION FLAGS	CCS	282	1	9.2	8.6	9.2	8.6	12.5	---
LOAD CONDITION FLAGS	CCL	283	1	10.5	9.8	10.5	9.8	13.9	---
CONVERT ADDRESS FROM CV	FRMCV	284	3	10.2	13.6	10.2	13.6	19.9	---
CONVERT ADDRESS TO CV	TOCV	285	3	11.9	11.9	11.9	11.9	17.2	---
DISABLE PERIPHERAL SERVICING	IOSP	287	1	--- (See note 2.)	--- (See note 2.)	12.5	13.9	19.8	---
ENABLE PERIPHERAL SERVICING	IORS	288	1	--- (See note 2.)	--- (See note 2.)	56.5	63.6	92.3	---

Note
1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.
2. Not supported by Duplex CPU Systems.

9-5-29 Block Programming Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
BLOCK PROGRAM BEGIN	BPRG	096	2	9.0	12.1	9.0	12.1	13.0	---
BLOCK PROGRAM END	BEND	801	1	8.0	9.6	8.0	9.6	12.3	---
BLOCK PROGRAM PAUSE	BPPS	811	2	7.0	10.6	7.0	10.6	12.3	---
BLOCK PROGRAM RESTART	BPRS	812	2	3.0	5.1	3.0	5.1	5.6	---
CONDITIONAL BLOCK EXIT	Execution condition	806	1	9.8	10.0	9.8	10.0	11.3	EXIT condition satisfied
	EXIT			4.9	4.0	4.9	4.0	4.9	EXIT condition not satisfied
CONDITIONAL BLOCK EXIT	EXIT (bit address)	806	2	11.6	6.8	11.6	6.8	13.5	EXIT condition satisfied
				6.4	4.7	6.4	4.7	7.2	EXIT condition not satisfied
CONDITIONAL BLOCK EXIT (NOT)	EXIT NOT (bit address)	806	2	11.6	12.4	11.6	12.4	14.0	EXIT condition satisfied
				6.4	7.1	6.4	7.1	7.6	EXIT condition not satisfied
Branching	Execution condition	802	1	2.7	4.6	2.6	4.6	4.8	IF true
	IF			4.6	6.7	4.6	6.7	7.3	IF false
Branching	IF (relay number)	802	2	4.6	6.8	4.2	6.8	7.2	IF true
				6.4	9.0	6.2	9.0	9.6	IF false
Branching (NOT)	IF NOT (relay number)	802	2	4.8	7.1	4.4	7.1	7.6	IF true
				6.4	9.2	6.3	9.2	10.1	IF false
Branching	ELSE	803	1	3.9	6.2	3.9	6.2	6.7	IF true
				4.6	6.8	2.4	6.8	7.7	IF false
Branching	IEND	804	1	4.4	6.9	4.4	6.9	7.7	IF true
				8.5	4.4	8.5	4.4	4.6	IF false
ONE CYCLE AND WAIT	Execution condition	805	1	12.9	12.6	12.9	12.6	13.7	WAIT condition satisfied
	WAIT			5.2	3.9	5.2	3.9	4.1	WAIT condition not satisfied
ONE CYCLE AND WAIT	WAIT (relay number)	805	2	12.0	12.0	12.0	12.0	13.4	WAIT condition satisfied
				7.0	6.1	7.0	6.1	6.5	WAIT condition not satisfied
ONE CYCLE AND WAIT (NOT)	WAIT NOT (relay number)	805	2	12.0	12.2	12.0	12.2	13.8	WAIT condition satisfied
				7.0	6.4	7.0	6.4	6.9	WAIT condition not satisfied

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
COUNTER WAIT	CNTW	814	4	18.0	17.9	18.0	17.9	22.6	Default setting
				16.8	19.1	16.8	19.1	23.9	Normal execution
	CNTWX	818	4	17.0	17.9	17.0	17.9	22.6	Default setting
				21.4	19.1	21.4	19.1	23.9	Normal execution
HIGH-SPEED TIMER WAIT	TMHW	815	3	20.8	25.8	20.8	25.8	27.9	Default setting
				22.2	20.6	17.6	20.6	22.7	Normal execution
	TMHWX	817	3	20.4	25.8	20.4	25.8	27.9	Default setting
				21.0	20.6	17.6	20.6	22.7	Normal execution
Loop Control	LOOP	809	1	5.2	7.9	5.2	7.9	9.1	---
Loop Control	Execution condition	810	1	4.2	7.7	4.2	7.7	8.4	LEND condition satisfied
	LEND			5.2	6.8	5.2	6.8	8.0	LEND condition not satisfied
Loop Control	LEND (relay number)	810	2	6.8	9.9	6.8	9.9	10.7	LEND condition satisfied
				6.8	8.9	6.0	8.9	10.3	LEND condition not satisfied
Loop Control	LEND NOT (relay number)	810	2	6.8	10.2	6.8	10.2	11.2	LEND condition satisfied
				7.2	9.3	6.0	9.3	10.8	LEND condition not satisfied
TIMER WAIT	TIMW	813	3	20.4	22.3	20.4	22.3	25.2	Default setting
				20.8	24.9	20.8	24.9	27.8	Normal execution
	TIMWX	816	3	19.6	22.3	19.6	22.3	25.2	Default setting
				21.2	24.9	21.2	24.9	27.8	Normal execution

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-30 Text String Processing Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
MOV STRING	MOV$	664	3	43.6	45.6	43.6	45.6	66.0	Transferring 1 character
CONCATE-NATE STRING	+$	656	4	80.9	86.5	80.9	86.5	126.0	1 character + 1 character
GET STRING LEFT	LEFT$	652	4	47.7	53.0	47.7	53.0	77.4	Retrieving 1 character from 2 characters
GET STRING RIGHT	RGHT$	653	4	45.4	52.2	45.4	52.2	76.3	Retrieving 1 character from 2 characters
GET STRING MIDDLE	MID$	654	5	50.6	56.5	50.6	56.5	84.6	Retrieving 1 character from 3 characters
FIND IN STRING	FIND$	660	4	43.2	51.4	43.2	51.4	77.5	Searching for 1 character from 2 characters
STRING LENGTH	LEN$	650	3	18.9	19.8	18.9	19.8	28.9	Detecting 1 character
REPLACE IN STRING	RPLC$	661	6	162.0	175.1	162.0	175.1	258.7	Replacing the first of 2 characters with 1 character
DELETE STRING	DEL$	658	5	65.9	63.4	65.9	63.4	94.2	Deleting the leading character of 2 characters
EXCHANGE STRING	XCHG$	665	3	57.3	60.6	57.3	60.6	87.2	Exchanging 1 character with 1 character
CLEAR STRING	CLR$	666	2	21.1	23.8	21.1	23.8	36.0	Clearing 1 character
INSERT INTO STRING	INS$	657	5	111.0	136.5	111.0	136.5	200.6	Inserting 1 character after the first of 2 characters
String Comparison Instructions	LD, AND, OR+=$	670	4	37.9	48.5	31.5	48.5	69.8	Comparing 1 character with 1 character
	LD, AND, OR+<>$	671							
	LD, AND, OR+<$	672							
	LD, AND, OR+>$	674							
	LD, AND, OR+>=$	675							

Note When a double-length operand is used, add 1 to the value shown in the length column in the following table.

9-5-31 Task Control Instructions

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
TASK ON	TKON	820	2	15.7	19.5	15.2	19.5	26.3	Cyclic task specified
TASK OFF	TKOF	821	2	81.5	13.3	80.9	13.3	19.0	Cyclic task specified

9-5-32 Special Instructions for Function Blocks

Instruction	Mnemonic	Code	Length (steps) (See note 1.)	Execution time (μs)					Conditions
				CPU6□HA (Duplex CPU)	CPU6□H (Duplex CPU)	CPU□□SA (Single CPU)	CPU6□S (Single CPU)	CPU4□S (Single CPU)	
VARIABLE TYPE ACQUISITION	GETID	286	4	15.0	--- (See note 2.)	14.9	--- (See note 2.)	--- (See note 2.)	

Note 1. When a double-length operand is used, add 1 to the value shown in the length column in the following table.

2. Not supported by CS1D-CPU□□H and CS1D-CPU□□S.

9-5-33 Function Block Instance Execution Time (CS1D-CPU□□HA/SA)

Use the following equation to calculate the effect of instance execution on the cycle time when function block definitions have been created and the instances copied into the user program.

Effect of Instance Execution on Cycle Time
= Startup time (A)
+ I/O parameter transfer processing time (B)
+ Execution time of instructions in function block definition (C)

The following table shows the length of time for A, B, and C.

Operation			CPU Unit model	
			CS1D-CPU□□HA	CS1D-CPU□□SA
A	Startup time	Startup time not including I/O parameter transfer	8.0 μs	6.9 μs
B	I/O parameter transfer processing time The data type is indicated in parentheses.	1-bit I/O variable (BOOL)	0.6 μs	0.5 μs
		1-word I/O variable (INT, UINT, WORD)	0.5 μs	0.4 μs
		2-word I/O variable (DINT, UDINT, DWORD, REAL)	0.7 μs	0.7 μs
		4-word I/O variable (LINT, ULINT, LWORD, LREAL)	2.4 μs	2.2 μs
		I/O variable	0.7 μs	0.6 μs
C	Function block definition instruction execution time	Total instruction processing time (same as standard user program)		

Example: CS1D-CPU68HA
Input variables with a 1-word data type (INT): 3
Output variables with a 1-word data type (INT): 2
Total instruction processing time in function block definition section: 10 μs
Execution time for 1 instance = 8.0 μs + (3 + 2) × 0.5 μs + 10 μs = 20.5 μs

Note The execution time is increased according to the number of multiple instances when the same function block definition has been copied to multiple locations.

Guidelines on Converting Program Capacities from Previous OMRON PLCs

Guidelines are provided in the following table for converting the program capacity (unit: words) of previous OMRON PLCs (SYSMAC C200HX/HG/HE, CVM1, or CV-series PLCs) to the program capacity (unit: steps) of the CS-series PLCs.

Add the following value (n) to the program capacity (unit: words) of the previous PLCs for each instruction to obtain the program capacity (unit: steps) of the CS-series PLCs.

CS-series steps = "a" (words) of previous PLC + n			
Instructions	**Variations**	**Value of n when converting from C200HX/HG/HE to CS Series**	**Value of n when converting from CV-series PLC or CVM1 to CS Series**
Basic instructions	None	OUT, SET, RSET, or KEEP(011): –1 Other instructions: 0	0
	Upward Differentiation	None	+1
	Immediate Refreshing (See note.)	Not supported by CS1D.	---
	Upward Differentiation and Immediate Refreshing (See note.)	Not supported by CS1D.	---

CS-series steps = "a" (words) of previous PLC + n			
Instructions	**Variations**	**Value of n when converting from C200HX/HG/HE to CS Series**	**Value of n when converting from CV-series PLC or CVM1 to CS Series**
Special instructions	None	0	–1
	Upward Differentiation	+1	0
	Immediate Refreshing (See note.)	Not supported by CS1D.	---
	Upward Differentiation and Immediate Refreshing (See note.)	Not supported by CS1D.	---

Note Duplex CPU Systems only. These functions are not supported by Duplex CPU Systems.

For example, if OUT is used with an address of CIO 000000 to CIO 25515, the program capacity of the previous PLC would be 2 words per instruction and that of the CS-series PLC would be 1 (2 – 1) step per instruction.

For example, if !MOV is used (MOVE instruction with immediate refreshing), the program capacity of a CV-series PLC would be 4 words per instruction and that of the CJ-series PLC would be 7 (4 + 3) steps. (Duplex CPU Systems only. Immediate refreshing is not supported by Duplex CPU Systems.)

Number of Function Block Program Steps (CS1D-CPU□□HA/SA)

Use the following equation to calculate the number of program steps when function block definitions have been created and the instances copied into the user program.

Number of steps

= Number of instances × (Call part size m + I/O parameter transfer part size n × Number of parameters) + Number of instruction steps in the function block definition p (See note.)

Note The number of instruction steps in the function block definition (p) will not be diminished in subsequence instances when the same function block definition is copied to multiple locations (i.e., for multiple instances). Therefore, in the above equation, the number of instances is not multiplied by the number of instruction steps in the function block definition (p).

Contents			**Steps**
m	Call part		57 steps
n	I/O parameter transfer part The data type is shown in parentheses.	1-bit I/O variable (BOOL)	6 steps
		1-word I/O variable (INT, UINT, WORD)	6 steps
		2-word I/O variable (DINT, UDINT, DWORD, REAL)	6 steps
		4-word I/O variable (LINT, ULINT, LWORD, LREAL)	12 steps
p	Number of instruction steps in function block definition	The total number of instruction steps (same as standard user program) + 27 steps.	

Example:
Input variables with a 1-word data type (INT): 5
Output variables with a 1-word data type (INT): 5
Function block definition section: 100 steps
Number of steps for 1 instance = 57 + (5 + 5) × 6 steps + 100 steps + 27 steps = 244 steps

SECTION 10
Troubleshooting

This section provides information on hardware and software errors that occur during PLC operation.

10-1 Error Log

Each time that an error occurs, the CPU Unit stores error information in the Error Log Area. The error information includes the error code (stored in A400), error contents, and time that the error occurred. Up to 20 records can be stored in the Error Log.

Errors Generated by FAL(006)/FALS(007)

In addition to system-generated errors, the PLC records user-defined FAL(006) and FALS(007) errors, making it easier to track the operating status of the system.

A user-defined error is generated when FAL(006) or FALS(007) is executed in the program. The execution conditions of these instructions constitute the user-defined error conditions. FAL(006) generates a non-fatal error and FALS(007) generates a fatal error. With a Single CPU System, CPU Unit operation will stop for a FALS error. With a Duplex CPU System in Duplex Mode, operation will switch to the standby CPU Unit for a FALS error and operation will continue. With a Duplex CPU System in Simplex Mode, CPU Unit operation will stop for a FALS error.

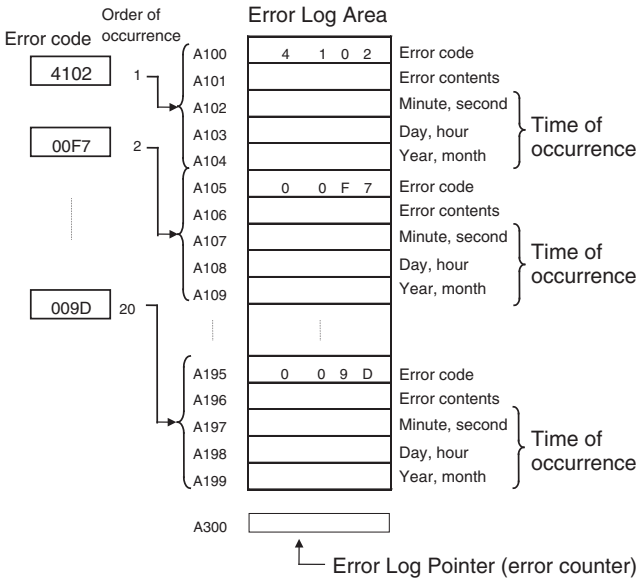
The following table shows the error codes for FAL(006) (beginning with “4”) and FALS(007) (beginning with “C”).

Instruction	FAL numbers	Error codes
FAL(006)	#0001 to #01FF hex (1 to 511 decimal)	4101 to 42FF
FALS(007)	#0001 to #01FF hex (1 to 511 decimal)	C101 to C2FF

The time the error occurred is also stored. If the program generates an FAL error, the CPU Unit will continue operation. If it generates an FALS error in Duplex Mode, the standby CPU Unit will become the active CPU Unit unless the error occurs in both CPU Units, in which case both CPU Units will stop.

Error Log Structure

When more than 20 errors occur, the oldest error data (in A100 to A104) is deleted, the errors in A105 to A199 are shifted by one, and the newest record is stored in A195 to A199.



The number of records is stored in binary in the Error Log Pointer (A300).

Note The Error Log Pointer can be reset by turning ON the Error Log Pointer Reset Bit (A50014). This operation will also clear the error log display for Programming Devices, but it will not clear the data in the Error Log itself (A100 to A199).

10-2 Error Processing

10-2-1 Error Categories

Error are classified as shown in the following table for CS1D Duplex Systems.

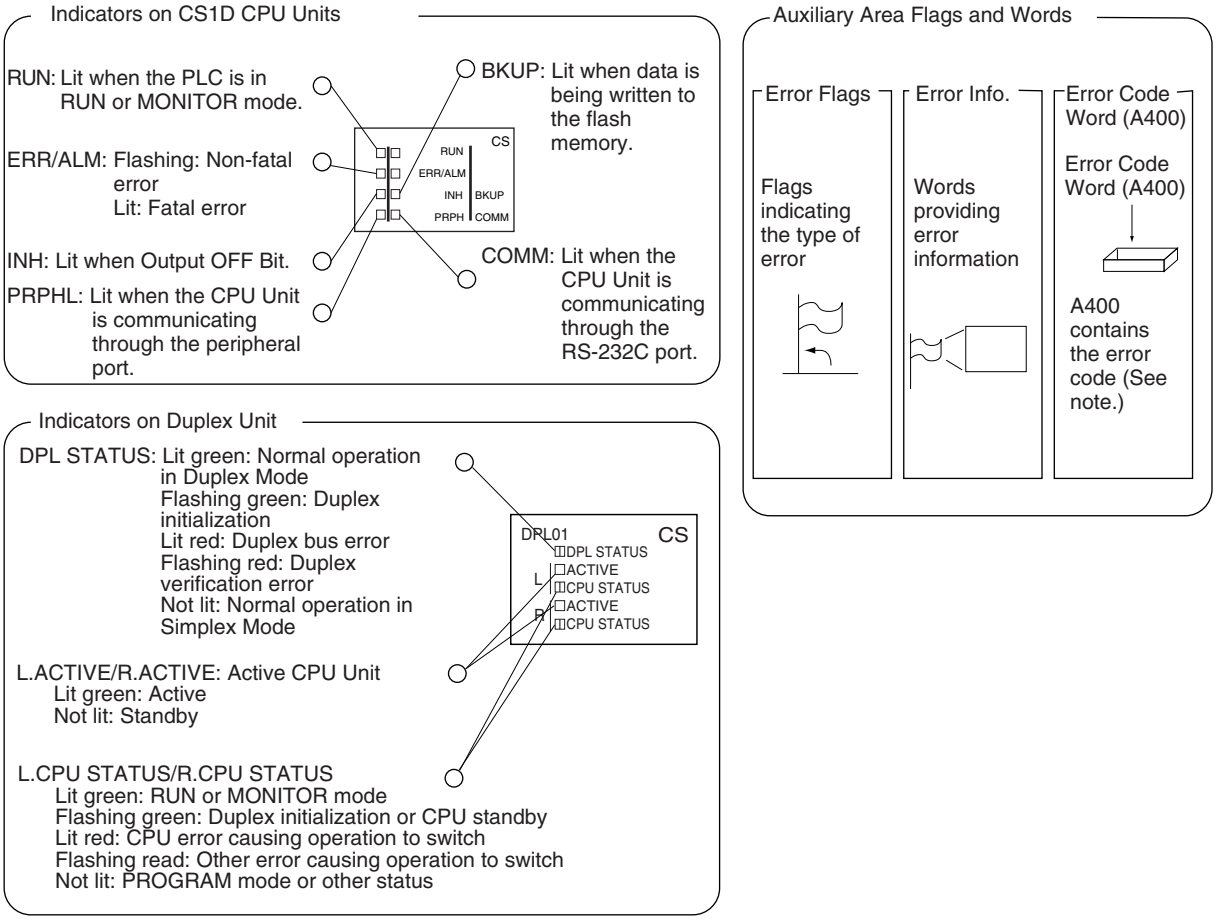
Error status		Duplex CPU Systems		Single CPU Systems
		Duplex Mode	Simplex Mode	
Operation switching errors • CPU errors • Memory errors • Program errors • Cycle time overrun errors • FALS execution • Fatal Inner Board errors (Single CPU Systems or Process-control CPU Units only)		Operation continues in Simplex Mode with the standby CPU Unit being switched to the active CPU Unit. Operation stops if the error occurs in both CPU Units.	Operation stops.	Operation stops.
Fatal errors • I/O bus errors • Number duplication errors (unit numbers or rack numbers) • Too many I/O points • I/O setting errors		Operation stops.		
Non-fatal errors	Duplex errors (errors causing a switch to Simplex Mode) • Duplex verification errors • Duplex bus errors	Operation continues, in Simplex Mode without changing the active CPU Unit.	Operation continues.	Will not occur on a Single CPU System.
	Errors for which Duplex Mode continues • Duplex power supply error • Duplex communications error • FAL error • PLC Setup error • I/O verification error • Basic I/O Unit error • CPU Bus Unit error • Special I/O Unit error • Battery error • CPU Bus Unit setting error • Special I/O Unit setting error • Non-fatal Inner Board error (Single CPU Systems or Process-control CPU Units only)	Operation continues, in Duplex Mode without changing the active CPU Unit.		Operation continues.
CPU standby (See note.)	• Waiting for standby CPU Unit at startup • Duplex bus error at startup • Duplex verification error at startup • Waiting for Special I/O Unit • Waiting for CPU Bus Unit • Waiting for Inner Board (Single CPU Systems or Process-control CPU Units only)	Waiting for operation	Waiting for operation	Waiting for operation
Expansion Rack power interruption		Waiting for operation	Waiting for operation	Waiting for operation
DIP Switch Settings Error		Operation not possible	Operation not possible	Operation not possible

Note The cause of the CPU Unit remaining on standby is stored in A322.

10-2-2 Error Information

There are basically five sources of information on errors that have occurred:

- The indicators on the CPU Units
- The indicators on the Duplex Unit (Duplex CPU Systems only)
- The Auxiliary Area Error Flags
- The Auxiliary Area Error Information Flag and Words
- The Auxiliary Area Error Code Word



Note When two or more errors occur at the same time, the highest (most serious) error code will be stored in A400.

Indicator Status and Error Classifications for Duplex CPU Systems

Simplex Mode / Duplex Mode		Fatal errors			Non-fatal errors					Duplex initialization	CPU standby	DIP switch settings error
		Operation switched and operation continues		Operation stops	Operation continues							
Indicator (See note 1.)		CPU error	Fatal error causing operation to switch	Fatal error	Duplex bus or verification error	Non-fatal error	Communications error		Outputs turned OFF			
							Peripheral port	RS-232C port				
CPU Unit	RUN	Not lit	Not lit	Not lit	Lit	Lit	Lit	Lit	Lit	---	Not lit	Flashing
	ERR/ALM	Lit	Lit	Lit	Flashing	Flashing	---	---	---	---	Not lit	---
	INH	Not lit	---	---	---	---	---	---	Lit	---	---	---
	PRPHL	---	---	---	---	---	Not lit	---	---	---	---	---
	COMM	---	---	---	---	---	---	Not lit	---	---	---	---
Duplex Unit	DPL STATUS	Not lit	Not lit	Not lit (See note 3.)	Lit or flashing red	---	---	---	---	Flashing green	---	---
	ACTIVE	Not lit	Not lit (See note 2.)	---	Lit	---	---	---	---	---	---	---
	CPU STATUS	Lit red	Flashing red	Not lit (See note 3.)	---	---	---	---	---	Flashing green	Flashing green	---

Note
1. The status of the indicators are given in RUN or MONITOR mode. "---" indicates that the indicator may be any status.
2. The ACTIVE indicator on the new active CPU Unit will light.
3. The indicator will flash green for any fatal errors except an I/O bus error.

Indicator Status and Error Classifications for Single CPU Systems

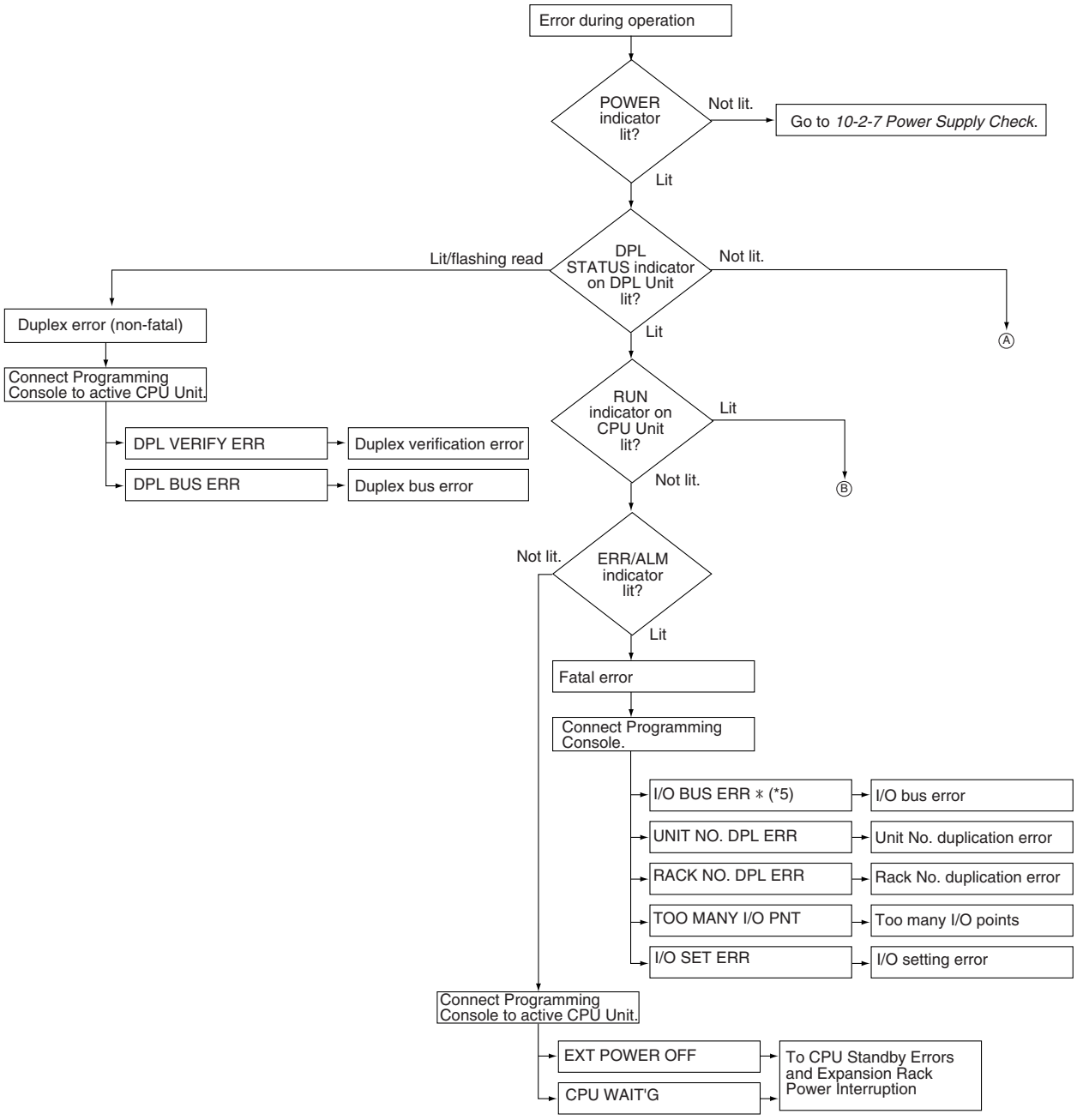
Indicator*	CPU error	CPU standby	Fatal error	Non-fatal error	Communications error		Output OFF Bit ON
					Peripheral	RS-232C	
RUN	OFF	OFF	OFF	ON	ON	ON	ON
ERR/ALM	ON	OFF	ON	Flashing	---	---	---
INH	OFF	---	---	---	---	---	ON
PRPHL	---	---	---	---	OFF	---	---
COMM	---	---	---	---	---	OFF	---

Note The status of the indicators are given in RUN or MONITOR mode. "---" indicates that the indicator may be any status.

10-2-3 Troubleshooting Flowcharts

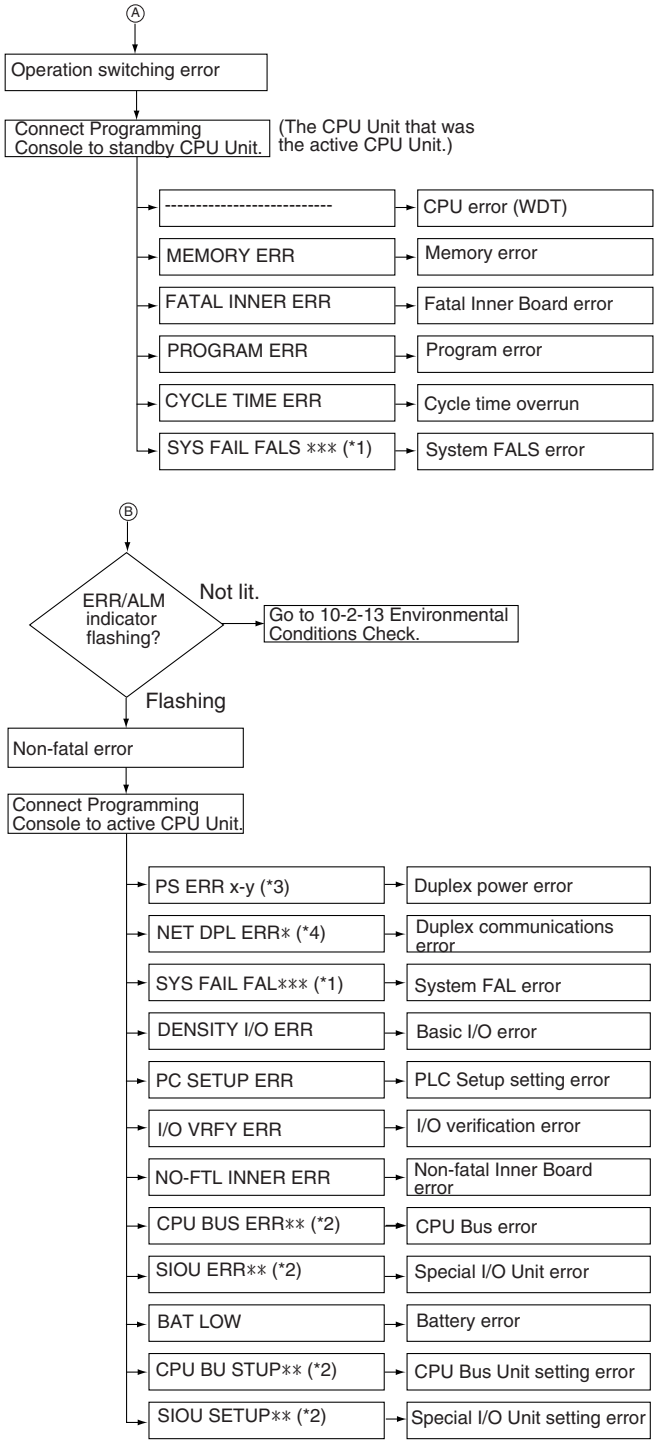
The following flowchart shows troubleshooting using a Programming Console. Determine the error according to the mode and take appropriate measures.

Duplex CPU Systems in Duplex Mode



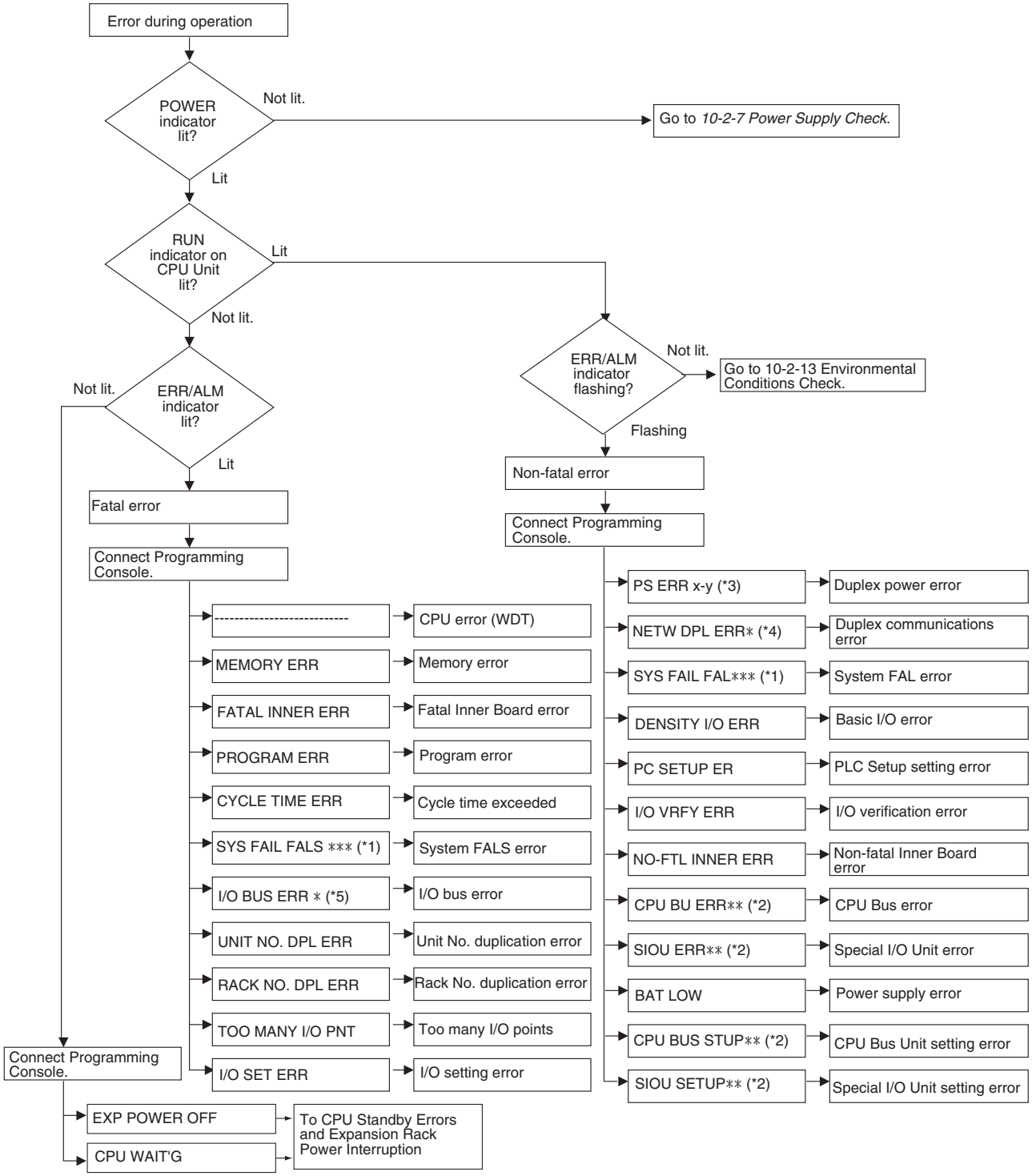
Note *1: ∗∗∗ indicates the FAL or FALS number.
*2: ∗∗ indicates the unit number.
*3: In x-y, x indicates the rack number and y indicates left or right.
*4: ∗ indicates the unit number.
*5: ∗ indicates the rack number.

Duplex Mode, Continued



Note *1: ∗∗∗ indicates the FAL or FALS number.
*2: ∗∗ indicates the unit number.
*3: In x-y, x indicates the rack number and y indicates left or right.
*4: ∗ indicates the unit number.
*5: ∗ indicates the rack number.

Duplex CPU Systems in Simplex Mode or Single CPU Systems



Note *1: ∗∗∗ indicates the FAL or FALS number.
*2: ∗∗ indicates the unit number.
*3: In x-y, x indicates the rack number and y indicates left or right.
*4: ∗ indicates the unit number.
*5: ∗ indicates the rack number.

10-2-4 Errors and Troubleshooting

The following tables show error messages for errors which can occur in CS1D PLCs and indicate the likely cause of the errors.

CPU Standby Errors and Expansion Rack Power Interruptions

When the following indicator status appears during operation in RUN or MONITOR Mode, a CPU standby error or Expansion Rack power interruption has occurred and the CX-Programmer display will indicate one of these errors.

Power Supply Unit	POWER		Lit green
CPU Unit	RUN		Not lit
	ERR/ALM		Not lit
	INH		---
	PRPHL		---
	COMM		---
Duplex Unit (with error occurring on active CPU Unit) (Duplex CPU Systems)	DPL STATUS		---
	Active CPU Unit indicators	ACTIVE	Lit green
		CPU STATUS	Flashing green
	Standby CPU Unit indicators	ACTIVE	Not lit
		CPU STATUS	Flashing green

For all of the following errors, operation will stop if the error occurs with a Single CPU Systems, or in either Duplex Mode or Simplex Mode with a Duplex CPU System.

Error	Programming Console display	Error flags in Auxiliary Area	Error code (in A400)	Flags and word data	Probable cause	Possible remedy
CPU standby error	CPU WAIT'G	None	None	A32203	A CPU Bus Unit has not started properly.	Check the settings of the CPU Bus Unit.
					A Special I/O Unit was not recognized.	Check the settings of the Special I/O Unit.
				A32207	Inner Board was not recognized.	Check the settings of the Inner Board.
				A32205	Duplex verification error.	Press the initialization switch on the Duplex Unit. If the problem persists, check the DIP switch setting. If the problem persists, check the model number of the CPU Units and the Inner Units to see if they are the same.
				A32204	Duplex bus error.	Press the initialization switch on the Duplex Unit. If the problem persists, replace the Duplex Unit.
				A32206	Waiting for other CPU unit.	Check the settings of the standby CPU Unit.
Expansion Rack power interruption	EXT POWER OFF	None	None	A32208	Power is not being supplied to an Expansion Rack.	Supply power to the Expansion Rack. With the CS1D, the Programming Console can be used in this condition.

Note When power supply is interrupted to an Expansion Rack, the CPU Unit will stop program operation. If power is then restored to the Expansion Rack, the CPU Unit will perform startup processing, i.e., the same operational status as existed before the power interrupt will not necessarily be continued.

Operation Switching Errors (Operation Stops in Simplex Mode or for Single CPU Systems)

In a Duplex CPU System, the standby CPU Unit will become the active CPU Unit and continue operation (assuming the standby CPU Unit is normal) in RUN or MONITOR mode and in Simplex Mode whenever an error causing operation to switch occurs. If, however, the same error occurs in the CPU Unit that was the standby or another error that would cause operation to switch occurs, system operation will stop.

In Simplex Mode or will a Single CPU System, all of these errors are fatal and will cause operation to stop.

Connect the CX-Programmer or a Programming Console to display the error message (in the PLC Error Window on the CX-Programmer). The cause of the error can be determined from the error message and related Auxiliary Area flags and words.

An error causing operation to switch (or a fatal error in Simplex Mode) has occurred if the indicators have the following conditions during operation in RUN or MONITOR mode.

Power Supply Unit	POWER		Lit green
CPU Unit With a Duplex CPU System, the CPU Unit that was active when the error occurred	RUN		Not lit
	ERR/ALM		Lit red
	INH		---
	PRPHL		---
	COMM		---
Duplex Unit (Duplex CPU System only)	DPL STATUS		Not lit
	Active CPU Unit indicators	ACTIVE	Not lit
		CPU STATUS	CPU error: Lit red Other: Flashing red
	Standby CPU Unit indicators	ACTIVE	Lit green
		CPU STATUS	Lit green

The standby CPU Unit in a Duplex CPU System will have the following indicator status when an error causing operation to switch occurs.

Power Supply Unit	POWER		Lit green
CPU Unit that was on standby when the error occurred	RUN		Not lit
	ERR/ALM		Lit red
	INH		---
	PRPHL		---
	COMM		---
Duplex Unit	DPL STATUS		Not lit
	Active CPU Unit indicators	ACTIVE	Lit green
		CPU STATUS	Lit green
	Standby CPU Unit indicators	ACTIVE	Not lit
		CPU STATUS	CPU error: Lit red Other: Flashing red

Note With a Duplex CPU System in Simplex Mode or with a Single CPU System, status will be as follows:
I/O memory will be cleared when any error that switches operation occurs except for an error generated by an FALS instruction. I/O memory will not be cleared for a FALS instruction.
If the I/O Memory Hold Bit is ON, I/O memory will be held, but outputs to all Output Units will be turned OFF.

Troubleshooting Table

For all of the following errors, operation will be switched to the standby and operation will continue in a Duplex CPU System in Duplex Mode. If the error occurs in a Single CPU System or in a Duplex CPU System in Simplex Mode, operation will stop.

Error	Programming Console display	Error flags in Auxiliary Area	Error code (in A400)	Flags and word data	Probable cause	Possible remedy
CPU error	———	None	None	None	Watchdog timer has exceeded maximum setting.	Use one of the following methods. • Toggle the USE/NO USE switch for the CPU Unit with the error to NO USE and back to USE and then press the initialization button. • If the automatic recovery setting has been enabled in the PLC Setup, use the automatic recovery function to restart. • If operation still cannot be recovered, replace the CPU Unit.
Memory error	MEMORY ERR	A40115: Memory Error Flag	80F1	A403: Memory Error Location	An error has occurred in memory. A bit in A403 will turn ON to show the location of the error as listed below.	See below for specific bits.
					A40300 ON: A checksum error has occurred in the user program memory.	Use one of the following methods If operation has switched from Duplex to Simplex Mode: • Toggle the USE/NO USE switch for the CPU Unit with the error to NO USE and back to USE and then press the initialization button. • If the automatic recovery setting has been enabled in the PLC Setup, use the automatic recovery function to restart. • If operation still cannot be recovered, replace the CPU Unit. If the error occurs in Simplex Mode: • Retransfer the program and parameters. • If operation still cannot be recovered, replace the CPU Unit.
					A40304 ON: A checksum error has occurred in the PLC Setup.	
					A40305 ON: A checksum error has occurred in the registered I/O table.	
					A40307 ON: A checksum error has occurred in the routing tables.	
					A40308 ON: A checksum error has occurred in the CS-series CPU Bus Unit setup.	
					A40309 ON: An error occurred during automatic transfer from the Memory Card at startup.	Make sure that the Memory Card is installed properly and that the correct file is on the Card.
					A40310 ON: Flash memory has failed.	A hardware error has occurred in the CPU Unit. Replace the CPU Unit.
					A40315 ON: Duplex CPU compatible setting is changed without executing Memory All Clear.	• If a DIP switch has been changed by mistake, reset the settings to the original settings, and then restart the Unit. • To change to a different model by using Duplex CPU compatible setting, perform Memory All Clear.
Fatal Inner Board error	FATAL INNER ERR	A40112: Fatal Inner Board Error Flag	82F0	A424: Inner Board Error Information	The Inner Board is faulty. An error occurred on the Inner bus.	Check the indicators on the Inner Boards and refer to the operation manual for the Inner Board.

Error	Programming Console display	Error flags in Auxiliary Area	Error code (in A400)	Flags and word data	Probable cause	Possible remedy
Program error	PROGRAM ERR	A40109: Program Error Flag	80F0	A294 to A299: Program error information	The program is incorrect. See the following rows of this table for details. The address at which the program stopped will be stored in A298 and A299. The task where the program stopped will be stored in A294.	If the error has occurred in both the active and standby CPU Units, use the information in A294, A298, and A299 to find the location and cause of the error, check the program, and correct the error. Then, clear the error. If the error occurred in only one of the CPU Units, use one of the following methods. • Toggle the USE/NO USE switch for the CPU Unit with the error to NO USE and back to USE and then press the initialization button. • If the automatic recovery setting has been enabled in the PLC Setup, use the automatic recovery function to restart. • If operation still cannot be recovered, replace the CPU Unit.
					A29511: No END error	If the error has occurred in both the active and standby CPU Units, place END(001) at the end of the task indicated in A294.
					A29512: Task error A task error has occurred. The following conditions will generate a task error. 1. There isn't an executable cyclic task. 2. There isn't a program allocated to the task. Check A294 for the number of the task missing a program. 3. The task specified in a TKON(820), TKOF(821), or MSKS(690) instruction doesn't exist.	• If the error has occurred in both the active and standby CPU Units, check the startup cyclic task attributes. • Check the execution status of each task as controlled by TKON(820) and TKOF(821). • Make sure that all of the task numbers specified in TKON(820), TKOF(821), and MSKS(690) instructions have corresponding tasks. • If the power OFF interrupt task is enabled in the PLC setup, make sure a power OFF interrupt task has been created.
					A29510: Illegal access error An illegal access error has occurred and the PLC Setup has been set to stop operation for an instruction error. The following are illegal access errors: 1. Reading/writing a parameter area. 2. Writing memory that is not installed. 3. Writing an EM bank that is EM file memory. 4. Writing to a read-only area. 5. Indirect DM/EM address that is not in BCD when BCD mode is specified.	If the error has occurred in both the active and standby CPU Units, find the program address where the error occurred (A298/A299) and correct the instruction.
					A29509: Indirect DM/EM BCD error An indirect DM/EM BCD error has occurred and the PLC Setup has been set to stop operation for an instruction error.	If the error has occurred in both the active and standby CPU Units, find the program address where the error occurred (A298/A299) and correct the indirect addressing or change to binary mode.
					A29508: Instruction error An instruction processing error has occurred and the PLC Setup has been set to stop operation for an instruction error.	If the error has occurred in both the active and standby CPU Units, find the program address where the error occurred (A298/A299) and correct the instruction. Alternatively, set the PLC Setup to continue operation for an instruction error.
					A29513: Differentiation overflow error Too many differentiated instructions have been inserted or deleted during online editing.	If the error has occurred in both the active and standby CPU Units, write any changes to the program, switch to PROGRAM mode and then return to MONITOR mode to continue editing the program.

Error	Programming Console display	Error flags in Auxiliary Area	Error code (in A400)	Flags and word data	Probable cause	Possible remedy
Program error	PROGRAM ERR	A40109: Program Error Flag	80F0	A294 to A299: Program error information	A29514: Illegal instruction error The program contains an instruction that cannot be executed.	If the error has occurred in both the active and standby CPU Units, retransfer the program to the CPU Unit.
					A29515: UM overflow error The last address in UM (user program memory) has been exceeded.	If the error has occurred in both the active and standby CPU Units, use a Programming Device to transfer the program again.
Cycle Time Overrun error	CYCLE TIME ERR	A40108: Cycle Time Overrun Flag	809F	---	The cycle time has exceeded the maximum cycle time (watch cycle time) set in the PLC Setup.	If the error has occurred in both the active and standby CPU Units, change the program to reduce the cycle time or change the maximum cycle time setting. The cycle time can be reduced by dividing unused parts of the program into tasks, jumping unused instructions in tasks, and disabling cyclic refreshing of Special I/O Units that don't require frequent refreshing. If the error occurred in only one of the CPU Units, use one of the following methods. • Toggle the USE/NO USE switch for the CPU Unit with the error to NO USE and back to USE and then press the initialization button. • If the automatic recovery setting has been enabled in the PLC Setup, use the automatic recovery function to restart. • If operation still cannot be recovered, replace the CPU Unit.
System FALS error	SYS FAIL FALS	A40106: FALS Error Flag	C101 to C2FF	---	FALS(007) has been executed in the program. The error code in A400 will indicate the FAL number. The leftmost digit of the code will be C and the rightmost 3 digits of the code will be from 100 to 2FF hex and will correspond to FAL numbers 001 to 511.	If the error has occurred in both the active and standby CPU Units, correct according to cause indicated by the FAL number (set by user). If the error occurred in only one of the CPU Units, use one of the following methods. • Toggle the USE/NO USE switch for the CPU Unit with the error to NO USE and back to USE and then press the initialization button. • If the automatic recovery setting has been enabled in the PLC Setup, use the automatic recovery function to restart. • If operation still cannot be recovered, replace the CPU Unit.

Fatal Errors

For the following errors, operation will stop for a Duplex CPU System in Duplex Mode or in Simplex Mode, or for a Single CPU System.

Connect the CX-Programmer or a Programming Console to display the error message (in the PLC Error Window on the CX-Programmer). The cause of the error can be determined from the error message and related Auxiliary Area flags and words.

A fatal error has occurred if the indicators have the following conditions during operation in RUN or MONITOR mode.

Power Supply Unit	POWER		Lit green
CPU Unit	RUN		Not lit
	ERR/ALM		Lit red
	INH		---
	PRPHL		---
	COMM		---
Duplex Unit (with error occurring on active CPU Unit)	DPL STATUS		Lit green
	Active CPU Unit indicators	ACTIVE	Lit green
		CPU STATUS	Not lit
	Standby CPU Unit indicators	ACTIVE	Not lit
		CPU STATUS	Not lit

Note

1. I/O memory will be cleared when a fatal error occurs.
2. If the I/O Hold Bit is ON, I/O memory will not be cleared, but all outputs from Output Units will be turned OFF.

Troubleshooting Table

For the following errors, operation will stop for a Duplex CPU System in Duplex Mode or in Simplex Mode, or for a Single CPU System.

Error	Programming Console display	Error flags in Auxiliary Area	Error code (in A400)	Flags and word data	Probable cause	Possible remedy
I/O Bus error	I/O BUS ERR ✳	A40114: I/O Bus Error Flag	80C0 to 80C7, or 80CF	A404: I/O Bus Error Slot and Rack Numbers	Error has occurred in the bus line between the CPU and I/O Units. A40400 to A40407 contain the error slot number (00 to 09) in binary. 0F indicates that the slot cannot be determined. A40408 to A40415 contain the error rack number (00 to 07) in binary. 0F indicates that the rack cannot be determined.	Try turning the power OFF and ON again. If the error isn't corrected, turn the power OFF and check cable connections between the I/O Units and Racks. Check for damage to the cable or Units. Correct the cause of the error and then turn the Rack's power supply OFF and then ON again.
	I/O BUS ERR B or I/O BUS ERR C	A40114: I/O Bus Error Flag	80CC, 80CB	A404: I/O Bus Error Slot and Rack Numbers	I/O bus error B: The CPU Units are not mounted to a Duplex CPU Backplane. I/O bus error C: The cable to an Expansion Rack is wired incorrectly. A40400 to A40407: 0F hex A40408 to A40415: 0B hex: I/O bus error B 0C hex: I/O bus error C	Turn OFF the power supply and replace the Backplane with a CS1D-B□□□□ Backplane. Correct the cable connections.
Unit/Rack Number Duplication error	UNIT NO. DPL ERR	A40113: Duplication Error Flag	80E9	A410: CPU Bus Unit Duplicate Number Flags	The same number has been allocated to more than one CPU Bus Unit. Bits A41000 to A41015 correspond to unit numbers 0 to F.	Check the unit numbers, eliminate the duplications, and turn the Rack's power supply OFF and then ON again.
				A411 to A416: Special I/O Unit Duplicate Number Flags	The same number has been allocated to more than one Special I/O Unit. Bits A41100 to A41615 correspond to unit numbers 0 to 95.	Check the unit numbers, eliminate the duplications, and turn the Rack's power supply OFF and then ON again.
	RACK NO. DPL ERR		80EA	A409: Expansion Rack Duplicate Rack Number	The same I/O word has been allocated to more than one Basic I/O Unit.	Check allocations to Units on the rack number whose bit in ON in A40900 to A40907. Correct the allocations so that no words are allocated more than once, including to Units on other Racks, and turn the Rack's power supply OFF and then ON again.
					An Expansion I/O Rack's starting word address exceeds CIO 0901. The corresponding bit in A40900 to A40907 (Racks 0 to 7) will be turned ON.	Check the first word setting for the Rack indicated in A40900 to A40907 and change the setting to a valid word address below CIO 0901 with a Programming Device.
Too Many I/O Points error	TOO MANY I/O PNT	A40111: Too Many I/O Points Flag	80E1	A407: Too Many I/O Points, Details	The probable causes are listed below. The 3-digit binary value (000 to 101) in A40713 to A40715 indicates the cause of the error. The value of these 3 bits is also output to A40700 to A40712. 1. The total number of I/O points set in the I/O tables exceeds the maximum allowed for the CPU Unit (bits: 000). 2. The number of Expansion Racks exceeds the maximum (bits: 101).	Correct the problem indicated by the content of A407 and turn the power OFF and ON again.
I/O Table Setting error	I/O SET ERR	A40110: I/O Setting Error Flag	80E0	---	Input and output word allocations do no agree with input/output words required by Units actually mounted.	Check the I/O table with I/O Table Verification operation. When the system has been corrected, register the I/O table again.

Non-fatal Errors

Operation will continue for any of the following errors for a Duplex CPU System in Duplex Mode or in Simplex Mode, or for a Single CPU System. For some of these errors, operation for a Duplex CPU System will switch from Duplex Mode to Simplex Mode and for other errors, operation will remain in Duplex Mode. These are listed separately below.

Connect the CX-Programmer or a Programming Console to display the error message (in the PLC Error Window on the CX-Programmer). The cause of the error can be determined from the error message and related Auxiliary Area flags and words.

Duplex Errors (Errors Causing a Switch to Simplex Operation for Duplex CPU Systems)

For a Duplex CPU System, duplex errors will cause operation to be switched to Simplex Mode, but operation will continue in RUN or MONITOR mode.

A non-fatal duplex error has occurred if the indicators have the following conditions during operation in RUN or MONITOR mode.

Duplex errors are unique to Duplex CPU Systems and will not occur on Single CPU Systems.

Power Supply Unit	POWER		Lit green
CPU Unit	RUN		Lit green
	ERR/ALM		Flashing red
	INH		---
	PRPHL		---
	COMM		---
Duplex Unit (with error occurring on active CPU Unit)	DPL STATUS		Duplex verification error: Flashing red Duplex bus error: Lit red
	Active CPU Unit indicators	ACTIVE	Lit green
		CPU STATUS	Lit green
	Standby CPU Unit indicators	ACTIVE	Not lit
		CPU STATUS	Lit green

Troubleshooting Table

For all of the following errors, operation will continue if the error occurs in Duplex Mode or in Simplex Mode. If it occurs in Duplex Mode, operation will switch to Simplex Mode.

Error	Programming Console display	DPL STATUS indicator	Error flags in Auxiliary Area	Error code (in A400)	Flags and word data	Probable cause	Possible remedy
Duplex verification error	DPL VERIFY ERR	Flashing red	A31600, A40214	0011	A317	One of the following is not the same between the two CPU Units. • CPU Unit model number • Parameter area data • User program • Inner Board internal data inconsistency • CPU Unit version verification error	Check the items to the left between the two CPU Units and be sure they are the same and then toggle the power supply. If the error still occurs after the Initial Switch is pressed, transfer the user program and Parameter Area (i.e., PLC Setup, CPU Bus Unit Setup, and I/O tables) again to the active CPU Unit. If the problem persists, replace the Duplex Unit.
Duplex bus error	DPL BUS ERR	Lit red	A31601, A40214	0010	---	An error occurred on the duplex bus in the Duplex System.	Prepare the system to stop operation and then press the initialization button on the Duplex Unit. If the problem persists, replace the Duplex Unit.

Errors for which Duplex Mode Continues

If any of the following errors occurs for a Duplex CPU System in Duplex Mode, operation will continue in Duplex Mode and in RUN or MONITOR mode. Operation will also continue if any of these errors occurs in Simplex Mode or in a Single CPU System.

A non-fatal error has occurred if the indicators have the following conditions during operation in RUN or MONITOR mode.

Power Supply Unit	POWER		Lit green
CPU Unit	RUN		Lit green
	ERR/ALM		Flashing red
	INH		----
	PRPHL		----
	COMM		----
Duplex Unit (with error occurring on active CPU Unit)	DPL STATUS		Lit green
	Active CPU Unit indicators	ACTIVE	Lit green
		CPU STATUS	Lit green
	Standby CPU Unit indicators	ACTIVE	Not lit
		CPU STATUS	Lit green

Troubleshooting Table

For all of the following errors, operation will continue if the error occurs for a Duplex CPU System in Duplex Mode or in Simplex Mode, or for a Single CPU System. If it occurs in Duplex Mode, operation will continue in Duplex Mode.

Error	Programming Console display	Error flags in Auxiliary Area	Error code (in A400)	Flags and word data	Probable cause	Possible remedy
Duplex power supply error	PS ERROR x-y x = Rack # y = Slot	A31602, A40214	0003	A319, A320	An error has occurred in one of the Power Supply Units. • The primary-side power supply has been interrupted. • The secondary-side voltage has dropped below 5 V or is an overvoltage.	Use A319 and A320 to identify the Power Supply Unit with an error and either correct the error or, if necessary, replace the Unit.
Duplex communications error	NET DPL ERR ✳ ✳ = Node address	A31603, A40214	0600 to 060F Rightmost digit is unit No.	A434 to A437	An error has occurred for a Communications Unit (Controller Link Unit) with a unit number that was set for duplex operation.	Use A434 and A437 to identify the Communications Unit with an error and either correct the error or, if necessary, replace the Unit.
System FAL error	SYS FAIL FAL	A40215: FAL Error Flag	4101 to 42FF	A360 to A391: Executed FAL Number Flags	FAL(006) has been executed in program. Executed FAL Number Flags A36001 to A39115 correspond to FAL numbers 001 to 511. The error code in A400 will indicate the FAL number. The leftmost digit of the code will be 4 and the rightmost 3 digits of the code will be from 100 to 2FF hex and will correspond to FAL numbers 001 to 511.	Correct according to cause indicated by FAL number (set by user).
PLC Setup error	PC SETUP ERR	A40210: PLC Setup Error Flag	009B	A406: PLC Setup Error Location	There is a setting error in the PLC Setup. The location (binary offset) of the error is written to A406.	Change the indicated setting to a valid setting.
I/O Table Verification error	I/O VRFY ERR	A40209: I/O Verification Error Flag	00E7	---	A Unit has been added or removed, so the registered I/O tables don't agree with the actual Units in the PLC. The I/O Verification Error Flag goes OFF when the situation is corrected.	Execute the I/O Table Verify operation to find the problem location. Create new I/O tables or replace the Unit to match the registered I/O tables.
Non-fatal Inner Board error	NO-FTL INNER ERR	A40208: Inner Board Error Flag	02F0	A424: Inner Board Error Information	An error occurred in the Duplex Inner Board	Check the Inner Board indicators. Refer to the Duplex Inner Board's operation manual for details.

Error	Programming Console display	Error flags in Auxiliary Area	Error code (in A400)	Flags and word data	Probable cause	Possible remedy
CS-series CPU Bus Unit error	CPU BU ERR	A40207: CS-series CPU Bus Unit Error Flag	0200 to 020F	A417: CS-series CPU Bus Unit Error, Unit Number Flags	An error occurred in a data exchange between the CPU Unit and a CS-series CPU Bus Unit. The corresponding flag in A417 is turned ON to indicate the problem Unit. Bits A41700 to A41715 correspond to unit numbers 0 to F.	Check the Unit indicated in A417. Refer to the Unit's operation manual to find and correct the cause of the error. Restart the Unit by toggling its Restart Bit or turn the power OFF and ON again. Replace the Unit if it won't restart.
Special I/O Unit error	SIOU ERR	A40206: Special I/O Unit Error Flag	0300 to 035F, or 03FF	A418 to A423: Special I/O Unit Error, Unit Number Flags	An error occurred in a data exchange between the CPU Unit and a Special I/O Unit. The corresponding flag in A418 to A423 is turned ON to indicate the problem Unit. Bits A41800 to A42315 correspond to unit numbers 0 to 95.	Check the Unit indicated in A418 to A423. Refer to the Unit's operation manual to find and correct the cause of the error. Restart the Unit by toggling its Restart Bit or turn the power OFF and ON again. Replace the Unit if it won't restart.
Basic I/O Unit error	DENSITY I/O ERR	A40212: Basic I/O Unit Error Flag	009A	A408: Basic I/O Unit error, slot number	An error occurred in the data exchange between the CPU Unit and a Basic I/O Unit. **Note:** A408 contains the slot number where the error occurred.	Mount the I/O Unit in the Backplane. If the error is not recurs, replace the I/O Unit.
Battery error	BATT LOW	A40204: Battery Error Flag	00F7	---	This error occurs when the PLC Setup has been set to detect battery errors and the CPU Unit's backup battery is missing or its voltage has dropped.	Check battery and replace if necessary. Change the PLC Setup setting if battery-free operation is being used.
CS-series CPU Bus Unit Setup error	CPU BU STUP	A40203: CS-series CPU Bus Unit Setting Error Flag	0400 to 040F	A427: CS-series CPU Bus Unit Setting Error, Unit Number Flags	An installed CS-series CPU Bus Unit does not match the CS-series CPU Bus Unit registered in the I/O table. The corresponding flag in A427 will be ON. Bits 00 to 15 correspond to unit numbers 0 to F.	Change the registered I/O tables.
Special I/O Unit Setup error	SIOU SETUP	A40202: Special I/O Unit Setting Error Flag	0500 to 055F	A428 to A433: Special I/O Unit Setting Error, Unit Number Flags	An installed Special I/O Unit does not match the Special I/O Unit registered in the I/O table. The corresponding flag in A428 to A433 will be ON. Bits A42800 to A43315 correspond to unit numbers 0 to 95.	
Interrupt task error	INTRPT ERR	A40213: Interrupt Task Error Flag	008B	A426: Interrupt Task Error, Task Number	An attempt was made to refresh I/O for a Special I/O Unit with IORF(097) within an interrupt task while cyclic I/O refresh processing was being performed for the same Special I/O Unit. Detecting interrupt task errors must be enabled in the PLC Setup to detect this error (redundant refreshing).	Review the program and either disable detecting interrupt task errors or prevent redundant refreshing from occurring.

Other Errors

	Error flags in Auxiliary Area	Error code (in A400)	Flags and word data	Error	Probable cause	Possible remedy
Power Supply Unit: POWER: Lit green. CPU Unit: RUN: Lit green.; ERR/ALM: ---; INH: ---; PRPHL: Not lit.; COMM: ---	----	----	----	Peripheral Port Communications Error	A communications error has occurred in communications with the device connected to the peripheral port if the indicators have the status shown at the left.	Check the PRPHL setting on the Duplex Unit or the DIP switch setting on the CPU Unit and the peripheral port settings in the PLC Setup. Also check the cable connections.
Power Supply Unit: POWER: Lit green. CPU Unit: RUN: Lit green.; ERR/ALM: ---; INH: ---; PRPHL: ---; COMM: Not lit.	----	----	----	RS-232C Port Communications Error	A communications error has occurred in communications with the device connected to the RS-232C port if the indicators have the status shown at the left.	Check the COMM setting on the Duplex Unit or the DIP switch setting on the CPU Unit, and also the RS-232C port settings in the PLC Setup. Also check the cable connections. If a host computer is connected, check the communications settings of the serial port on the host computer and the communications program in the host computer.
Power Supply Unit: POWER: Lit green. CPU Unit: RUN: Lit green.; ERR/ALM: ---; INH: ---; PRPHL: ---; COMM: ---	----	----	----	Communications error	The cycle time was long, causing the response monitoring time of the CX-Programmer to be exceeded.	Set a longer response monitoring time on the CX-Programmer. Right-click the PLC on the CX-Programmer and select ***Change***. The Change PLC Dialog Box will be displayed. Click the **Setting** Button for the network type and increase the response monitoring time on the Network Tab Page.
Power Supply Unit: POWER: Lit green. CPU Unit: RUN: Flashing green.; ERR/ALM: ---; INH: ---; PRPHL: ---; COMM: ---				DIP switch settings error	The DIP switch setting of the CPU Unit is incorrect.	Correct the DIP switch setting. (Refer to *2-4-2 Components*)

10-2-5 Error Codes

The following table list error in order of severity, with the most serious error given first. When more than one error occurs at the same time, the most serious error code will be stored in A400.

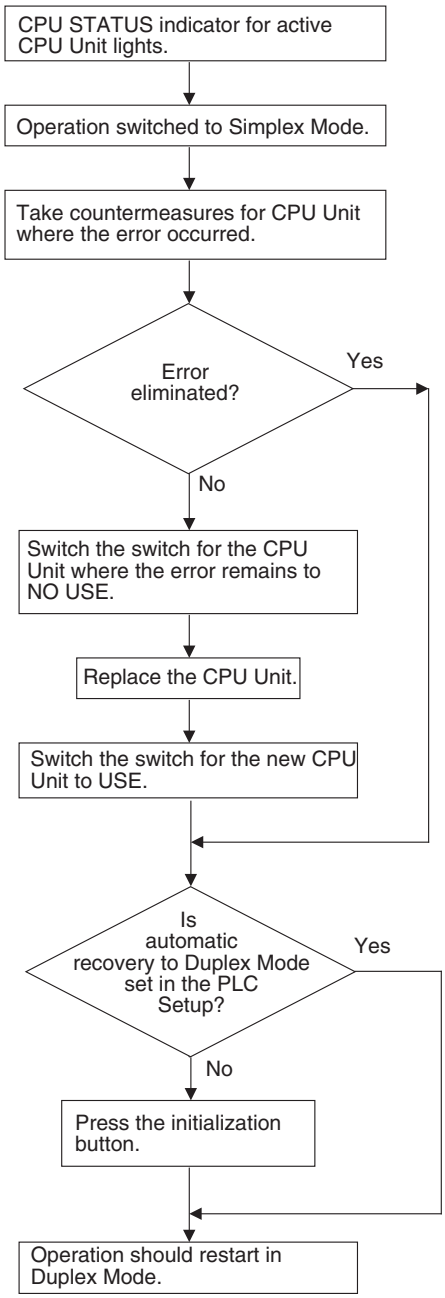
Rank	Error	Programming Console display	Error flag	Code stored in A400
1	Memory error	MEMORY ERR	A40115 Memory Error Flag	80F1
2	I/O bus errors	I/O BUS ERR ∗ (See note 1.)	A40114 I/O Bus Error Flag	80C0 to 80C7, 80CF
		I/O BUS ERR B		80CC
		I/O BUS ERR C		
3	Duplicated number errors	UNIT NO. DPL ERR	A40113 Duplicated Number Flag	80E9
4		RACK NO. DPL ERR		80EA
5	Too many I/O points	TOO MANY I/O PNT	A40111 Too Many I/O Points Flag	80E1

Rank	Error	Programming Console display	Error flag	Code stored in A400
6	I/O setting error	I/O SET ERR	A40110 I/O Setting Error Flag	80E0
7	Program error	PROGRAM ERR	A40109 Program Error Flag	80F0
8	Cycle time overrun error	CYCLE TIME ERR	A40108 Cycle Time Overrun Flag	809F
9	FALS execution	SYS FAIL FALS ∗∗∗ (See note 2.)	A40106 FALS Error Flag	C101 to C2FF
10	Duplex verification error	DPL VERIFY ERR (See note 6.)	A40214, A31600	0011
11	Duplex bus error	DPL BUS ERR (See note 6.)	A40214, A31601	0010
12	Duplex power error	PS ERR x-y (See note 3.)	A40214, A31602	0003
13	Duplex communications error	NET DPL ERR ∗ (See note 4.)	A40214, A31603	0600 to 060F
14	FAL execution	SYS FAIL FAL ∗∗∗ (See note 2.)	A40215 FAL Error Flag	4101 to 42FF
15	Interrupt task error	INTRPT ERR	A40213: Interrupt Task Error Flag	008B
16	Basic I/O Unit error	DENSITY I/O ERR	A40212 Basic I/O Unit Error Flag	009A
17	PLC Setup setting error	PC SETUP ERR	A40210 PLC Setup Setting Error Flag	009B
18	I/O verification error	I/O VRFY ERR	A40209 I/O Verification Error Flag	00E7
19	CPU Bus Unit error	CPU BU ERR ∗∗ (See note 5.)	A40207 CPU Bus Unit Error Flag	0200 to 020F
20	Special I/O Unit error	SIOU ERR ∗∗ (See note 5.)	A40206 Special I/O Unit Error Flag	0300 to 035F, 03FF
21	Battery error	BATT LOW	A40204 Battery Error Flag	00F7
22	CPU Bus Unit setting error	CPU BU STUP ∗∗ (See note 5.)	A40203 CPU Bus Unit Setting Error Flag	0400 to 040F
23	Special I/O Unit setting error	SIOU SETUP ∗∗ (See note 5.)	A40202 Special I/O Unit Setting Error Flag	0500 to 055F

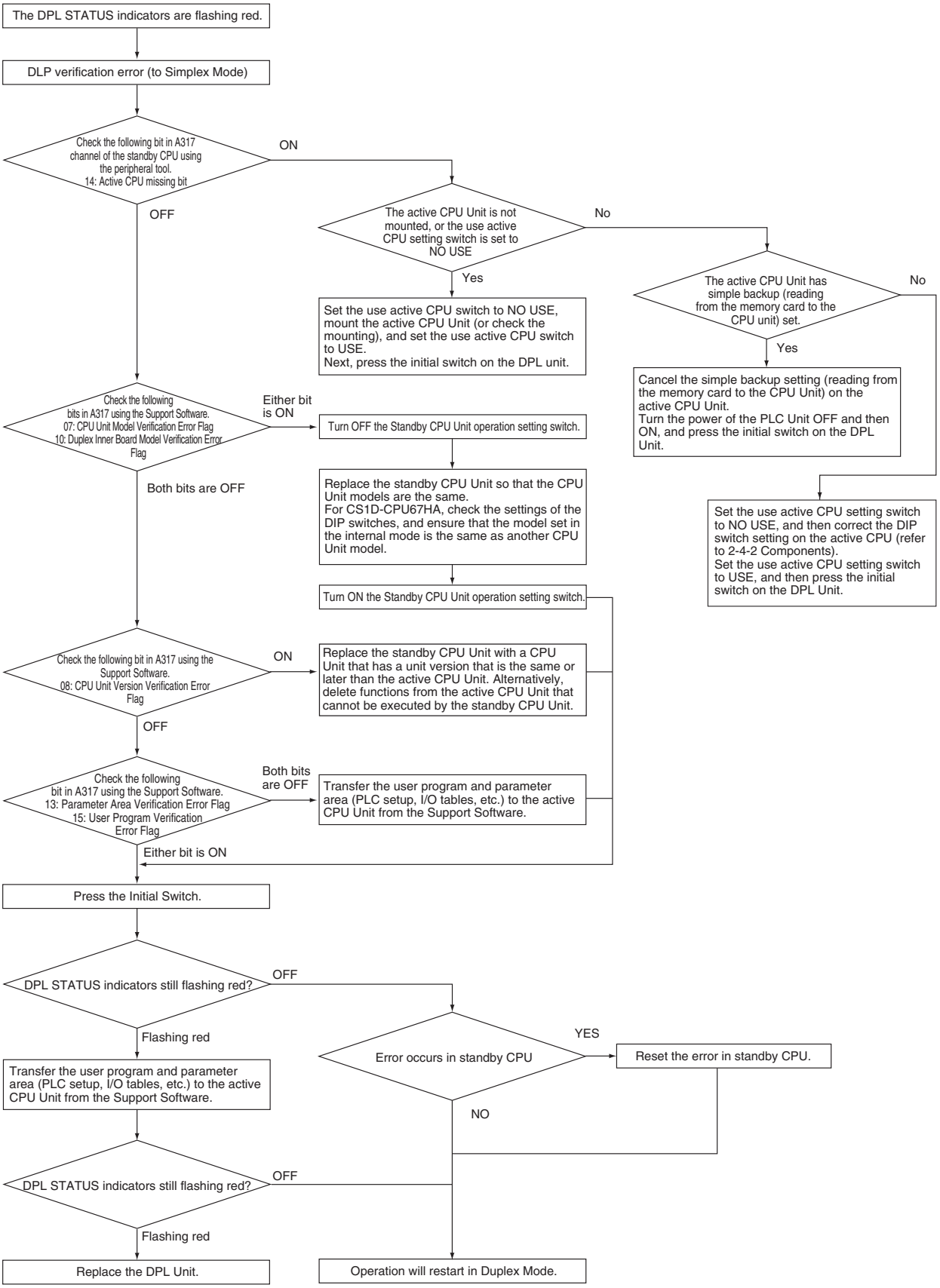
Note
1. ∗ = Rack number
2. ∗∗∗ = FAL or FALS number
3. x-y: x = Rack number, y = L for left or R for right
4. ∗ = Unit number
5. ∗∗ = Unit number
6. These errors occur only for Duplex CPU Systems.

10-2-6 Duplex Check

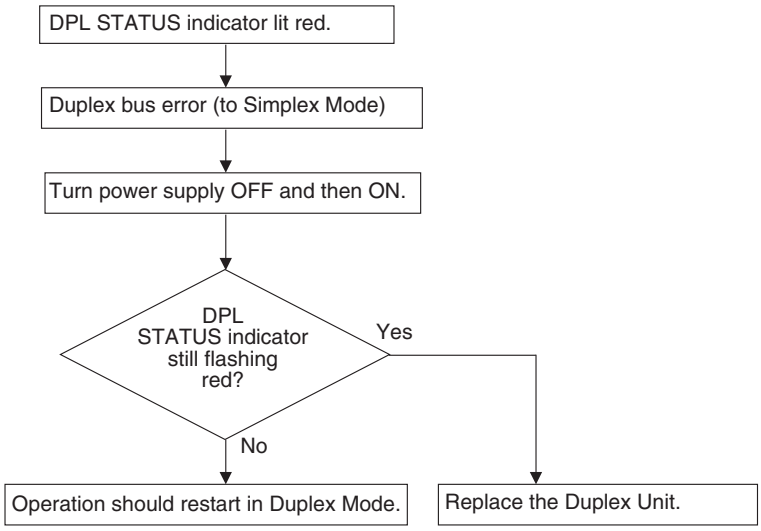
Errors Causing Operation to Switch to Standby CPU Unit (Duplex CPU Systems Only)



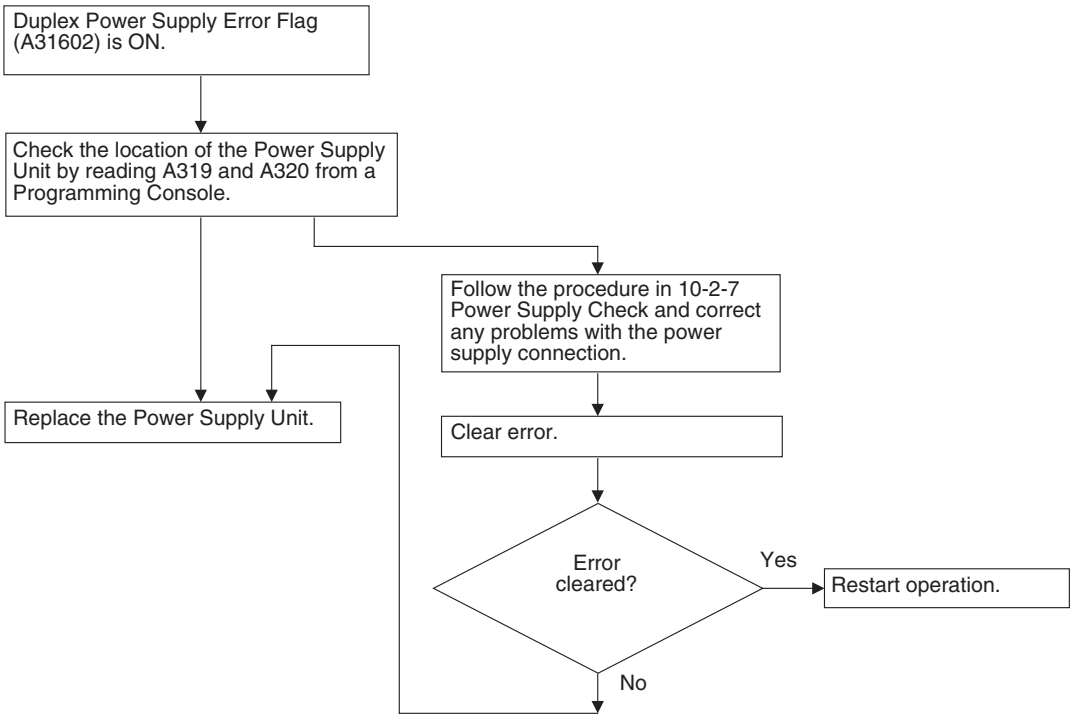
Duplication Verification Errors (Duplex CPU Systems Only)



Duplex Bus Errors (Duplex CPU Systems Only)

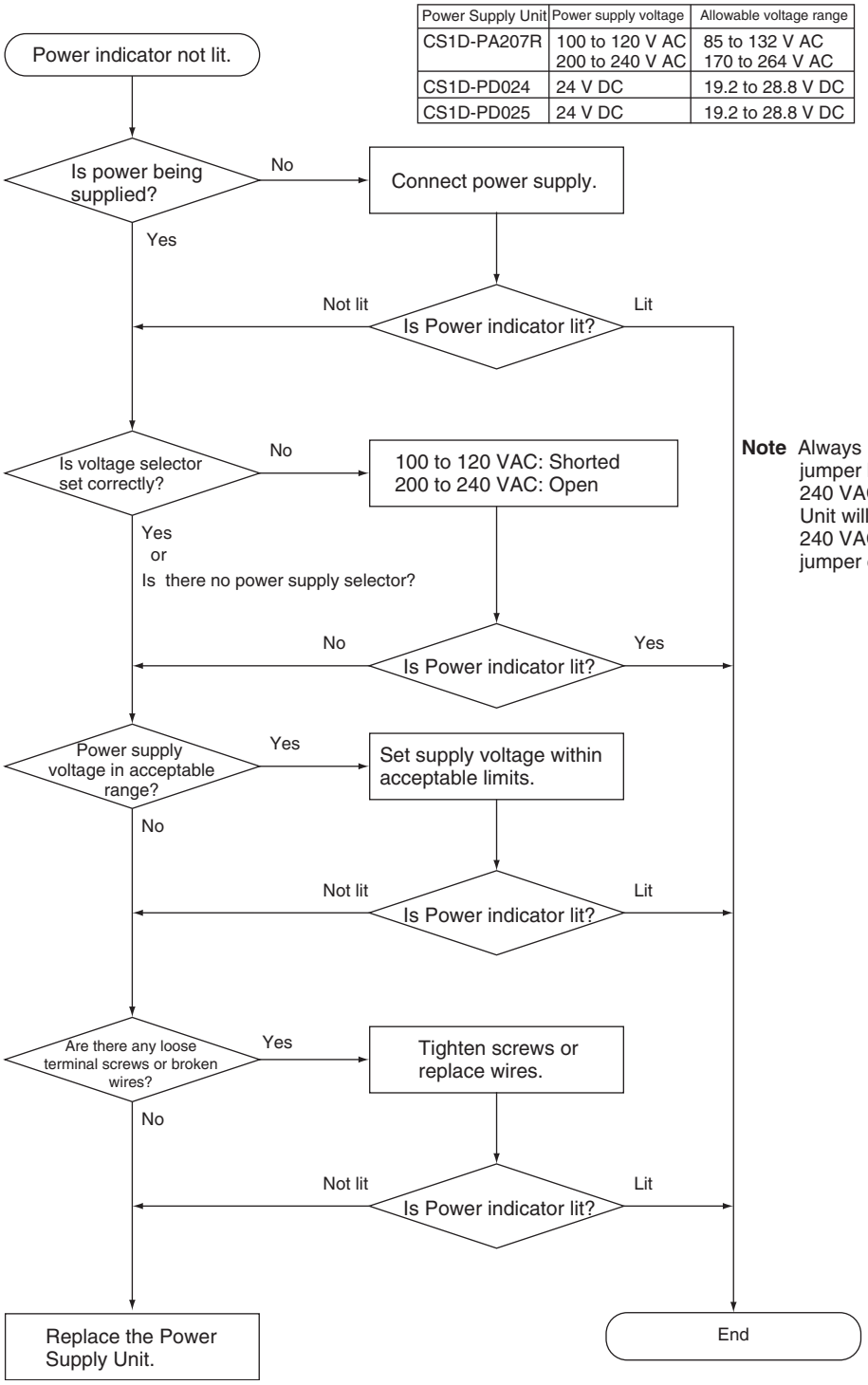


Duplex Power Supply Errors



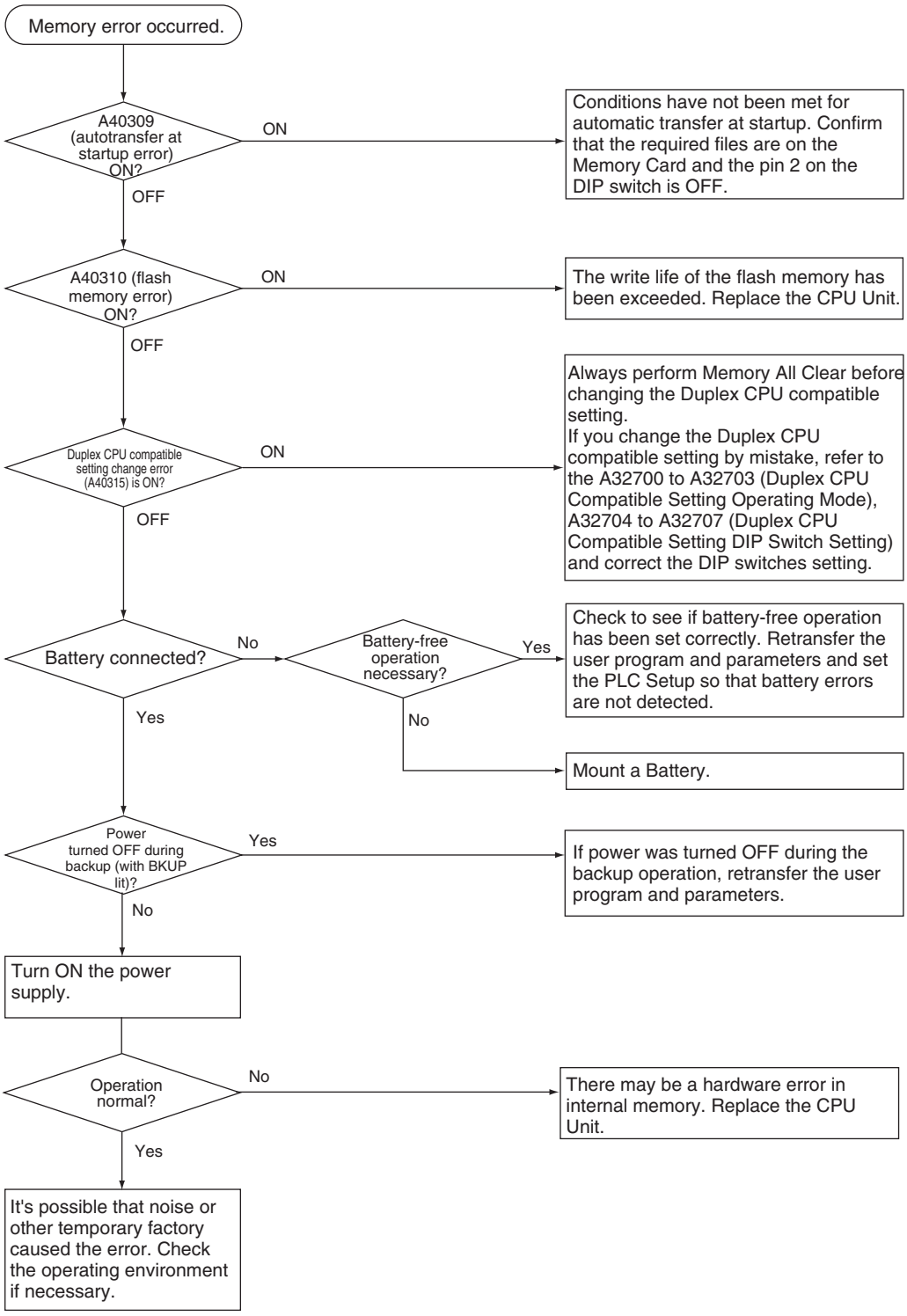
10-2-7 Power Supply Check

Power Supply Unit	Power supply voltage	Allowable voltage range
CS1D-PA207R	100 to 120 V AC 200 to 240 V AC	85 to 132 V AC 170 to 264 V AC
CS1D-PD024	24 V DC	19.2 to 28.8 V DC
CS1D-PD025	24 V DC	19.2 to 28.8 V DC

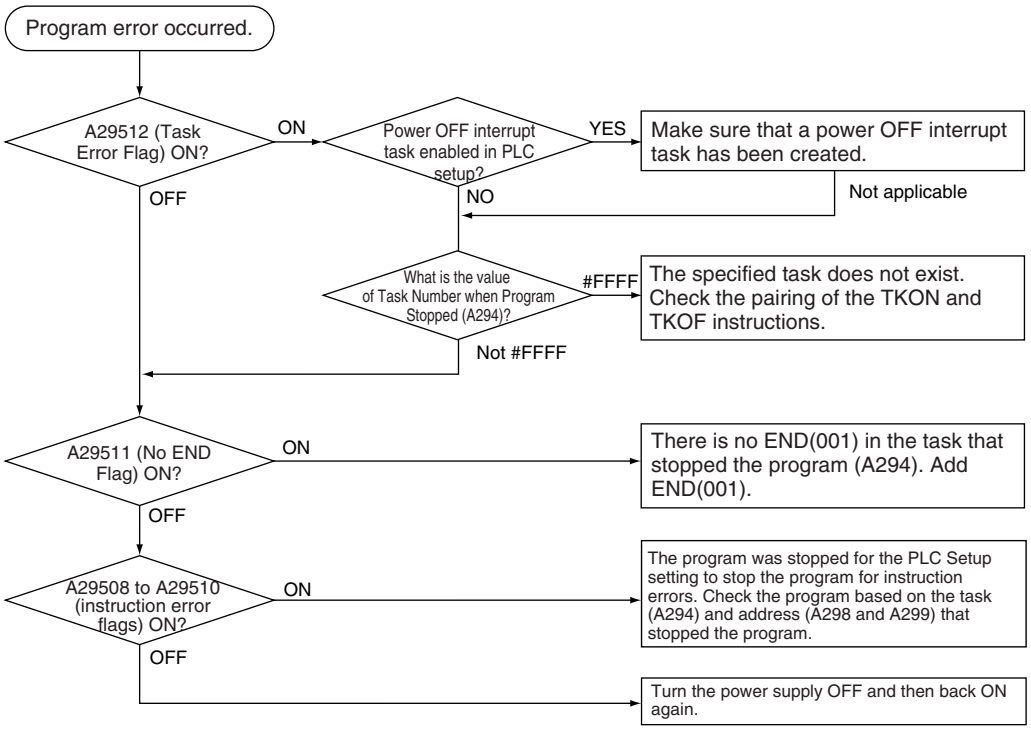


Note Always remove the short jumper before supplying 200 to 240 VAC. The Power Supply Unit will be destroyed if 200 to 240 VAC is supply with the jumper connected.

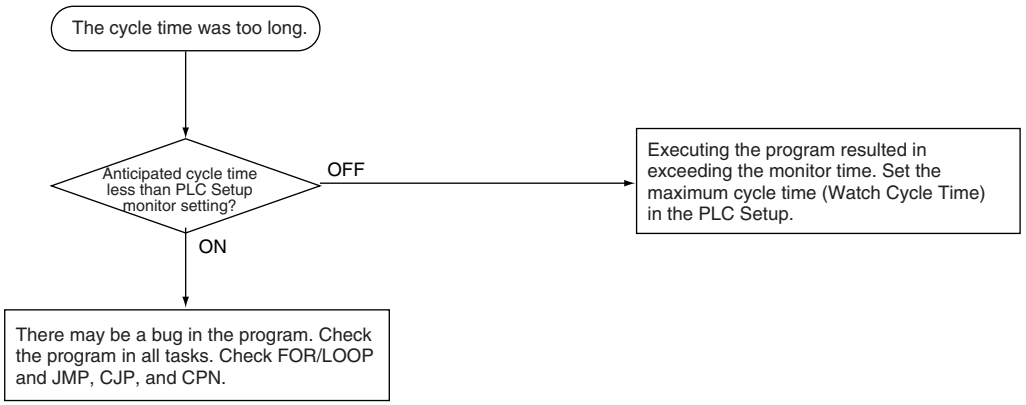
10-2-8 Memory Error Check



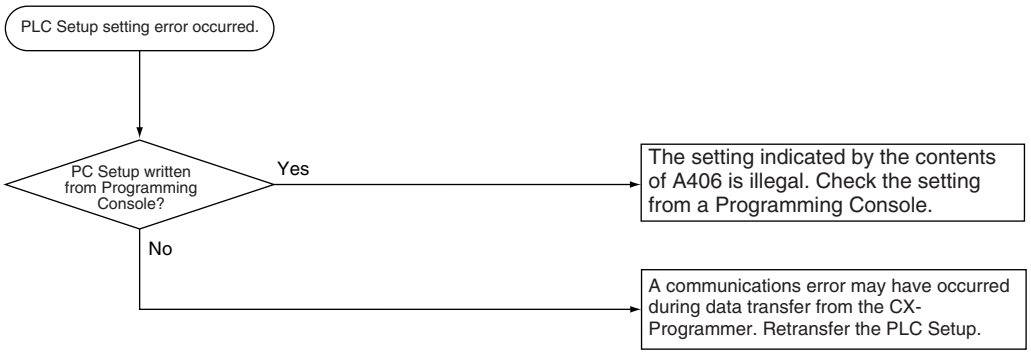
10-2-9 Program Error Check



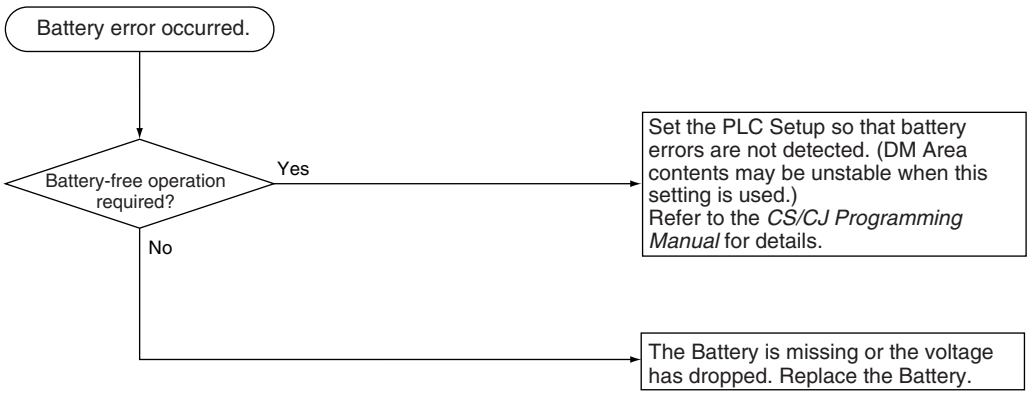
10-2-10 Cycle Time Overrun Error Check



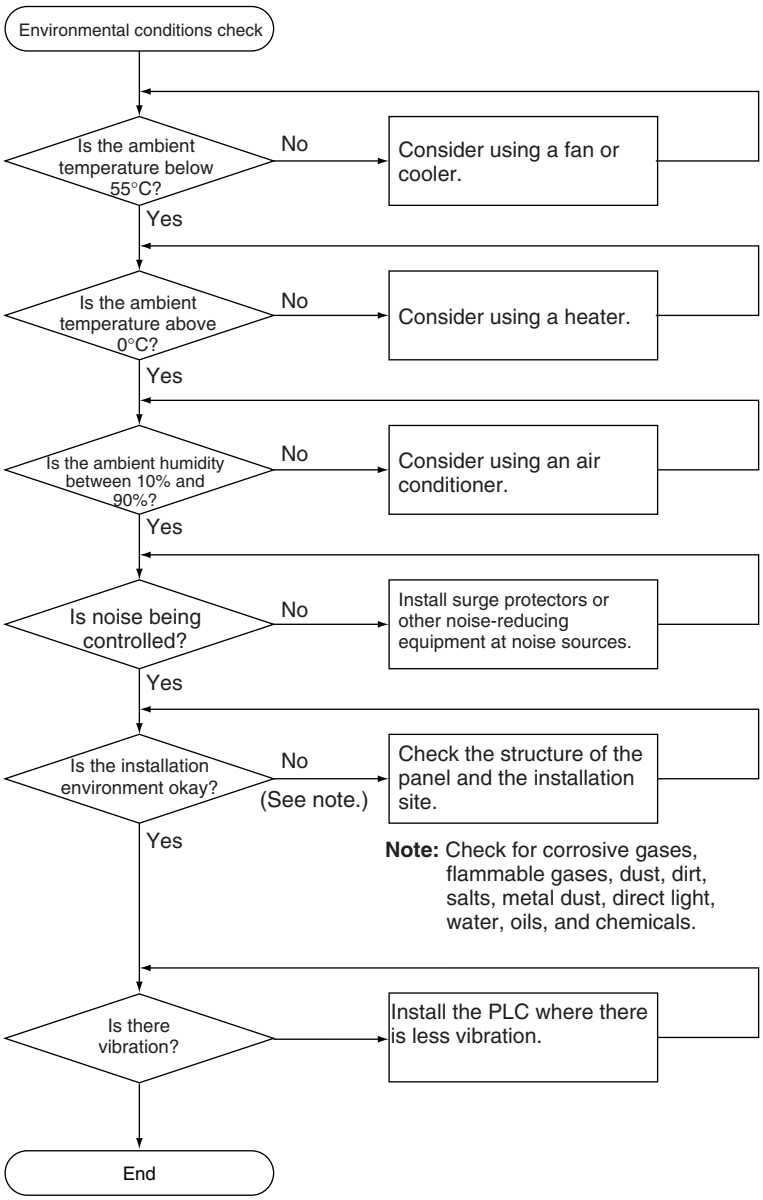
10-2-11 PLC Setup Setting Error Check



10-2-12 Battery Error Check

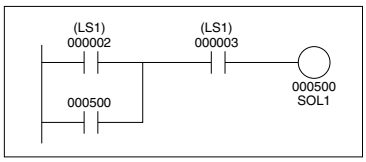


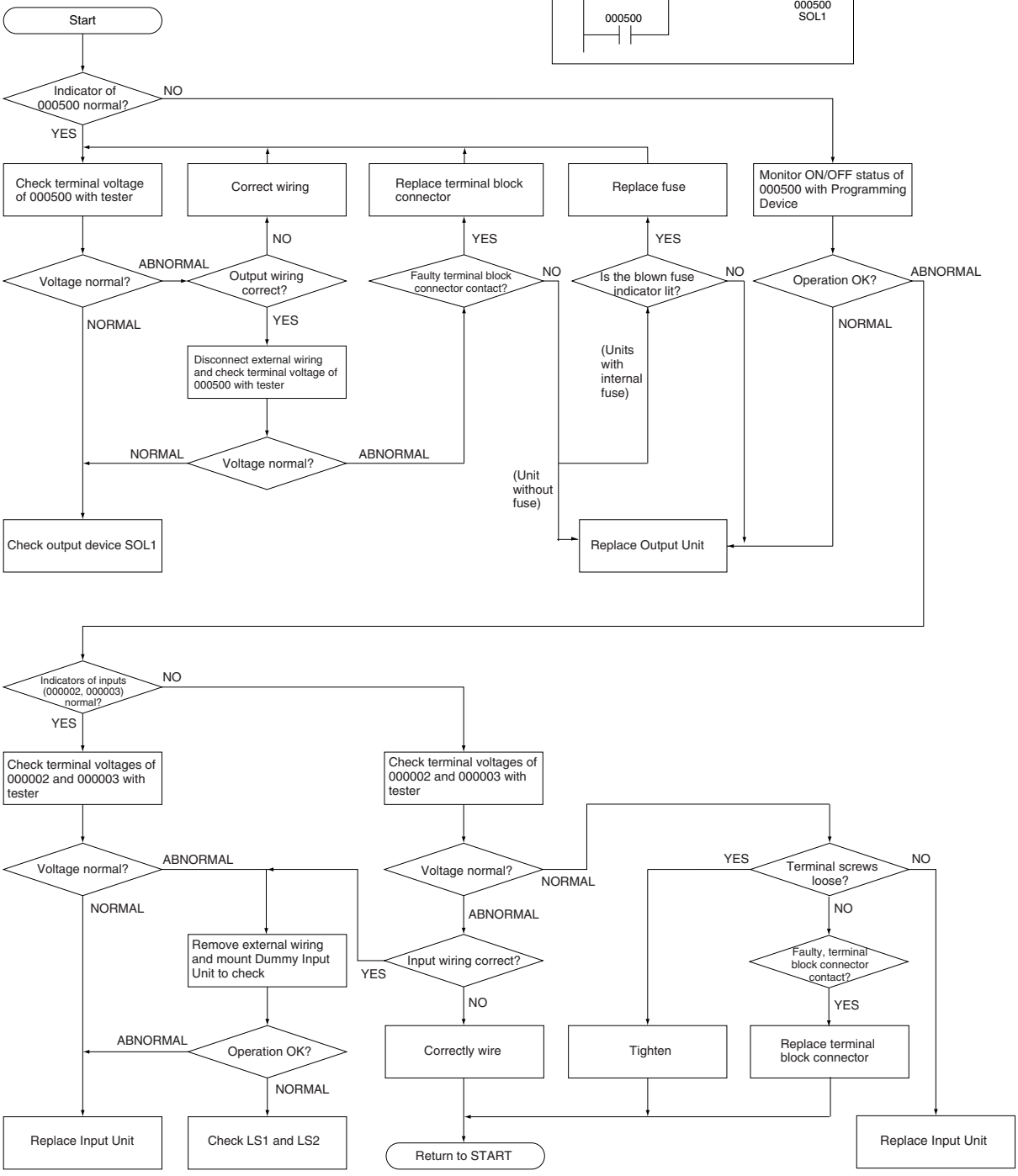
10-2-13 Environmental Conditions Check



10-2-14 I/O Check

The I/O check flowchart is based on the following ladder diagram section assuming that SOL1 does not turn ON.





10-3 Troubleshooting Racks and Units

CPU Racks and Standard Expansion Racks

Symptom	Cause	Remedy
POWER indicator is not lit on Power Supply Unit.	PCB short-circuited or damaged.	Replace Power Supply Unit or Backplane.
RUN indicator is not lit on CPU Unit	(1) Error in program.	Correct program.
	(2) Power line is faulty.	Replace Power Supply Unit.
RUN output does not turn ON on Power Supply Unit. RUN indicator lit on CPU Unit.	Internal circuitry of Power Supply Unit is faulty.	Replace Power Supply Unit.
Serial Communications Unit or CS-series CPU Bus Unit does not operate or malfunctions.	(1) The I/O Connecting Cable is faulty. (2) The I/O bus is faulty.	Replace the I/O Connecting Cable. Replace the Backplane.
Bits do not operate past a certain point.		
Error occurs in units of 8 or 16 points.		
I/O bit turns ON.		
All bits in one Unit do not turn ON.		

Special I/O Units

Refer to the *Operation Manual* for the Special I/O Unit to troubleshoot any other errors.

Symptom	Cause	Remedy
The ERH and RUN indicators on the Special I/O Unit are lit.	I/O refreshing is not being performed for the Unit from the CPU Unit (CPU Unit monitoring error). It's possible that cyclic refreshing has been disabled for the Special I/O Unit in the Cyclic Refresh Disable Setting in the PLC Setup (i.e., the bit corresponding to the unit number has been set to 1).	Change the bit corresponding to the unit number to 0 to enable cyclic refreshing, or make sure that the Unit is refreshed from the program using IORF at least once every 11 s.

Long-distance Expansion Racks

Symptom	Cause	Remedy
Expansion Rack not detected.	(1) A Terminator is not connected.	If the TERM indicator is lit, connect a Terminator.
	(2) An Expansion Rack is not connected correctly.	Recheck the connections and configuration using information in *2-2-2 Expansion Racks* and *2-10-1 CS1W-IC102 I/O Control Units, I/O Interface Units, and Terminators.*
	(3) A Unit is faulty.	Gradually remove/replace Units to determine the Unit that is faulty, including the Backplane, Power Supply Unit, I/O Units, I/O Control/Interface Unit, and I/O Connecting Cable.
I/O bus error or I/O verification error occurs.	(1) An I/O Connecting Cable or Terminator connection is faulty.	Check that I/O Connecting Cables and Terminators are connected correctly.
	(2) Noise or other external factor.	Separate all cables from possible sources of noise or place them in metal ducts.
	(3) A Unit is faulty.	Gradually remove/replace Units to determine the Unit that is faulty, including the Backplane, Power Supply Unit, I/O Units, I/O Control/Interface Unit, and I/O Connecting Cable.

Symptom	Cause	Remedy
Cycle time is too long.	(1) A CPU Bus Unit that is allocated many words (e.g., Controller Link Unit) is mounted to a Long-distance Expansion Rack.	Move the CPU Bus Unit to the CPU Rack.
	(2) A Unit is faulty.	Gradually remove/replace Units to determine the Unit that is faulty, including the Backplane, Power Supply Unit, I/O Units, I/O Control/Interface Unit, and I/O Connecting Cable.
I/O Control Unit and I/O Interface Units do not appear on CX-Programmer I/O table.	This is not an error. These Units are not allocated I/O words and thus are not registered in the I/O tables.	---

Input Units

Symptom	Cause	Remedy
Not all inputs turn ON or indicators are not lit.	(1) Power is not supplied to Input Unit.	Supply power
	(2) Supply voltage is low.	Adjust supply voltage to within rated range.
	(3) Terminal block mounting screws are loose.	Tighten screws.
	(4) Faulty contact of terminal block connector.	Replace terminal block connector.
Not all inputs turn ON (indicator lit).	Input circuit is faulty. (There is a short at the load or something else that caused an overcurrent to flow.)	Replace Unit.
Not all inputs turn OFF.	Input circuit is faulty.	Replace Unit.
Specific bit does not turn ON.	(1) Input device is faulty.	Replace input devices.
	(2) Input wiring disconnected.	Check input wiring.
	(3) Terminal block screws are loose.	Tighten screws.
	(4) Faulty terminal block connector contact.	Replace terminal block connector.
	(5) Too short ON time of external input.	Adjust input device.
	(6) Faulty input circuit	Replace Unit.
	(7) Input bit number is used for output instruction.	Correct program.
Specific bit does not turn OFF.	(1) Input circuit is faulty.	Replace Unit.
	(2) Input bit number is used for output instruction.	Correct program.
Input irregularly turns ON/OFF.	(1) External input voltage is low or unstable.	Adjust external input voltage to within rated range.
	(2) Malfunction due to noise.	Take protective measures against noise, such as: (1) Increase input response time (PLC Setup) (2) Install surge suppressor. (3) Install insulation transformer. (4) Install shielded cables between the Input Unit and the loads.
	(3) Terminal block screws are loose.	Tighten screws.
	(4) Faulty terminal block connector contact.	Replace terminal block connector.
Error occurs in units of 8 points or 16 points, i.e., for the same common.	(1) Common terminal screws are loose.	Tighten screws.
	(2) Faulty terminal block connector contact.	Replace terminal block connector.
	(3) Faulty data bus	Replace Unit.
	(4) Faulty CPU	Replace CPU.
Input indicator is not lit in normal operation.	Faulty indicator or indicator circuit.	Replace Unit.

Output Units

Symptom	Cause	Remedy
Not all outputs turn ON.	(1) Load is not supplied with power.	Supply power
	(2) Load voltage is low.	Adjust voltage to within rated range.
	(3) Terminal block screws are loose.	Tighten screws.
	(4) Faulty terminal block connector contact.	Replace terminal block connector.
	(5) An overcurrent (possibly caused by a short at the load) resulted in a blown fuse in the Output Unit. (Some Output Units provide an indicator for blown fuses.)	Replace fuse or Unit.
	(6) Faulty I/O bus connector contact.	Replace Unit.
	(7) Output circuit is faulty.	Replace Unit.
	(8) If the INH indicator is lit, the Output OFF Bit (A50015) is ON.	Turn A50015 OFF.
Not all outputs turn OFF.	Output circuit is faulty.	Replace Unit.
Output of a specific bit number does not turn ON or indicator is not lit.	(1) Output ON time too short because of a mistake in programming.	Correct program to increase the time that the output is ON.
	(2) Bit status controlled by multiple instructions.	Correct program so that each output bit is controlled by only one instruction.
	(3) Faulty output circuit.	Replace Unit.
Output of a specific bit number does not turn ON (indicator lit).	(1) Faulty output device.	Replace output device.
	(2) Break in output wiring.	Check output wiring.
	(3) Loose terminal block screws.	Tighten screws.
	(4) Faulty terminal block connector faulty.	Replace terminal block connector.
	(5) Faulty output bit.	Replace relay or Unit.
	(6) Faulty output circuit.	Replace Unit.
Output of a specific bit number does not turn OFF (indicator is not lit).	(1) Faulty output bit.	Replace relay or Unit.
	(2) Bit does not turn OFF due to leakage current or residual voltage.	Replace external load or add dummy resistor.
Output of a specific bit number does not turn OFF (indicator lit).	(1) Bit status controlled by multiple instructions.	Correct program.
	(2) Faulty output circuit.	Replace Unit.
Output irregularly turns ON/OFF.	(1) Low or unstable load voltage.	Adjust load voltage to within rated range.
	(2) Bit status controlled by multiple instructions.	Correct program so that each output bit is controlled by only one instruction.
	(3) Malfunction due to noise.	Protective measures against noise: (1) Install surge suppressor. (2) Install insulation transformer. (3) Use shielded cables between the Output Unit and the loads.
	(4) Terminal block screws are loose.	Tighten screws.
	(5) Faulty terminal block connector contact.	Replace terminal block connector.
Error occurs in units of 8 points or 16 points, i.e., for the same common.	(1) Loose common terminal screw.	Tighten screws.
	(2) Faulty terminal block connector contact.	Replace terminal block connector.
	(3) An overcurrent (possibly caused by a short at the load) resulted in a blown fuse in the Output Unit.	Replace fuse or Unit.
	(4) Faulty data bus.	Replace Unit.
	(5) Faulty CPU.	Replace CPU.
Output indicator is not lit (operation is normal).	Faulty indicator.	Replace Unit.

10-4 Troubleshooting Errors in Duplex Connecting Cables

10-4-1 Identifying and Correcting the Cause of the Error

When a duplexed Connecting Cable is disconnected or damaged, the location of the error can be identified with Auxiliary Area flags (in A270 and A271), the CS1D I/O Control Unit LED indicators, and the CS1D I/O Interface Unit LED indicators.

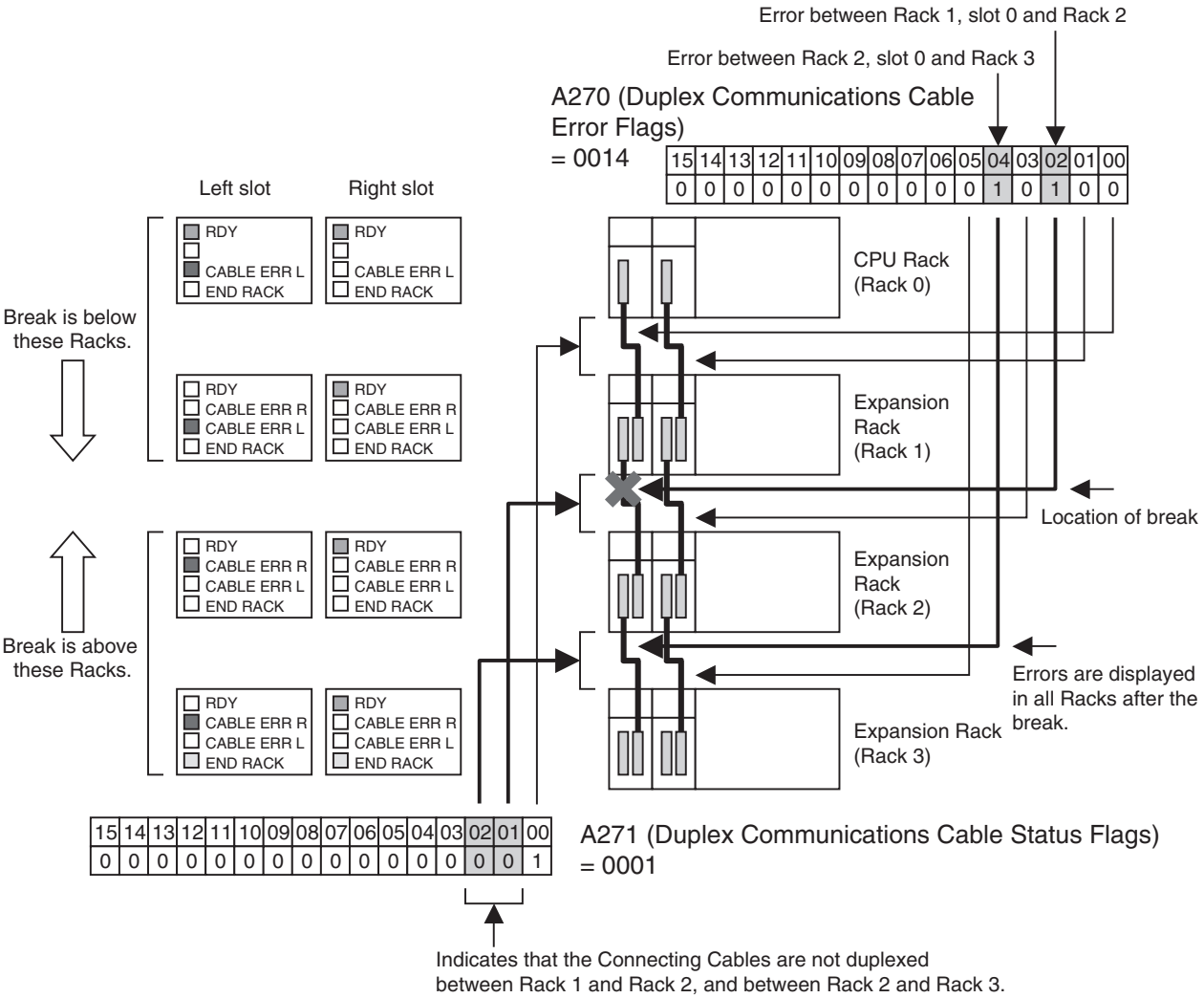
Note The CPU Unit's alarm output (alarm display) does not indicate the error.

■ Error Indications for a Disconnected/Damaged Connecting Cable

In this example, there is an error in the Connecting Cable between Rack 1, slot 0 and Rack 2, so the corresponding flag in A270 (A27002) is turned ON. The flag for the same slot in the following Rack (A27004) is also turned ON.

Since the error occurred in a Connecting Cable after Rack 1, the Duplex Communications Cable Status Flags are OFF for the connections between Rack 1 and Rack 2 (A27101) and between Rack 2 and Rack 3 (A27102).

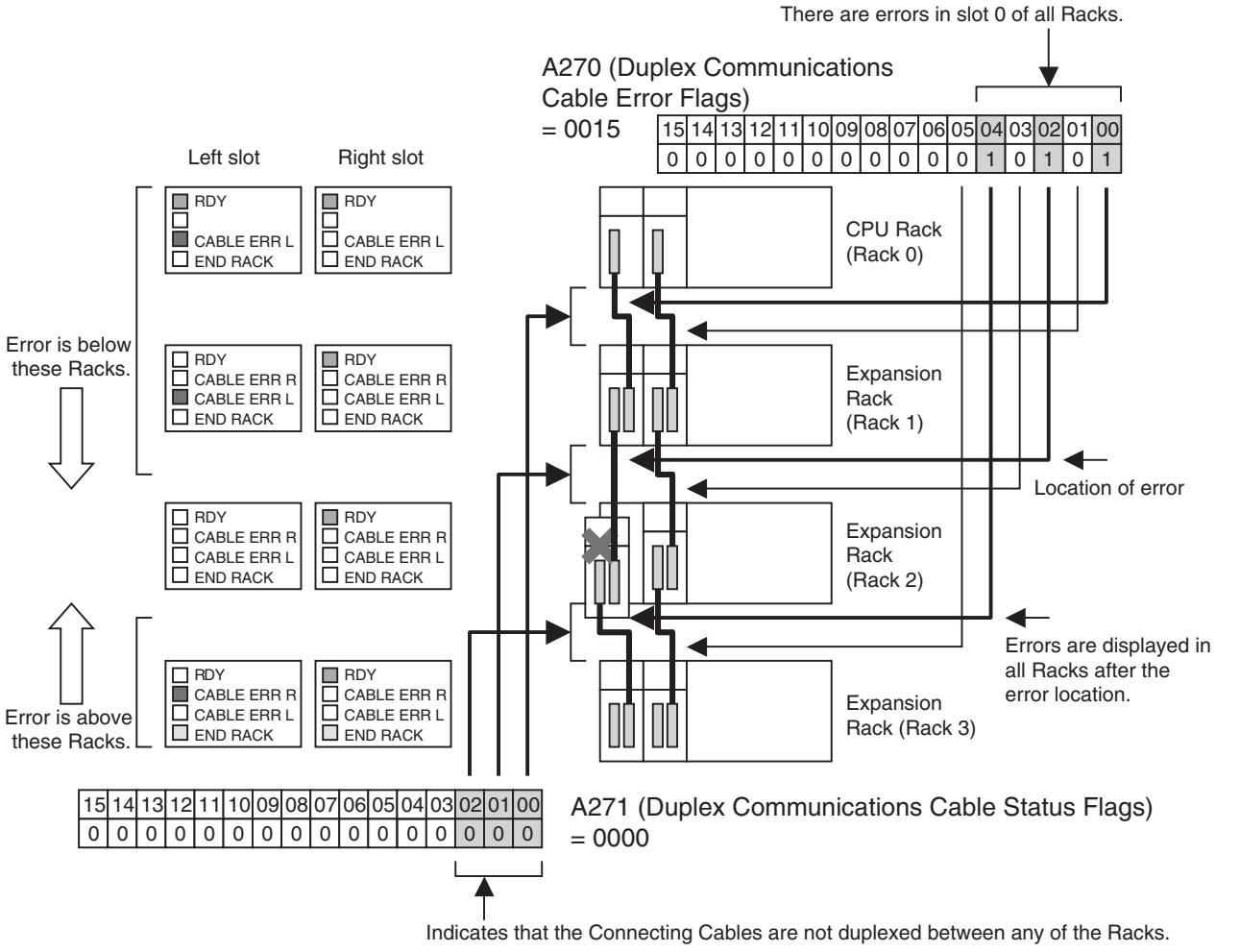
The CS1D I/O Control Unit and CS1D I/O Interface Unit LED indicators all indicate errors in the side where the break occurred. The CABLE ERR L Indicator is lit red in the Units above the break and the CABLE ERR R Indicator is lit red in the Units below the break.



■ Error Indications When an Expansion Unit is Removed

In this example, the Expansion Unit in Rack 1, slot 0 is removed, so the affected slot 0 flags in A270 (A27002, A27004, and A27006) are turned ON. The Duplex Communications Cable Status Flags are turned OFF for the all of the Racks (A27100 to A27102).

The CS1D I/O Control Unit and CS1D I/O Interface Unit LED indicators all indicate errors in the side where the error occurred. The CABLE ERR L Indicator is lit red in the Units above the error and the CABLE ERR R Indicator is lit red in the Units below the error.



■ Troubleshooting Connecting Cable and Expansion Unit Problems

Once the error location has been identified, use the remedy described in the following table to correct the error.

Cause	Remedy
Disconnected Connecting Cable	Connect the cable that is disconnected.
Bad cable connection	Disconnect the cable and then connect it again. If an error occurs when the cable is reconnected, replace the cable. **Note** If the cable to the other slot is disconnected, the PLC will stop.

Cause	Remedy
Cable IN/OUT connections are reversed.	Connect the Connecting Cables properly. If either cable is connected to the wrong side when the power supply is turned ON, an I/O bus error C will occur and the PLC will not operate. **Note** If the cable to the other slot is disconnected, the PLC will stop.
Faulty Expansion Unit	Replace the Expansion Unit. Refer to *11-6 Replacement of Expansion Units* for details. **Note** If the cable to the other slot is disconnected, the PLC will stop.

SECTION 11
Inspection and Maintenance

This section provides inspection and maintenance information.

11-1 Inspections

Daily or periodic inspections are required in order to maintain the CS1D's functions in peak operating condition.

11-1-1 Inspection Points

The major electronic components in CS1D PLCs are semiconductor components, which although have an extremely long life time, can deteriorate under improper environmental conditions. Periodic inspections are thus required to ensure that the required conditions are being kept.

Inspection is recommended at least once every six months to a year, but more frequent inspections will be necessary in adverse environments.

Take immediate steps to correct the situation if any of the conditions in the following table are not met.

Inspection Points

No.	Item	Inspection	Criteria	Action
1	Source Power Supply	Check for voltage fluctuations at the power supply terminals.	The voltage must be within the allowable voltage fluctuation range. (See note.)	Use a voltage tester to check the power supply at the terminals. Take necessary steps to bring voltage fluctuations within limits.
2	I/O Power Supply	Check for voltage fluctuations at the I/O terminals.	Voltages must be within specifications for each Unit.	Use a voltage tester to check the power supply at the terminals. Take necessary steps to bring voltage fluctuations within limits.
3	Ambient environment	Check the ambient temperature. (Inside the control panel if the PLC is in a control panel.)	0 to 55°C	Use a thermometer to check the temperature and ensure that the ambient temperature remains within the allowed range of 0 to 55°C.
		Check the ambient humidity. (Inside the control panel if the PLC is in a control panel.)	Relative humidity must be 10% to 90% with no condensation.	Use a hygrometer to check the humidity and ensure that the ambient humidity remains within the allowed range.
		Check that the PLC is not in direct sunlight.	Not in direct sunlight	Protect the PLC if necessary.
		Check for accumulation of dirt, dust, salt, metal filings, etc.	No accumulation	Clean and protect the PLC if necessary.
		Check for water, oil, or chemical sprays hitting the PLC.	No spray on the PLC	Clean and protect the PLC if necessary.
		Check for corrosive or flammable gases in the area of the PLC.	No corrosive or flammable gases	Check by smell or use a sensor.
		Check the level of vibration or shock.	Vibration and shock must be within specifications.	Install cushioning or shock absorbing equipment if necessary.
		Check for noise sources near the PLC.	No significant noise sources	Either separate the PLC and noise source or protect the PLC.

No.	Item	Inspection	Criteria	Action
4	Installation and wiring	Check that each Unit is installed securely.	No looseness	Tighten loose screws with a Phillips-head screwdriver.
		Check that cable connectors are fully inserted and locked.	No looseness	Correct any improperly installed connectors.
		Check for loose screws in external wiring.	No looseness	Tighten loose screws with a Phillips-head screwdriver.
		Check crimp connectors in external wiring.	Adequate spacing between connectors	Check visually and adjust if necessary.
		Check for damaged external wiring cables.	No damage	Check visually and replace cables if necessary.
5	User-serviceable parts	Check whether the CS1W-BAT01 Battery has reached its service life.	Life expectancy is 5 years at 25°C, less at higher temperatures. (From 0.4 to 5 years depending on model, power supply rate, and ambient temperature.)	Replace the battery when its service life has passed even if a battery error has not occurred. (Battery life depends upon the model, the percentage of time in service, and ambient conditions.)

Note The following table shows the allowable voltage fluctuation ranges for source power supplies.

Supply voltage	Allowable voltage range
100 to 120 V AC	85 to 132 V AC
200 to 240 V AC	170 to 264 V AC
24 V DC	19.2 to 28.8 V DC

Tools Required for Inspections

Required Tools

- Slotted and Phillips-head screwdrivers
- Voltage tester or digital voltmeter
- Industrial alcohol and clean cotton cloth

Tools Required Occasionally

- Synchroscope
- Oscilloscope with pen plotter
- Thermometer and hygrometer (humidity meter)

11-1-2 Unit Replacement Precautions

Check the following when replacing any faulty Unit.

- Either do not replace a Unit until the power is turned OFF or perform one of the following.

Replacing a CPU Unit	Set the switch on the Duplex Unit to “NO USE” and turn OFF the power supply only to the CPU Unit being replaced. (Duplex CPU Systems only)
Replacing a Basic I/O Unit, Special I/O Unit, or CPU Bus Unit	Perform the online Unit replacement operation from the CX-Programmer or from a Programming Console.
Replacing a Power Supply Unit	Turn OFF the power supply to the Power Supply Unit being replaced.

Replacing a Duplex Unit (Duplex CPU, Dual I/O Expansion System only)	Set the DPL Switch on the front of the Duplex Unit to NO USE and turn OFF the power supply to the Duplex Unit only.
Replacing an Expansion Unit (Duplex CPU, Dual I/O Expansion System with duplex Connection Cables only)	Disconnect the cables to the Expansion Unit and remove the Expansion Unit. **Note** Before replacing an Expansion Unit, verify that the cable to the other slot is functioning properly.

- Check the new Unit to make sure that there are no errors.
- If a faulty Unit is being returned for repair, describe the problem in as much detail as possible, enclose this description with the Unit, and return the Unit to your OMRON representative.
- For poor contact, take a clean cotton cloth, soak the cloth in industrial alcohol, and carefully wipe the contacts clean. Be sure to remove any lint prior to remounting the Unit.

Note

1. When replacing a CPU Unit, be sure that not only the user program but also all other data required for operation is transferred to or set in the new CPU Unit before starting operation, including DM Area and HR Area settings. If data area and other data are not correct for the user program, unexpected accidents may occur. Be sure to include the routing tables, Controller Link Unit data link tables, network parameters, and other CPU Bus Unit data, which are stored as parameters in the CPU Unit. Refer to the CPU Bus Unit and Special I/O Unit operation manuals for details on the data required by each Unit.
2. The simple backup operation can be used to store the user program and all parameters for the CS1D CPU Unit, DeviceNet Units, Serial Communications Units, and other specific Units in a Memory Card as backup files. A Memory Card and the simple backup operation can be used to easily restore data after replacing any of these Units. Refer to the *CS/CJ Series Programming Manual* (W394) for details.

11-2 Replacing User-serviceable Parts

The following parts should be replaced periodically as preventative maintenance. The procedures for replacing these parts are described later in this section.

- Battery (the CPU Unit's RAM-backup battery)

11-2-1 Battery Replacement

Battery Functions

The battery retains the following data of the CPU Unit's RAM when the main power supply is OFF. This data will not be stable when the power supply is turned OFF if a battery is not installed or the battery has expired its useful life.

- Retained regions of I/O memory (such as the Holding Area and DM Area)

Battery Service Life and Replacement Period

At 25°C, the maximum service life for batteries is 5 years whether or not power is supplied to the CPU Unit while the battery is installed. The battery's lifetime will be shorter when it is used at higher temperatures and when power is not supplied to the CPU Unit for long periods. In the worst case conditions, the battery will last for only 1.8 years.

The time that CPU power is ON shown in the following table (power supply rate) is calculated as follows:

Power supply rate =

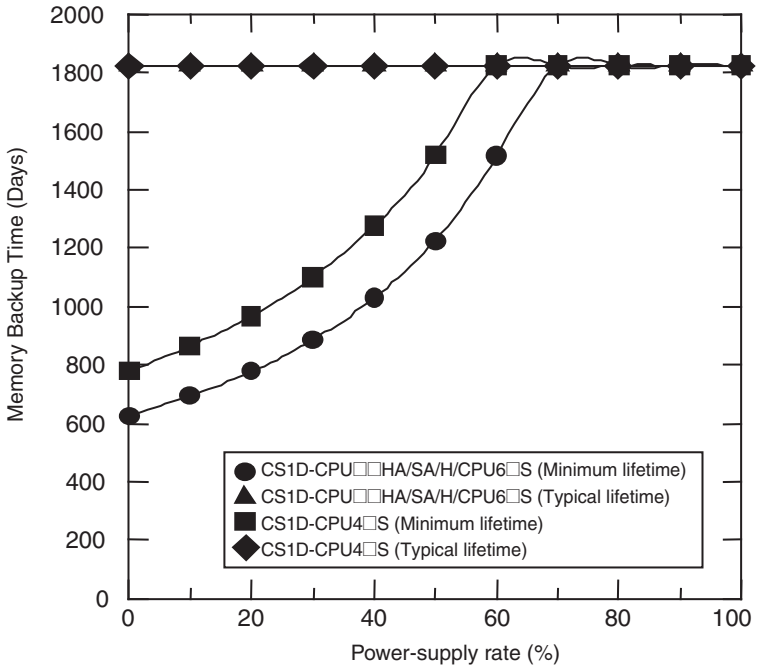
Total time power is ON/(total time power is ON + total time power is OFF)

The following table shows minimum lifetimes and typical lifetimes for the backup battery.

Model	Time that CPU Unit power is ON	Minimum lifetime	Typical lifetime	Min. time for battery error detection	Time from battery error detection to complete discharge
CS1D-CPU□□HA CS1D-CPU□□SA CS1D-CPU□□H CS1D-CPU6□S	0%	626 days (1 yr, 8 mo)	1,825 days (5 yr)	626 days	5 days
	30%	886 days (2 yr, 5 mo)	1,825 days (5 yr)	886 days	5 days
	50%	1,225 days (3 yr, 4 mo)	1,825 days (5 yr)	1,225 days	5 days
	70%	1,825 days (5 yr)	1,825 days (5 yr)	1,825 days	5 days
	100%	1,825 days (5 yr)	1,825 days (5 yr)	1,825 days	5 days
CS1D-CPU4□S	0%	780 days (2 yr, 1 mo)	1,825 days (5 yr)	780 days	5 days
	30%	1,101 days (3 yr)	1,825 days (5 yr)	1,101 days	5 days
	50%	1,519 days (4 yr, 1 mo)	1,825 days (5 yr)	1,519 days	5 days
	70%	1,825 days (5 yr)	1,825 days (5 yr)	1,825 days	5 days
	100%	1,825 days (5 yr)	1,825 days (5 yr)	1,825 days	5 days

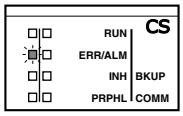
Note

1. The minimum lifetime is the memory backup time at an ambient temperature of 55°C. The typical lifetime is the memory backup time at an ambient temperature of 25°C.
2. There is no difference between the minimum lifetimes and the minimum times to battery error detection.
3. The battery lifetime and low battery voltage detection will vary under application at high power-supply rates.

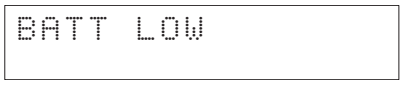


Low Battery Indicators

If the PLC Setup has been set to detect a low-battery error, the ERR/ALM indicator on the front of the CPU Unit will flash when the CPU Unit detects that the battery is nearly discharged.



When the ERR/ALM indicator flashes, connect the CX-Programmer to the peripheral port and read the error message. If the message “BATT LOW” appears on the Programming Console* and the Battery Error Flag (A40204) is ON*, first check whether the battery is properly connected to the CPU Unit. If the battery is properly connected, replace the battery as soon as possible.



Once a low-battery error has been detected, it will take 5 days before the battery fails. Battery failure can be delayed by ensuring that the CPU Unit power is not turned OFF until the battery has been replaced.

Note *The PLC Setup must be set to detect a low-battery error (Detect Low Battery). If this setting has not been made, the BATT LOW error message will not appear on the Programming Console and the Battery Error Flag (A40204) will not go ON when the battery fails.

Replacement Battery

Install a replacement battery within 2 years of the production date shown on the battery’s label.

Use the following replacement battery: CS1W-BAT01 Battery Set

Manufactured in June 2002.

Replacement Battery

The battery replacement method depends on whether a CPU Unit is used in a duplex or simplex system, and on the CPU Unit’s unit version.

⚠ **Caution** We recommend replacing the battery with the power OFF to prevent the CPU Unit’s sensitive internal components from being damaged by static electricity. The battery can be replaced with the power ON, but be sure to touch a grounded metal object to discharge any static electricity before replacing the battery. After replacing the battery, connect a Programming Device and clear the battery error.

Unit Versions and Corresponding Battery Replacement Methods

Type	Unit version	Number of battery connectors	Replacement time (see note)	Replacement method
CPU Simplex System	Unit Ver. 2.□	1	3 min.	Refer to *Replacement Procedure for CS1-H (Pre-Ver. 2.0 and Ver. 2.0) CPU Units with One Battery Connectors*.
	Unit Ver. 4.0 or later	2	3 min.	Refer to *Replacement Procedure for CPU Units with Two Battery Connectors (CPU Units for CS1D Duplex-CPU Systems with unit version 1.2 or later / CPU Units for Single CPU Systems with unit version 4.0 or later).*

Type	Unit version	Number of battery connectors	Replacement time (see note)	Replacement method
CPU Duplex System	No unit version Unit Ver. 1.1	1	3 min.	Refer to *Replacement Procedure for CPU Units with One Battery Connector*.
	Unit Ver. 1.2 or later	2	3 min.	Refer to *Replacement Procedure for CPU Units with Two Battery Connectors (CPU Units for CS1D Duplex-CPU Systems with unit version 1.2 or later / CPU Units for Single CPU Systems with unit version 4.0 or later).*

Replacement Procedure for CPU Units with One Battery Connector

Use the following procedure to replace a battery that has been completely discharged.

1,2,3... 1. Turn OFF the power to the CPU Unit. (If the power was already OFF, turn the power ON for at least one minute before turning the power OFF again.)

Note There is a capacitor in the CPU Unit that will back up memory while the battery is being replaced. If this capacitor is not completely charged by turning ON the power supply for one minute, data will not be stable during battery replacement.

2. Insert a small flat-blade screwdriver into the notch at the bottom of the battery compartment cover and lift open the cover.
3. Disconnect the connector under the cover of the CPU Unit, remove the old battery from the compartment, and replace the battery with a new one.

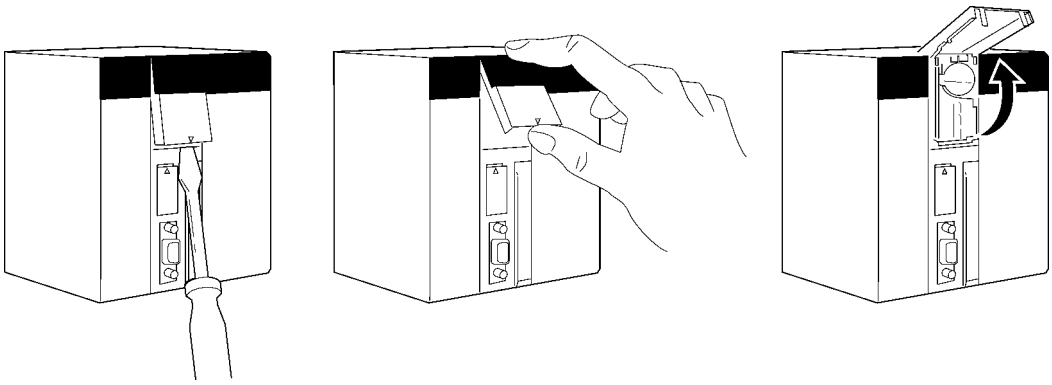
Note Complete the battery replacement procedure (at an ambient temperature of 25°C) within three minutes of turning OFF the power supply. If more than three minutes elapse without a battery installed in the CPU Unit, data will not be stable during battery replacement.

Replacement Procedure for CPU Units with Two Battery Connectors (CPU Units for CS1D Duplex-CPU Systems with unit version 1.2 or later / CPU Units for Single CPU Systems with unit version 4.0 or later)

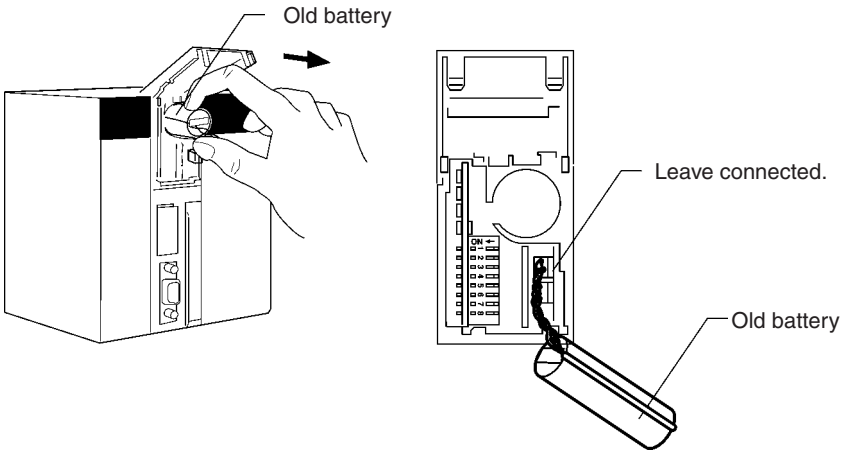
Use the following procedure to replace a battery that has been completely discharged.

When replacing a battery with the power OFF, connect the new battery while the old battery is in place. Remove the old battery after connecting the new battery. (There are two pairs of identical connectors for the battery. The old battery will not be charged even if the new battery is connected at the same time.)

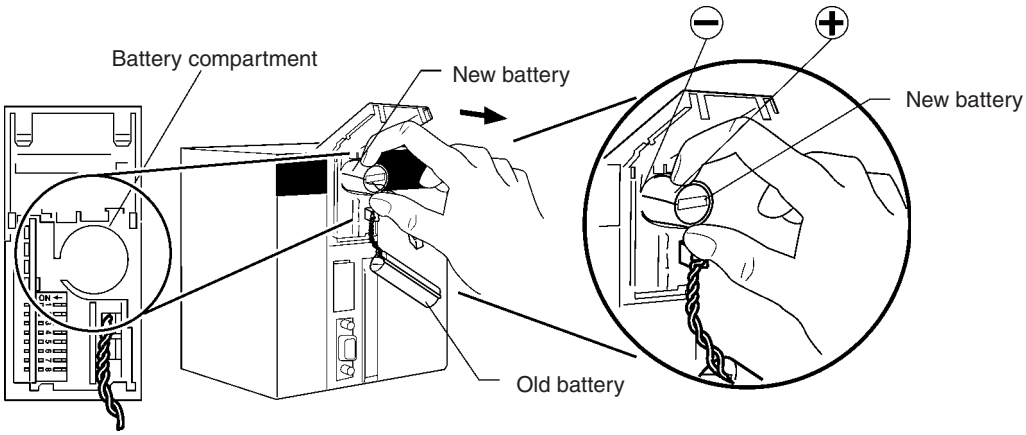
1,2,3... 1. Turn OFF the power to the CPU Unit. (If the power was already OFF, turn the power ON for at least ten seconds before turning the power OFF again.)
2. Insert a small flat-blade screwdriver into the notch at the bottom of the battery compartment cover and lift open the cover.



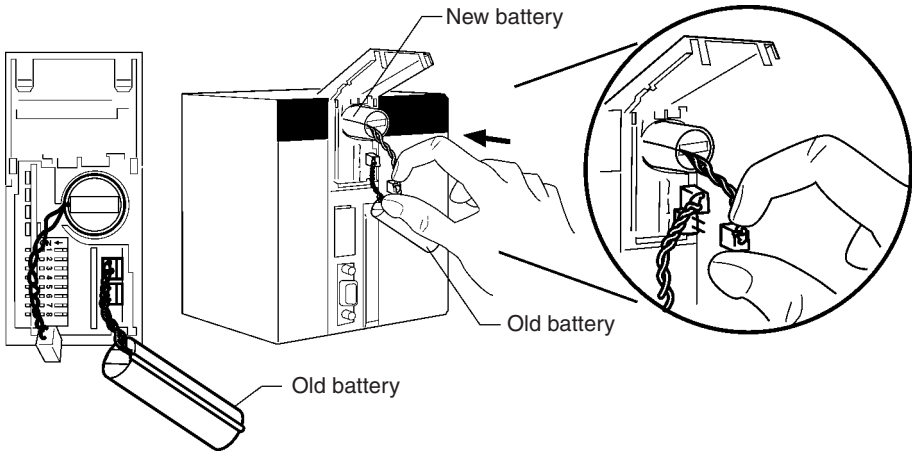
3. Remove the old battery from the compartment, but leave its connector connected.



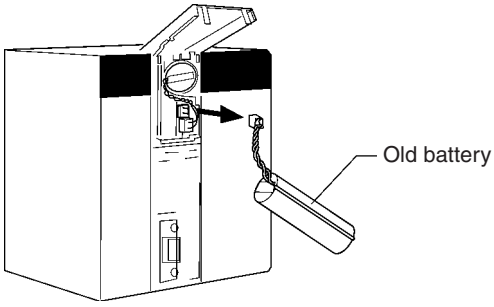
4. Insert the new battery into the battery compartment with the cable and connector facing outward.



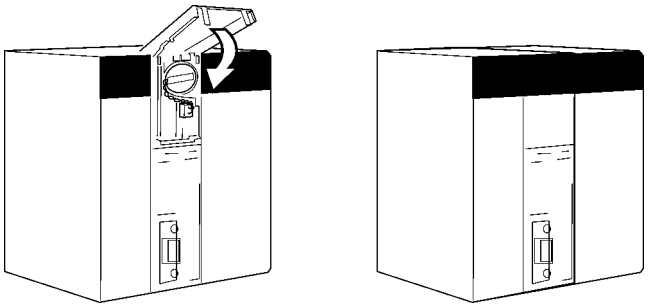
5. With the old battery connected, insert the new battery's connector in the open connector in the CPU Unit. Be sure that the connector is inserted so that its red wire is at the top and the white wire is at the bottom.



6. Remove the old battery's connector.



7. Push the new battery's wire into the battery compartment and close the cover.



8. Connect a Programming Device and verify that the Battery Error has been cleared.

Note

1. Replacement procedure for CPU Units with two battery connectors, even if this procedure is not used and the old battery is disconnected with the power OFF (power OFF and no battery connected), memory will be backed up for a short time by an internal capacitor. In this case, the internal capacitor will discharge within approximately 30 s after the power is turned OFF, so be sure to connect the new battery immediately.
2. If the above procedure is not used and the old battery is disconnected with the power ON (power ON and no battery connected), memory will still be backed up. However, be sure to touch a grounded metal object to discharge any static electricity before replacing the battery.
3. With CPU Units that have two battery connectors, leave the old battery attached while connecting the new battery. This prevents a battery error occurring during battery replacement. Remove the old battery after the new battery is connected.

⚠ **Caution** Do not short the battery terminals or charge, disassemble, heat, or incinerate the battery. Do not subject the battery to strong shocks. Doing any of these may result in leakage, rupture, heat generation, or ignition of the battery.

⚠ **Caution** Dispose of any battery that has been dropped on the floor or otherwise subjected to excessive shock. Batteries that have been subjected to shock may leak if they are used.

⚠ **Caution** Do not allow unqualified persons to replace batteries. UL standards required that batteries be replaced only by experienced technicians.

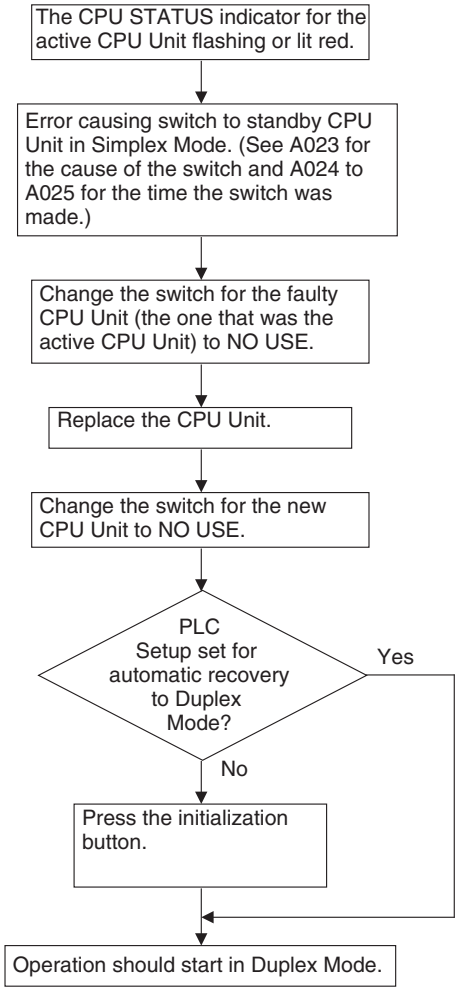
⚠ **Caution** Turn ON the power after replacing the battery for a CPU Unit that has been unused for a long time. Leaving the CPU Unit unused again without turning ON the power even once after the battery is replaced may result in a shorter battery life.

11-3 Replacing a CPU Unit

If the active CPU Unit fails during operation in a Duplex CPU System, the standby CPU Unit will switch to become the active CPU Unit and operation will continue. Use the following procedure to replace the faulty CPU Unit and restore duplex operation.

Online Unit replacement is not possible for a CPU Unit in a Single CPU System. Turn OFF the power supply to the PLC before replacing the Unit.

11-3-1 Replacement Flowchart after Switch to Standby CPU Unit



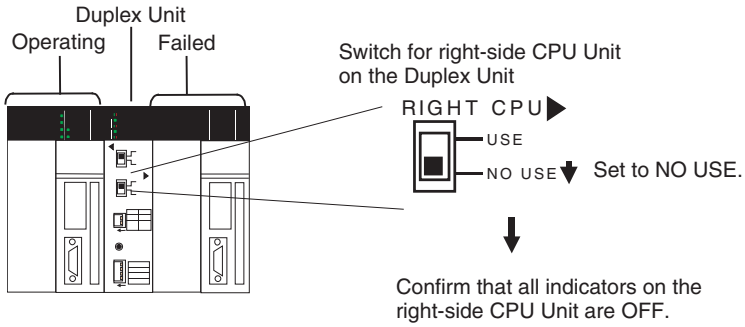
11-3-2 CPU Unit Replacement Procedure

1,2,3... 1. Change the USE/NO USE switch for the CPU Unit to be replaced to NO USE. When the switch is changed to NO USE, the power supply to the CPU Unit will turn OFF.

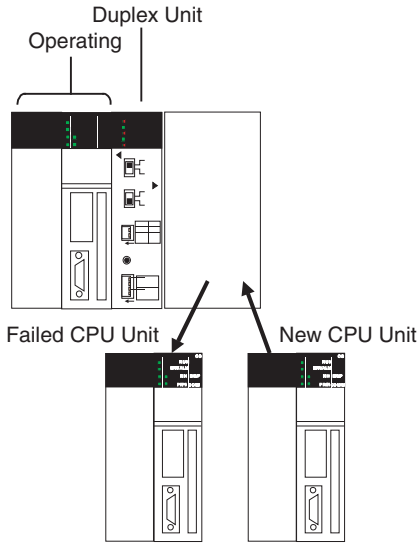
2. Confirm that the indicators on the CPU Unit to be replaced have all gone out.

⚠**Caution** You must set the USE/NO USE switch on the Duplex Unit to NO USE before replacing a CPU Unit to turn OFF the power supply to the CPU Unit. If a CPU Unit is replaced while power is still being provided (i.e., with the switch set to USE), the CPU Backplane for Duplex CPU System or Duplex Unit may be damaged.

Example: The following illustration shows the switch setting when the right CPU Unit has failed and the left CPU Unit has taken over operation in Simplex Mode.



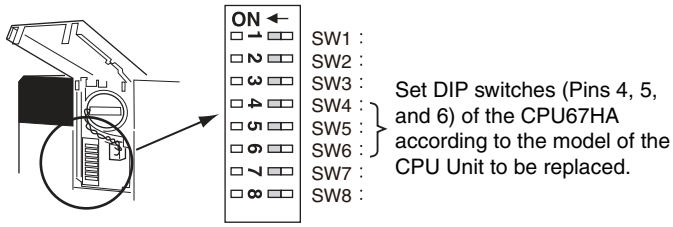
3. Replace the faulty CPU Unit with a new CPU Unit.



4. Make sure of using either of the following for the new CPU Unit.
   - CPU Unit model same as before replacement
   - Set the CS1D-CPU67HA to allow the combination of the CPU Unit model in operation and the Duplex CPU Compatible Setting when using the Duplex CPU Compatibility Setting of the CS1D-CPU67HA.

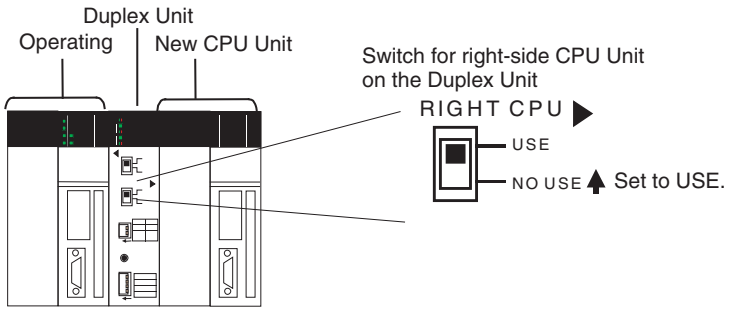
     To determine whether or not CPU Unit duplication is possible for the combination of a CPU Unit model and Duplex CPU Compatible Setting, refer to *3-1-8 Duplex CPU Compatible Setting*.

Duplex CPU compatibility setting is set with DIP switches (Pin 4, 5, and 6).



Note When changing the Duplex CPU Compatible Setting using the DIP switches (Pins 4, 5, and 6), do so after performing Memory All Clear using the Programming Device and then turning the CPU Unit power off. If the Duplex CPU Compatible Setting is changed without executing Memory All Clear, a memory error (Duplex CPU Compatible Setting change error) will occur.

5. Change the USE/NO USE switch for the new CPU Unit to USE.



Note If the PLC Setup is not set for automatic recovery to Duplex Mode (the default setting disables automatic recovery), then the program and parameter data will not be transferred to the new CPU Unit even if the USE/NO USE switch is set to USE. Operation will continue in Simplex Mode and operation will stop if an error occurs in the CPU Unit that is currently running.

Note If a memory error (Detailed error: Duplex CPU compatible setting change error) occurs in the CS1D-CPU67HA, reset the error according to the following procedure.

(1) Change the setting of the CPU USE/NO USE switch to “NO USE” from “USE.”

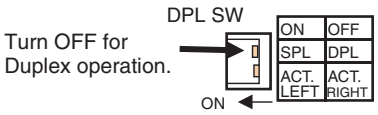
(2) Set the DPL SW to “SPL,” and change the setting of the CPU USE/NO USE switches to “USE” from “NO USE.”

(3) Connect the Programming Device and execute Memory All Clear. (In the CX-Programmer, select ***Clear All Memory Areas*** from ***PLC*** menu.)

(4) Change the setting of the CPU USE/NO USE switches to “NO USE” from “USE,” and set the DPL SW to “DPL.”

(5) Change the setting of the CPU USE/NO USE switches to “USE” from “NO USE.” Proceed to step 5.

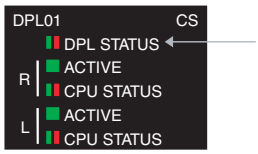
6. Use the following procedure if the PLC Setup has not been changed to enable automatic recovery to Duplex Mode.
   a) Confirm that the switch is set for duplex operation.



   b) After setting the USE/NO USE switch to USE, press the initialization button.

   Note If initialization is not started when the initialization button is pressed, press it again.

   c) When the initialization button is pressed, the DPL STATUS and CPU STATUS indicators will flash green and the program and parameter data will be transferred. When these indicators stop flashing and light green, the transfer has been completed and operation has restarted in Duplex Mode.



If automatic recovery to Duplex Mode has been set in the PLC Setup and the mode has been set to Duplex Mode on the Duplex Unit, the program and parameter data will be transferred automatically and operation will restart in Duplex Mode when the USE/NO USE switch is set to USE.

11-4 Online Replacement of I/O Units, Special I/O Units, and CPU Bus Units

I/O Units, Special I/O Units, and CPU Bus Units can be replaced while power is being supplied and the PLC is operating in both Single CPU and Duplex CPU Systems.

- Online replacement is possible from a Programming Console or the CX-Programmer (Ver. 3.1 or later).
- I/O for the Unit that is being replaced with be interrupted during the replacement operation.
- When a Unit is replaced, some of that Unit's CPU Unit data is retained and some is cleared.
  A Basic I/O Unit's output data is retained.
  A Basic I/O Unit's input data is not retained.
  If the Unit is a Special I/O Unit or CPU Bus Unit, the data is retained in Special I/O Unit Area or CPU Bus Unit Area allocated to that Unit.

⚠ **Caution** Before replacing a Unit online, always disable the operation of all connected external devices before starting the replacement procedure. Unexpected outputs from the Unit being replaced may result in unexpected operation of controlled devices or systems.

⚠Caution If an Output Unit is replaced and ON status is held in memory for that Unit, the corresponding output will turn ON as soon as the online replacement operation has been completed. Confirm system safety in advance.

⚠Caution When online replacement is started or completed in a Duplex CPU System, duplex initialization will be performed. This will cause a cycle time that is longer than the normal cycle time. Confirm system safety in advance for the increase in the cycle time.

11-4-1 Replacing One Unit at a Time

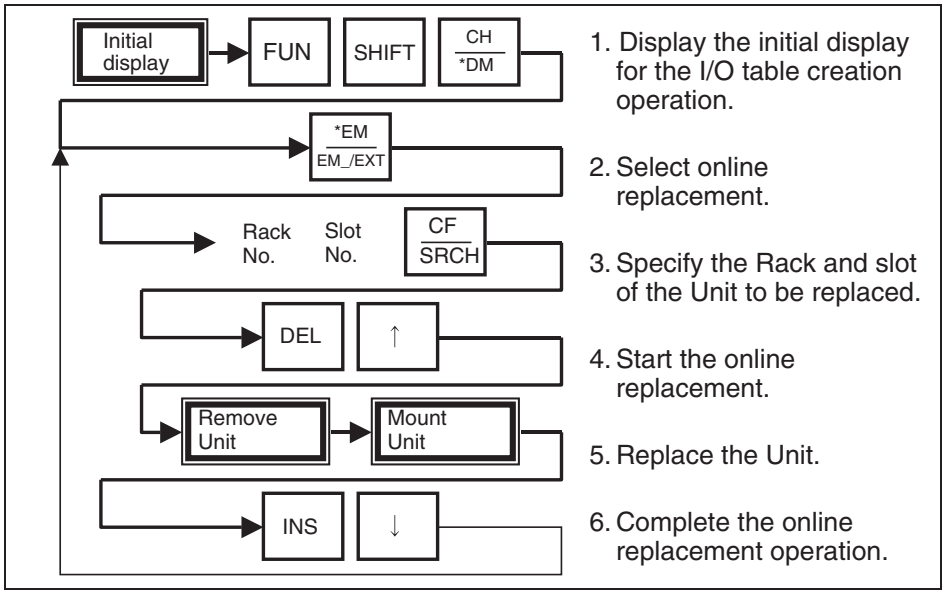
Operating Mode

As shown below, online replacement is possible in any operating mode.

RUN	MONITOR	PROGRAM
OK	OK	OK

Note Units cannot be replaced if the CPU is on standby or power is interrupted to an Expansion Rack.

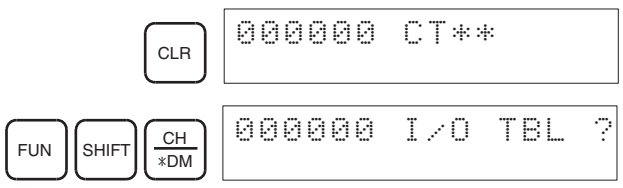
Basic Procedure



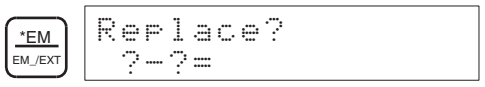
Example Procedure

1,2,3...

1. Connect a Programming Console to the peripheral port on the active CPU Unit.
2. Access the I/O table creation display from the initial display by pressing the keys shown below.



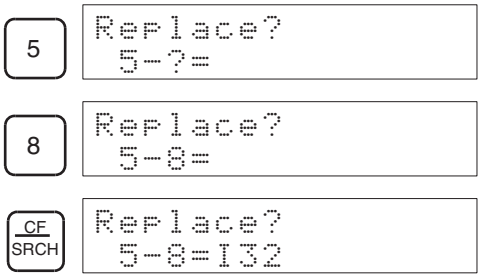
3. Select online replacement by pressing the EXT Key.



To exit online replacement, go to step *7.* To start online replacement, continue to step *4.*

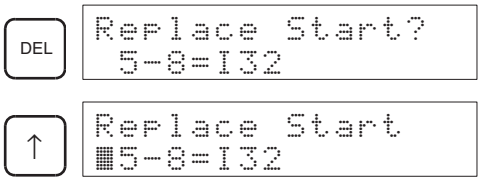
4. Specify the number of the Rack and the slot where the Unit is to be replaced.

   In this example, slot 8 on Rack 5 is used. In 5-8=I32 in the following displays, 5 is the rack number, 8 is the slot number, and I32 is the Unit type.



⚠Caution Before replacing a Unit online, always disable the operation of all connected external devices before starting the replacement procedure. Unexpected outputs from the Unit being replaced may result in unexpected operation of controlled devices or systems.

5. Start the online replacement operation by pressing the DEL Key and Up Key. The square displayed at the lower left of the display indicates that online replacement has been enabled.



6. Confirm that online replacement has been enabled using the flags listed in *Related Auxiliary Area Flags*, below, and then replace the Unit.

   Note After installing the replacement Unit, tighten the mounting screws to the proper torque to secure the Unit.

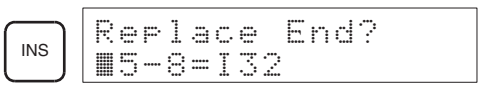
⚠WARNING Do not touch any live terminals. You will receive an electric shock.

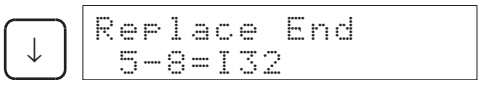
⚠Caution Before replacing a Unit online, always disable the operation of all connected external devices before starting the replacement procedure. Unexpected outputs from the Unit being replaced may result in unexpected operation of controlled devices or systems.

⚠Caution If an Output Unit is replaced and ON status is held in memory for that Unit, the corresponding output will turn ON as soon as the online replacement operation has been completed. Confirm system safety in advance.

Note Always replace the Unit with one of the same model number.

7. After the Unit has been replaced, end the online replacement operation by pressing the INS Key and Down Key.



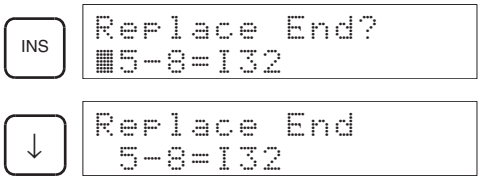


Canceling Online Replacement

Use the following procedure to return to the initial display after starting the online replacement procedure.

- Instead of the Rack and slot numbers, press the following keys to enter Online Replacement Mode.

- Press the INS Key and Down Key to go to the display that appears for step *6.* This will enable ending the online replacement operation.



Related Auxiliary Area Flags

Word	Bits	Description
A034	00 to 04	Used to confirm when online replacement is in progress for a slot on Rack 0. A bit will be ON when online replacement is in progress for the corresponding slot. Bits 00 to 04 correspond to slots 0 to 4. 00: ON when online replacement is in progress for slot 0 on Rack 0. 01: ON when online replacement is in progress for slot 1 on Rack 0. 02: ON when online replacement is in progress for slot 2 on Rack 0. 03: ON when online replacement is in progress for slot 3 on Rack 0. 04: ON when online replacement is in progress for slot 4 on Rack 0.
A035	00 to 08	Used to confirm when online replacement is in progress for a slot on Rack 1. A bit will be ON when online replacement is in progress for the corresponding slot. Bits 00 to 08 correspond to slots 0 to 8.
A036	00 to 08	Used to confirm when online replacement is in progress for a slot on Rack 2. A bit will be ON when online replacement is in progress for the corresponding slot. Bits 00 to 08 correspond to slots 0 to 8.
A037	00 to 08	Used to confirm when online replacement is in progress for a slot on Rack 3. A bit will be ON when online replacement is in progress for the corresponding slot. Bits 00 to 08 correspond to slots 0 to 8.
A038	00 to 08	Used to confirm when online replacement is in progress for a slot on Rack 4. A bit will be ON when online replacement is in progress for the corresponding slot. Bits 00 to 08 correspond to slots 0 to 8.
A039	00 to 08	Used to confirm when online replacement is in progress for a slot on Rack 5. A bit will be ON when online replacement is in progress for the corresponding slot. Bits 00 to 08 correspond to slots 0 to 8.

Word	Bits	Description
A040	00 to 08	Used to confirm when online replacement is in progress for a slot on Rack 6. A bit will be ON when online replacement is in progress for the corresponding slot. Bits 00 to 08 correspond to slots 0 to 8.
A041	00 to 08	Used to confirm when online replacement is in progress for a slot on Rack 7. A bit will be ON when online replacement is in progress for the corresponding slot. Bits 00 to 08 correspond to slots 0 to 8.
A261	10	ON while an online replacement operation is in progress. Turns OFF when the operation is completed normally.

Unit Types

The unit types displayed on the Programming Console during online replacement are listed in the following table.

Unit		Programming Console display	Examples
None or Dummy Unit		*****	*****
Basic I/O Units	Input Unit	"I" followed by number of input points	I8, I16, I32, I48, I64, I96
	Output Unit	"O" followed by number of output points	O8, O16, O32, O48, O64, O96
	Mixed I/O Unit	"M" followed by number of I/O points	M8, M16, M32, M48, M64, M96
	Interrupt Input Unit	"INT" followed by the Interrupt Input Unit number. (Interrupt Input Units can be used only as normal Input Units for the CS1D.)	INT0, INT1
Special I/O Unit		"SIO" followed by the unit number	SIO00, SIO95
CPU Bus Units	Ethernet Unit	"ET" followed by the unit number	ET00
	CS1D Ethernet Unit	"ED" followed by the unit number	ED10 (See note 2.)
	Controller Link Unit	"NS" followed by the unit number	NS12 (See note 1.)
	SYSMAC Link Unit	"SL" followed by the unit number	SL11
	Serial Communications Unit	"SC" followed by the unit number	SC13
	DeviceNet Unit	"DN" followed by the unit number	DN14
	Loop Control Unit	"LC" followed by the unit number	LC15

Note

1. If a Duplex Controller Link Unit is used, "a" will be added to the end of the display for the active Unit and "s" will be added for the standby Unit. For example, "NS12a" would be a Controller Link Unit with a unit number of 12 functioning as the active Unit. "NS12s" would be the same Unit functioning as the standby Unit.
2. When using duplex Ethernet Units (CS1D Ethernet Units), a "p" will be added to the end of the unit type for the primary Unit and an "s" will be added for the secondary Unit.
   Examples:
   ED10p: The primary CS1D Ethernet Unit set to unit number 10
   ED10s: The second CS1D Ethernet Unit set to unit number 10

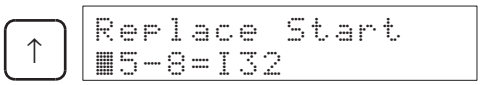
11-4-2 Replacing More than One Unit at a Time

The PLC Setup can be set to enable online replacement of more than one Unit at a time.

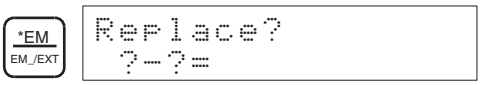
This operation is possible only from the Programming Console.

Starting Online Replacement for Multiple Units

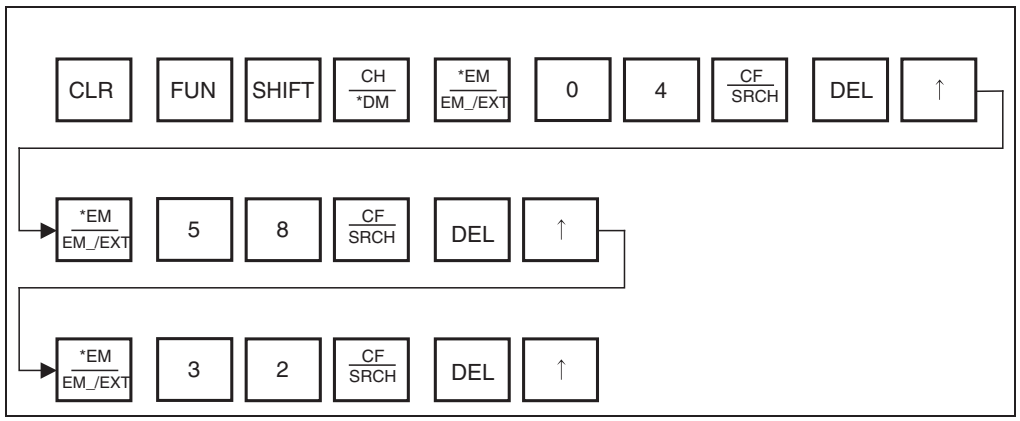
Another Unit can be replaced after completing steps *1.* to *5.* in the basic procedure by pressing the CLR Key and then repeating steps *1.* to *5.*, or by pressing the EXT Key and then using the following procedure.



If the EXT Key is pressed in the status shown above, the display will appear to enable inputting another rack number and slot number.

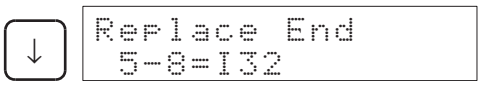


The following example shows the key inputs for replacing Units online in slot 4 or Rack 0, slot 5 in Rack 8, and slot 2 in Rack 3.

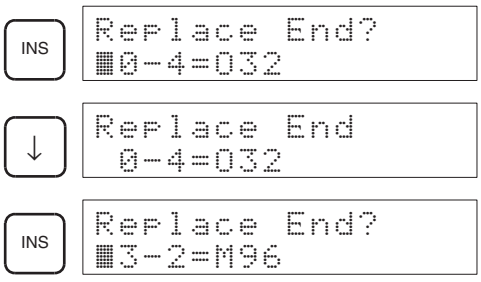


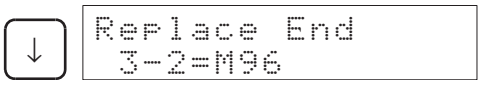
Ending Replacement of Multiple Units

When the last Unit has been replaced and the online replacement procedure for it has been completed, the replacement procedures for the remaining Units can be ended either by pressing the CLR Key and then performing steps *1.* through *3.* and then step *7.* in the basic procedure, or by using the following procedure to end the replacement procedures directly using step *7.*

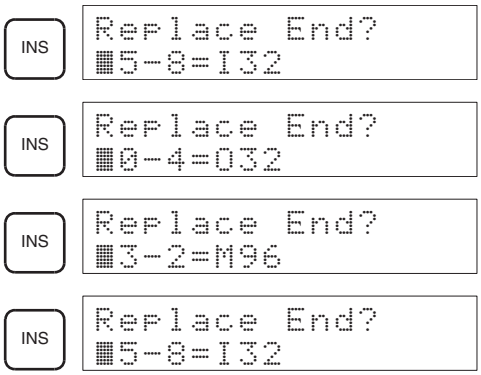


If the INS Key is pressed in the status shown above, the following displays will appear allowing you to end the replacement procedures for all Units for which replacement has been started.





When the online replacement procedure for the last Unit has been ended, the display will not change even if the INS Key is pressed. If the INS Key is pressed without pressing the Down Key, the Units for which online replacement procedures have been started can be displayed without ending the procedures.

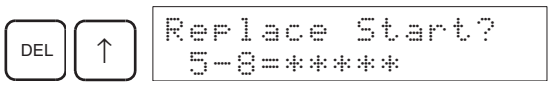


11-4-3 Error Displays

Errors can occur when starting and stopping online replacement procedures. These are described in this section.

Starting Online Replacement

Specifying an Empty Slot



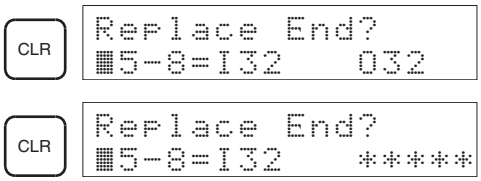
Error Displays when Ending Online Replacement

- The following display will appear if a different type of Unit is mounted from the one that was removed.
- It is also displayed if the unit number (UNIT No./MACH No.) is different from the Unit that was removed.

- The following display will appear if the node number is different from the Unit that was removed (for online replacement of a Duplex Controller Link Unit or Duplex Ethernet Unit).

The CLR Key can be pressed to display the Unit registered in the I/O tables and the Unit that was mounted.

The display on the left is the registered Unit and the display on the right is the Unit that is currently mounted.



11-4-4 Online Replacement Precautions for Special I/O and CPU Bus Units

Special I/O Units and CPU Bus Units have hardware switches, software switches, and parameters, all of which help to control Unit operation. When a Unit is replaced, all of these must be set to the same status as the Unit that was replaced.

The specific settings that must be set depend on the type of Unit that is being used. Refer to the operation manual for the specific Unit for details on these settings.

⚠ **Caution** Before replacing a Unit online, always disable the operation of all connected external devices before starting the replacement procedure. Unexpected outputs from the Unit being replaced may result in unexpected operation of controlled devices or systems.

⚠ **Caution** If an Output Unit is replaced and ON status is held in memory for that Unit, the corresponding output will turn ON as soon as the online replacement operation has been completed. Confirm system safety in advance.

⚠ **Caution** If the settings in the new Unit are not the same as those in the Unit that was replaced, unexpected operation may result possibly causing an accident. Replace a Unit only after making sure that all settings are the same.

Refer to the operation manual of the specific Unit for details on any Units not listed in the following tables and follow all replacements provided in the manual.

Unit Settings and Replacement Precautions

Special I/O Units

Name and model number	Settings			Precautions
	Hardware settings on Special I/O Unit	Settings stored in CPU Unit	Settings stored in Special I/O Unit	
Analog Input Units CS1W-AD041 CS1W-AD041-V1 CS1W-AD081 CS1W-AD081-V1	Unit number (rotary switch)	Settings in allocated DM Area words	None	Refer to the operation manual for replacement procedures, and observe the following precautions. 1) Turn OFF the power supply to all external devices connected to the Unit before starting the replacement procedure. 2) Set the same unit number on the new Unit as was set on the Unit being replaced. 3) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit.
Analog Output Units CS1W-DA041 CS1W-DA08V CS1W-DA08C	Unit number (rotary switch)	Settings in allocated DM Area words	None	
Analog I/O Unit CS1W-MAD44	Unit number (rotary switch)	Settings in allocated DM Area words	None	
Process I/O Units CS1W-PTS01-V1 CS1W-PTS02/03 CS1W-PTW01 CS1W-PD01 CS1W-PMV01/02 CS1W-PTR01/02 CS1W-PPS01	Unit number (rotary switch)	Settings in allocated DM Area words	None	
Customizable Counter Units CS1W-HIO01-V1 CS1W-HCP22-V1 CS1W-HCA22-V1 CS1W-HCA12-V1	Unit number (rotary switch)	Settings in allocated DM Area words	In flash memory: • User program • General-purpose read-only DM Area • Unit functions setting area • Expansion instructions information • Ladder library information	Refer to the Customizable Counter Unit operation manual for replacement procedures, and observe the following precautions. 1) Turn OFF the power supply to all external devices connected to the Unit before starting the replacement procedure. 2) Stop Unit operation before starting the replacement procedure. 3) Set the same unit number on the new Unit as was set on the Unit being replaced. 4) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit. 5) Use one of the following methods to transfer the same data to the flash memory in the Special I/O Unit as was in the Unit that was replaced: a) Use the simple backup function or b) Transfer the user program and required data from the CX-Programmer. **Note** The version 1 (-V1) Customizable Counter Units support a simple backup function. If the data stored in the flash memory in the Unit is saved to a Memory Card in advance and the Memory Card is inserted into the CPU Unit, the Memory Card can be used after online replacement to automatically transfer the required data to the new Unit. (See note 1 following next table.) Pre-V1 versions of the Units do not support the simple backup operation. Use the CX-Programmer to either transfer the required data or set it again to the same settings as the Unit being replaced. (See note 2 following next table.)
High-speed Counter Units (2 or 4 axes) CS1W-CT021 CS1W-CT041	Unit number (rotary switch)	Settings in allocated DM Area words	None	Refer to the High-speed Counter Unit operation manual for replacement procedures, and observe the following precautions. 1) Turn OFF the power supply to all external devices connected to the Unit before starting the replacement procedure. 2) Set the same unit number on the new Unit as was set on the Unit being replaced. 3) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit. **Note** If the gate open operation is being performed with bit operations for the following bits, turn the bits ON after completing online replacement so that the bits are effective: Bit 00 of CIO n+2, Bit 00 of CIO n+5, Bit 00 of CIO n+8, and Bit 00 of CIO n+11.

Name and model number	Settings			Precautions
	Hardware settings on Special I/O Unit	Settings stored in CPU Unit	Settings stored in Special I/O Unit	
GP-IB Interface Unit CS1W-GPI01	Unit number (rotary switch)	Settings in allocated DM Area words	None	Refer to the GP-IB Unit operation manual for replacement procedures, and observe the following precautions. 1) Turn OFF the power supply to all external devices connected to the Unit before starting the replacement procedure. 2) Set the same unit number on the new Unit as was set on the Unit being replaced. 3) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit.
Position Control Units CS1W-NC113 CS1W-NC133 CS1W-NC213 CS1W-NC233 CS1W-NC413 CS1W-NC433	Unit number (rotary switch)	Settings in allocated DM Area words There may also be settings in user-specified DM/EM Area words.	In flash memory: • Axis parameters • Sequence data • Speed data • Acceleration/deceleration data • Dwell data • Zone data	Refer to the Position Control Unit operation manual for replacement procedures, and observe the following precautions. 1) Turn OFF the power supply to all external devices connected to the Unit before starting the replacement procedure. 2) Set the same unit number on the new Unit as was set on the Unit being replaced. 3) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit. 4) Write the same parameters as the Unit being replaced to flash memory in the new Unit in advance by downloading them from the CX-Position. (See note 2 following next table.)
Motion Control Units CS1W-MC421-V1 CS1W-MD221-V1	Unit number (rotary switch)	Settings in allocated DM Area words	In flash memory (if save is performed): • System parameters • Position data • G-language program	Refer to the Motion Control Unit operation manual for replacement procedures, and observe the following precautions. 1) Turn OFF the power supply to all external devices connected to the Unit before starting the replacement procedure. 2) Set the same unit number on the new Unit as was set on the Unit being replaced. 3) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit. 4) Write the same parameters as the Unit being replaced to flash memory in the new Unit in advance by downloading them from the CX-Motion. (See note 2 following next table.)
ID Sensor Units CS1W-V600C11 CS1W-V600C12	Unit number (rotary switch)	Settings in allocated DM Area words	None	Refer to the I/O Sensor Unit operation manual for replacement procedures, and observe the following precautions. 1) Turn OFF the power supply to all external devices connected to the Unit before starting the replacement procedure. 2) Set the same unit number on the new Unit as was set on the Unit being replaced. 3) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit.

CPU Bus Units

Name and model number	Settings			Precautions
	Hardware settings on CPU Bus Unit	Settings stored in CPU Unit	Settings stored in CPU Bus Unit	
Optical-ring Controller Link Units CS1W-CLK12-V1 CS1W-CLK52-V1 CS1W-CLK13 CS1W-CLK53	Unit number (rotary switch) Node address (rotary switch)	In CPU Bus Setup Area: • Data link tables • Network parameters • Routing tables In allocated DM Area words: • Data link settings, others	None	Refer to the procedure in the Controller Link Unit operation manual for replacing the Unit while the system is still operating, and observe the following precautions. 1) The external power supply must be turned OFF. If another node is sharing the power supply so that the power supply cannot be turned OFF only to the Unit being replaced, a power interruption will be detected, causing a communications error. Confirm that the power supply can be turned OFF safety. 2) When the optical cable is removed, a disconnection of the line will be detected at other nodes. 3) If a Duplex Communications Unit is being used, the standby Unit will take over and continue communications. (Pre-V1 Unit do not support duplex operation and cannot continue communications when replaced. Communications, however, will be continued at the other nodes.) 4) Set the same unit number and node address on the new Unit as were set on the Unit being replaced. 5) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit.
Optical-bus Controller Link Units CS1W-CLK11	Unit number (rotary switch) Node address (rotary switch)	In CPU Bus Setup Area: • Data link tables • Network parameters • Routing tables In allocated DM Area words: • Data link settings, others	None	Refer to the Controller Link Unit operation manual for replacement procedures and observe the following precautions. 1) The external power supply must be turned OFF to all nodes before a Unit can be replaced. Communications will stop for all nodes. 2) Set the same unit number and node address on the new Unit as were set on the Unit being replaced. 3) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit.
Wired Controller Link Units CS1W-CLK21-V1	Unit number (rotary switch) Node address (rotary switch) Baud rate (DIP switch) Terminating resistance (slide switch)	In CPU Bus Setup Area: • Data link tables • Network parameters • Routing tables In allocated DM Area words: • Data link settings, others	None	Refer to the Controller Link Unit operation manual for replacement procedures and observe the following precautions. 1) If a CJ1W-TB101 Relay Terminal Block is being used, a Unit can be replaced without turning OFF the power supply to all nodes in the network. Communications will stop for the node of the Unit being replaced. 2) If a Relay Terminal Block is not being used or if the node of the Unit being replaced is at the end of the network, power must be turned OFF to all nodes on the network before replacement is possible. Communications will stop for all nodes. 3) Set the same unit number, node address, baud rate, and terminating resistance setting on the new Unit as were set on the Unit being replaced. 4) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit.
SYSMAC Link Units CS1W-SLK21 (coaxial) CS1W-SLK11 (optical)	Unit number (rotary switch) Node address (rotary switch)	In CPU Bus Setup Area: • Data link tables • Network parameters • Routing tables In allocated DM Area words: • Data link settings, others	None	Refer to the SYSMAC Link Unit operation manual for replacement procedures and observe the following precautions. 1) Turn OFF the power supply to all nodes in the network before replacing the Unit. Because the power is turned OFF to all nodes during online replacement, communications cannot be continued. 2) Set the same unit number and node address on the new Unit as were set on the Unit being replaced. 3) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit.

Name and model number	Settings			Precautions
	Hardware settings on CPU Bus Unit	Settings stored in CPU Unit	Settings stored in CPU Bus Unit	
Ethernet Units CS1W-ETN01 CS1W-ETN11	Unit number (rotary switch) Node address (rotary switch) IP address (rotary switch)	In CPU Bus Setup Area: Network settings • Routing tables In allocated DM Area words: • Various settings	None	Refer to the Ethernet Unit operation manual for replacement procedures and observe the following precautions. 1) Turn OFF the power supply connected to the Unit before starting the replacement procedure. 2) Set the same unit number, node address, and I/P address on the new Unit as were set on the Unit being replaced. 3) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit.
Ethernet units CS1W-ETN21 CS1D-ETN21D	Unit number (rotary switch) Node address (rotary switch)	In CPU Bus Setup Area: • Network settings (e.g., IP address) • Routing tables In allocated DM Area words: • Various settings	None	Refer to the Ethernet Unit operation manual for replacement procedures and observe the following precautions. 1) Set the same unit number and node address, on the new Unit as were set on the Unit being replaced. 2) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit.
Serial Communications Unit CS1W-SCU21-V1 CS1W-SCU31-V1	Unit number (rotary switch)	In allocated DM Area words: • Baud rate, others	In flash memory: • Protocol macro data	Refer to the Serial Communications Unit operation manual for replacement procedures, and observe the following precautions. 1) Turn OFF the power supply to all external devices connected to the Unit before starting the replacement procedure. 2) Set the same unit number on the new Unit as was set on the Unit being replaced. 3) When the new Unit has been mounted and the online replacement operation has been completed for it, the settings stored in the CPU Unit will be automatically transferred to the new Unit. 4) If protocol macros are being used, use one of the following methods to transfer the same data to the flash memory in the Special I/O Unit as was in the Unit that was replaced: a) Use the simple backup function or b) Transfer the required data from the CX-Protocol. **Note** The version 1 (-V1) Serial Communications Units support a simple backup function. If the data stored in the flash memory in the Unit is saved to a Memory Card in advance and the Memory Card is inserted into the CPU Unit, the Memory Card can be used after online replacement to automatically transfer the required data to the new Unit. (See note 1.) Pre-V1 versions of the Units do not support the simple backup operation. Use the CX-Protocol to either transfer the required data or set it again to the same settings as the Unit being replaced. (See note 2.)

Name and model number	Settings			Precautions
	Hardware settings on CPU Bus Unit	Settings stored in CPU Unit	Settings stored in CPU Bus Unit	
DeviceNet Unit CS1W-DRM21-V1	Unit number (rotary switch) Node address (rotary switch) Baud rate (rotary switch) Continuation of remote I/O for communications error (master, DIP switch) Hold/Clear of remote I/O for communications error (slave, DIP switch)	In CPU Bus Setup Area: • Routing tables (when required)	In non-volatile memory: • Scan list (master) • Communications cycle time settings (master) • Slave scan list (slave) • Message monitor time list (for message communications) • Master/Slave function enable settings	Refer to the DeviceNet Unit operation manual for replacement procedures, and observe the following precautions. **When Using Master Function** 1) All parameters are stored in non-volatile memory in the Unit. Write all of these parameters to the Unit before starting the replacement procedure by downloading them from the DeviceNet Configurator. (See note 2.) 2) Remote I/O communications will stop when the DeviceNet communications connector is removed and communications errors will occur at all the slaves. 3) At this point, a network power error can be confirmed at the CPU Unit. The status of all inputs to the CPU Unit from the DeviceNet Unit will be held by the CPU Unit. 4) The outputs from Output Slaves will be either held or cleared when the communications error occurs, depending on the settings at the slaves. 5) Remote I/O communications will automatically recover when the DeviceNet communications connector is reconnected after the replacement operation. After recovery, the status of outputs from Output Slaves will be controlled again by the status of the output words allocated to them in the CPU Unit. **When Using Slave Function** 1) Just like the master function, all parameters are stored in non-volatile memory in the Unit. Write all of these parameters to the Unit before starting the replacement procedure by downloading them from the DeviceNet Configurator. (See note 2.) 2) A communications error will occur at the master when the DeviceNet communications connector is removed. Depending on the settings of the master, all I/O communications may stop. Check the settings and operation of the master. 3) A network power error can be confirmed at the CPU Unit. The status of all inputs to the slave (outputs from the CPU Unit will be held or cleared according to the setting on the DIP switch. 4) If the master is set so that remote I/O communications will not stop, only communications for the Unit being replaced will stop and normal communications will be possible for other slaves. Normal communications will recover when the DeviceNet communications connector is reconnected. 5) If the master is set so that all remote I/O communications stop, then restarting communications must be specified at the master after the Unit is replaced and the communications connector is reconnected. 6) Set the same unit number on the new Unit as was set on the Unit being replaced. **Note** The version 1 (-V1) DeviceNet Unit (to be released soon) will support a simple backup function. If the data stored in the non-volatile memory in the Unit is saved to a Memory Card in advance and the Memory Card is inserted into the CPU Unit, the Memory Card can be used after online replacement to automatically transfer the required data to the new Unit. (See note 1.) The remaining precautions given above will still apply.
Loop Control Unit CS1W-LC001	Unit number (rotary switch)	In allocated DM Area words: None	In battery-backup RAM or flash memory (if save is performed for flash memory): • Function block data	Refer to the Loop Control Unit operation manual for replacement procedures, and observe the following precautions. 1) Turn OFF the power supply to all external devices connected to the Unit before starting the replacement procedure. 2) Set the same unit number on the new Unit as was set on the Unit being replaced. 3) Write the same function block data as the previous Unit to the new Unit and save it to flash memory in advance by downloading them from the CX-Process Tool. (See note 2.)

Note

1. Refer to the Programming Manual (W339), *5-2-6 Simple Backup Operation* for details on the simple backup function. If the Memory Card is inserted in the new Unit, the data on the Memory Card will be automatically transferred to the Unit when the online replacement operation is completed.
2. To write parameters (such as the settings stored in the Special I/O Unit or CPU Bus Unit) to the Unit in advance for replacement, it is necessary to prepare separately a system consisting of a CS-series CPU Unit, CPU Backplane, and Power Supply Unit. Mount the Unit to be used for replacement to this Backplane and download the parameters to it from a Programming Device.

Note CS1W-PNT21 units can be used in the configuration with CS1D (duplex system) but do NOT support HOT SWAPPING function.
If you insert PROFINET IO Controller CS1W-PNT21 on the PLC backplane while the CS1D (duplex) PLC system is in operation (i.e. as part of an online replacement procedure), "I/O Bus error" will occur in the CS1D CPU unit, and program execution will stop. Whether or not a programming device is used at the time has no effect on this.
If the problem occurs, the system will resume normal operation after switching OFF/ON the power supply of the PLC system.
(CS1W-PNT21 is a spcific product released in a specific area.)

11-4-5 Online Replacement without a Programming Device

When the Unit Removal without a Programming Device or Removal/Addition of Units without a Programming Device function is enabled in the PLC Setup, a Unit can be replaced without using the CX-Programmer or a Programming Console.

Note The following table shows the CPU Units that support these functions.

Unit version	Unit Removal without a Programming Device or	Removal/Addition of Units without a Programming Device
Unit version 1.1 or earlier	Not supported (See note 1.)	Not supported (See note 1.)
Unit version 1.2	Supported	Not supported (See note 2.)
Unit version 1.3 or later	Supported (See note 3.)	Supported (See note 3.) (Duplex CPU, Dual I/O Expansion Systems only)

Note

1. If these functions are set, it will not operate. An “I/O bus error” will occur and PLC will stop if the Unit is removed without using a Programming Device.
2. If just the “Removal/Addition of Units without a Programming Device function” is set in a CPU Unit, it will not operate. An “I/O bus error” will occur and PLC will stop if the Unit is removed without using a Programming Device.
3. If both functions are set in a CPU Unit operating in a Duplex CPU Dual Expansion System, the “Removal/Addition of Units without a Programming Device function” will be enabled. If the system is a a Duplex CPU Single I/O Expansion System, the Unit Removal without a Programming Device will be enabled. If the system is a CPU Duplex Single Expansion System, the “Unit Removal without a Programming Device function” will be enabled. If only the “Removal/Addition of Units without a Programming Device function” is set for a CPU Duplex Single Expansion System, the Unit

will operate according to the "Unit Removal without a Programming Device function."

A Programming Device can be used for online replacement even if one of these functions is enabled. Two or more Units can be removed at one time with this setting.

Note When two or more Units are being replaced at one time, incorrect operation may occur.

Previously, if a Unit was removed or failed, an I/O bus error will occur and the PLC (CPU Unit) will stop operating, but this function causes the I/O bus error to be treated as a non-fatal error so the PLC will continue operating.

Note

1. In a Single CPU System or Duplex CPU Single I/O Expansion System, a fatal error will occur if another major component (such as a Backplane, Expansion Rack Cable, Duplex Unit, or Long-distance Expansion I/O Rack) is removed or fails. In a Duplex CPU Dual I/O Expansion System, a fatal error will occur if a Backplane is removed or fails.
2. When a Unit has been removed during operation without a PLC Programming Device (CX-Programmer or a Programming Console), data transferred from the removed Unit to the CPU Unit may be invalid. If an invalid data transfer will adversely affect the system, use a Programming Device to replace the Unit online.
3. When the Unit Removal without a Programming Device or Removal/Addition of Units without a Programming Device function is enabled in the PLC Setup and a Special I/O Unit has been removed, the Special I/O Unit Area words allocated to that Unit for data transfer (to and from the CPU Unit) will be cleared. If the loss of the Special I/O Unit Area data will adversely affect the system, disable the Unit Removal without a Programming Device or Removal/Addition of Units without a Programming Device function in the PLC Setup and use a Programming Device to replace the Unit online. (When a Programming Device is used to replace the Unit online, the data in the Special I/O Unit Area is retained while the Unit is removed.)
4. An I/O bus error, which can be caused by a Unit malfunction, is normally a fatal error that stops operation. When the Unit Removal without a Programming Device or Removal/Addition of Units without a Programming Device function is enabled in the PLC Setup, the I/O bus error will be treated as a non-fatal error and PLC (CPU Unit) will not stop operating. If there are any Units that will adversely affect the system if an I/O bus error occurs, do not enable the Unit Removal without a Programming Device or Removal/Addition of Units without a Programming Device function in the PLC Setup.

Differences between the Online Unit Removal Functions

The following table shows the differences between the Unit Removal without a Programming Device or Removal/Addition of Units without a Programming Device function.

Status change	Unit Removal without a Programming Device function	Removal/Addition of Units without a Programming Device function
Unit removal	A Programming Device is not required. A non-fatal Unit error will occur in the Unit being replaced.	A Programming Device is not required. A Unit error will not occur. (See note.)
Unit addition	The Online Replacement Completed Bit (A80215) will go ON.	A Programming Device is not required.
Unit failure	A non-fatal Unit error will occur.	A non-fatal Unit error will occur.

Note A Unit error may occur if the Unit is removed slowly.

Steps required before Starting Online Replacement without a Programming Device

The following steps must be performed in advance before replacing a Unit online without a PLC Programming Device.

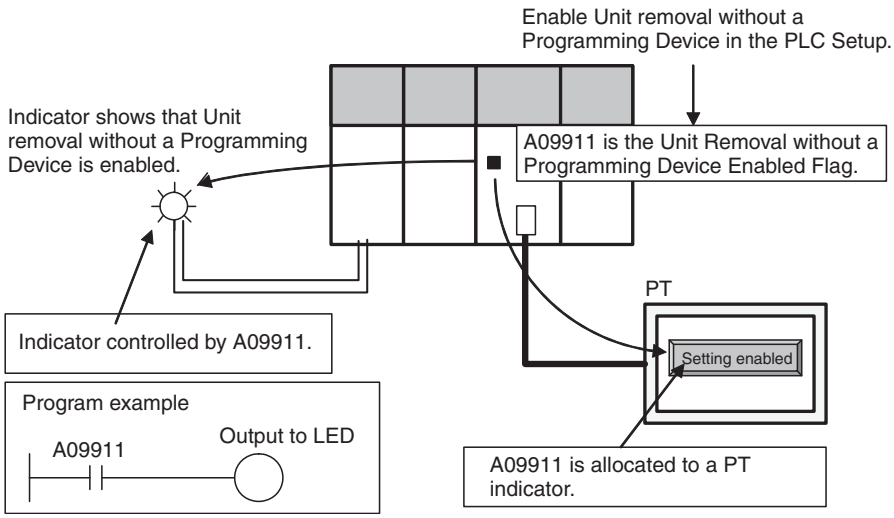
Enable Online Replacement without a Programming Device

The Unit Removal without a Programming Device or Removal/Addition of Units without a Programming Device function must be enabled in the PLC Setup in order to remove a Unit without a PLC Programming Device.

Use a Programming Console to set the appropriate PLC Setup address.

Note Before removing a Unit during operation without a PLC Programming Device (CX-Programmer or a Programming Console), always confirm that the Unit Removal without a Programming Device or Removal/Addition of Units without a Programming Device function has been enabled in the PLC Setup. If a Unit is mistakenly removed without enabling the function in the PLC Setup, an I/O bus error will occur and the PLC (CPU Unit) will stop operating.
When this function is enabled in the PLC Setup, the Unit Replacement without a Programming Device Enabled Flag (A09911) will be ON. This flag can be used to confirm that the required PLC Setup setting has been made.

Example



Maintenance Start Bit (A80015)

When the Unit Removal without a Programming Device function is selected and a Unit is removed without a PLC Programming Device, one of the following non-fatal errors will be generated depending on the type of Unit that was removed. The PLC (CPU Unit) will not stop operating even if one of these non-fatal errors occurs.

Unit type	Non-fatal error
Basic I/O Unit	Basic I/O Unit error
Special I/O Unit	Special I/O Unit error
CPU Bus Unit	CPU Bus Unit error

The Maintenance Start Bit is provided to prevent a non-fatal error from occurring even if a Unit is removed without a Programming Device.

When you don't want a non-fatal error to be generated, turn this bit ON before removing the Unit.

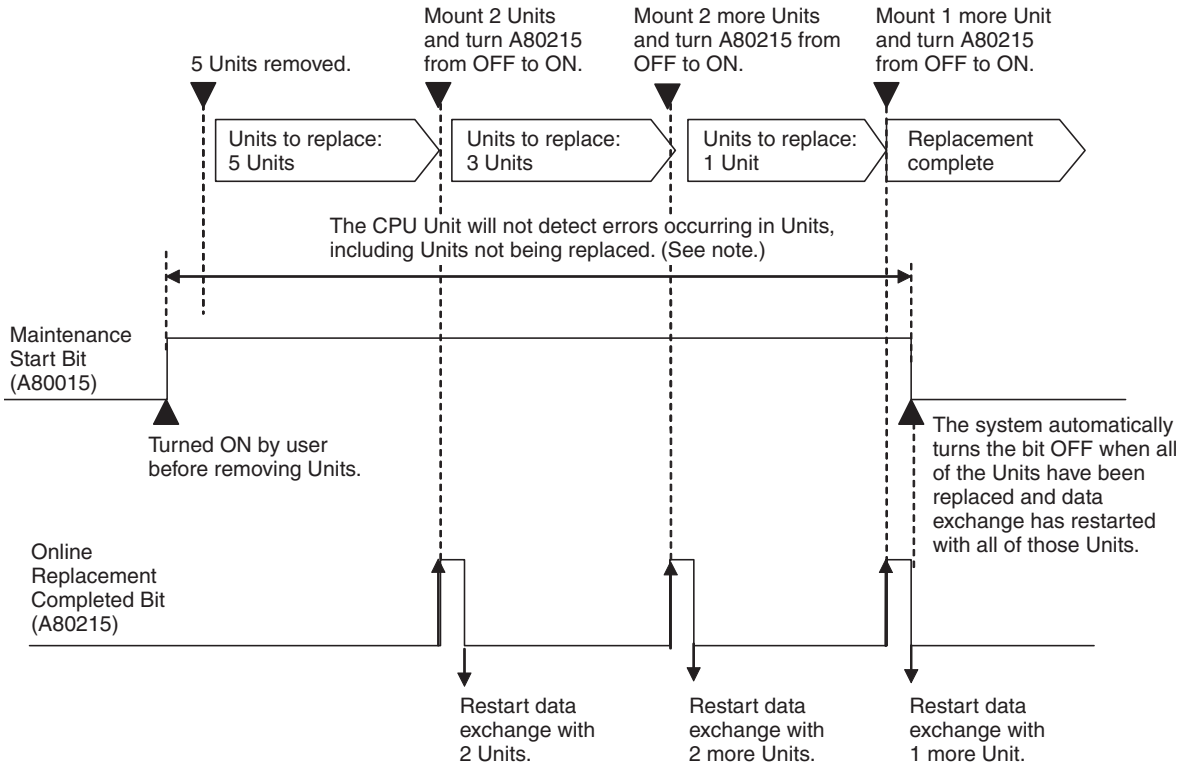
This bit can be turned ON externally (just like the Online Replacement Completed Bit) by allocating the bit to an external switch on an Input Unit and inputting the signal or turning ON the bit from a PT. (The bit can also be turned ON from the CX-Programmer or a Programming Console.)

Note Do not turn ON the Maintenance Start Bit (A80015) continuously from the ladder program or other source. As long as the Maintenance Start Bit is ON, errors will not be generated even if there are Unit malfunctions, so the system may be adversely affected.

The Maintenance Start Bit will be turned OFF automatically when the Online Replacement Completed Bit (A80215) is turned ON to restart data exchange between the replacement Unit and the CPU Unit.

When two or more Units have been removed and replacement Units are being added to the system in order, the Maintenance Start Bit will be turned OFF when data exchange is restarted with the last Unit that was replaced.

Example



Note If you want to detect errors in other Units before all of the Units have been replaced online, turn OFF the Maintenance Start Bit.

Online Replacement Completed Bit (A80215)

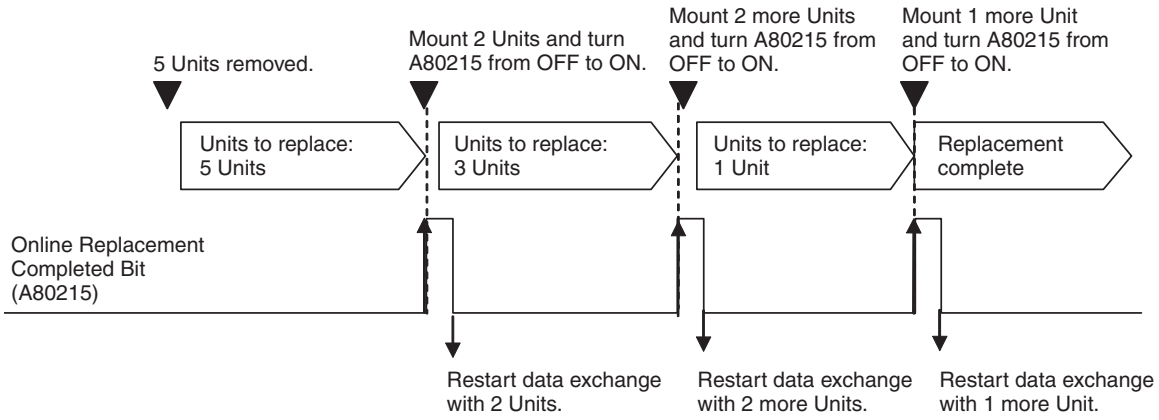
When the Unit Removal without a Programming Device function is selected and a Unit has been installed during operation without a Programming Device, the Online Replacement Completed Bit (A80215) must be turned ON in order to restart the data exchange between the replaced Unit and the CPU Unit.

When turning this bit ON externally, allocating the bit to an external switch or turn the bit ON from a PT. (The bit can also be turned ON from the CX-Programmer or a Programming Console.)

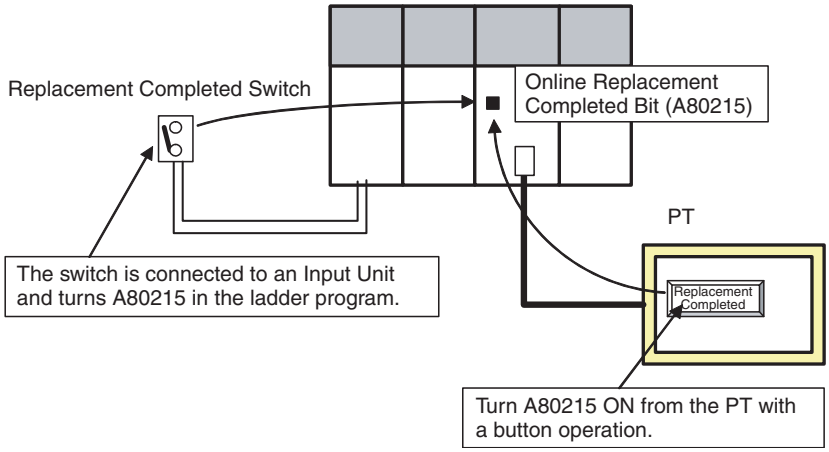
Note Do not turn ON the Online Replacement Completed Bit (A80215) continuously from the ladder program or other source. If the Unit is mounted while the Online Replacement Completed Bit is ON, the PLC (CPU Unit) may stop operating.

If two or more Units have been removed at one time, data exchange will restart only with the newly mounted Units when the Online Replacement Completed Bit is turned ON. Therefore, the Online Replacement Completed Bit must be turned ON each time that Units are mounted.

Example

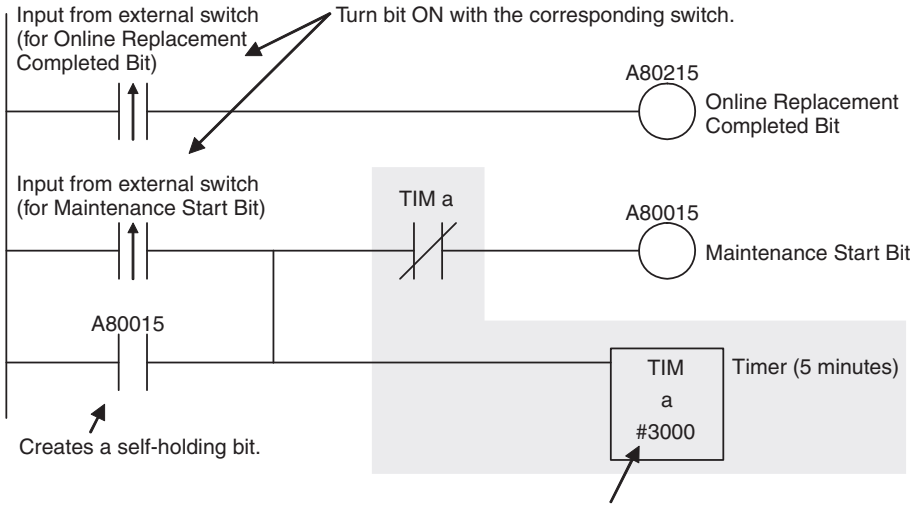


Example



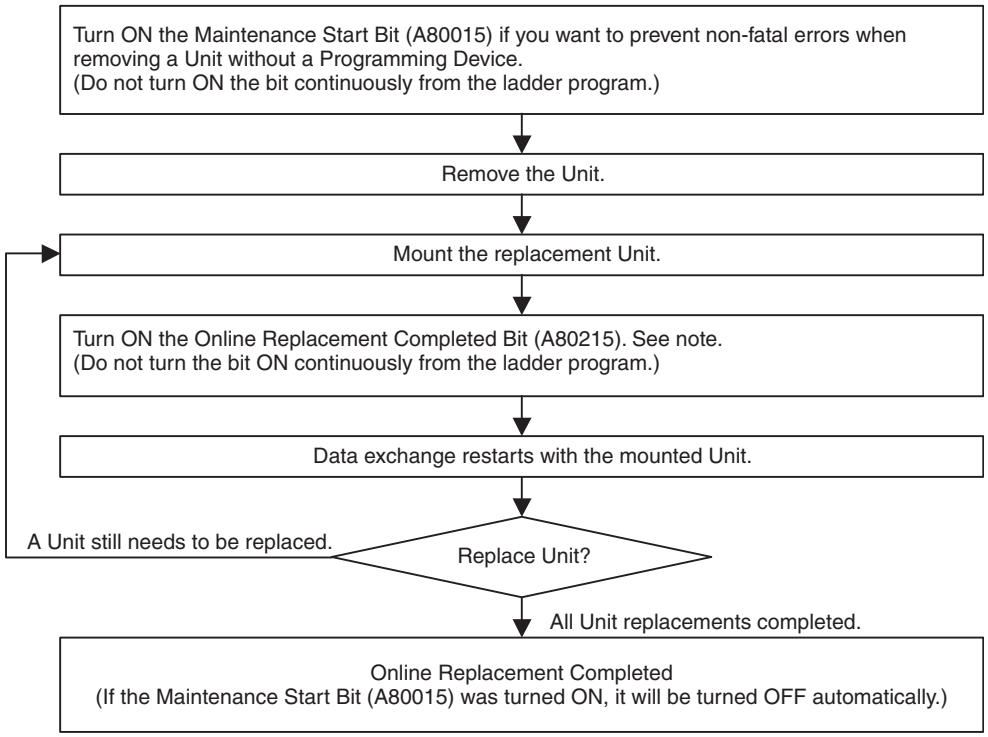
Ladder Programming for the Online Replacement Bit and Maintenance Start Bit

Example



Procedure for Online Replacement without a Programming Device

Flowchart of the Replacement Procedure



Note The Online Replacement Completed Flag is required only when the Unit Removal without a Programming Device function is being used. When the Removal/Addition of Units without a Programming Device function is being used, the data exchange is restarted automatically after the replacement Unit is mounted.

1,2,3... 1. Confirm that the Unit Removal without a Programming Device or the Removal/Addition of Units without a Programming Device function is enabled in the PLC Setup.

⚠ **Caution** Do not touch any of the terminals or terminal blocks while the power is being supplied. Doing so may result in electric shock.

Note a) If an Output Unit is being replaced, output ON status is retained and the outputs will go back ON as soon as online replacement is completed.

b) When a Unit has been removed during operation without a PLC Programming Device (CX-Programmer or a Programming Console), data transferred from the removed Unit to the CPU Unit may be invalid. If an invalid data transfer will adversely affect the system, use a Programming Device to replace the Unit online.

2. Remove the Unit that is being replaced.
   When the Unit Removal without a Programming Device function is selected, one of the following non-fatal errors will be generated at this point, depending on the type of Unit that was removed.

Unit type	Non-fatal error
Basic I/O Unit	Basic I/O Unit error
Special I/O Unit	Special I/O Unit error
CPU Bus Unit	CPU Bus Unit error

   Note a) These non-fatal errors will not be generated when the Removal/Addition of Units without a Programming Device function is selected, unless the Unit is removed or mounted slowly.

   b) If you don't want one of these non-fatal errors to be generated when removing a Unit without a Programming Device, turn ON the Maintenance Start Bit (A80015) before removing the Unit. When this bit is ON, the errors above will not occur when the Unit is removed.

   c) Do not turn ON the Maintenance Start Bit (A80015) continuously from the ladder program or other source. As long as the Maintenance Start Bit is ON, errors will not be generated even if there are Unit malfunctions, so the system may be adversely affected.

3. Replace the Unit.

   Note a) If an Output Unit is being replaced, output ON status is retained and the outputs will go back ON as soon as online replacement is completed.

   b) Replace the Unit with the same kind of Unit.

4. After the Unit is replaced, turn ON the Online Replacement Completed Bit (A80215). (This step is not required with the Removal/Addition of Units without a Programming Device function.)

   Note a) The Online Replacement Completed Flag is required only when the Unit Removal without a Programming Device function is being used. When the Removal/Addition of Units without a Programming Device function is being used, the data exchange is restarted automatically after the replacement Unit is mounted.

   b) When the Online Replacement Completed Bit (A80215) is turned ON, the replaced Unit will restart data exchange processing with the CPU Unit.
   When data exchange processing restarts, the Online Replacement Completed Bit (A80215) will turned OFF. At the same time, the Maintenance Start Bit (A80015) will be turned OFF automatically if it is ON.

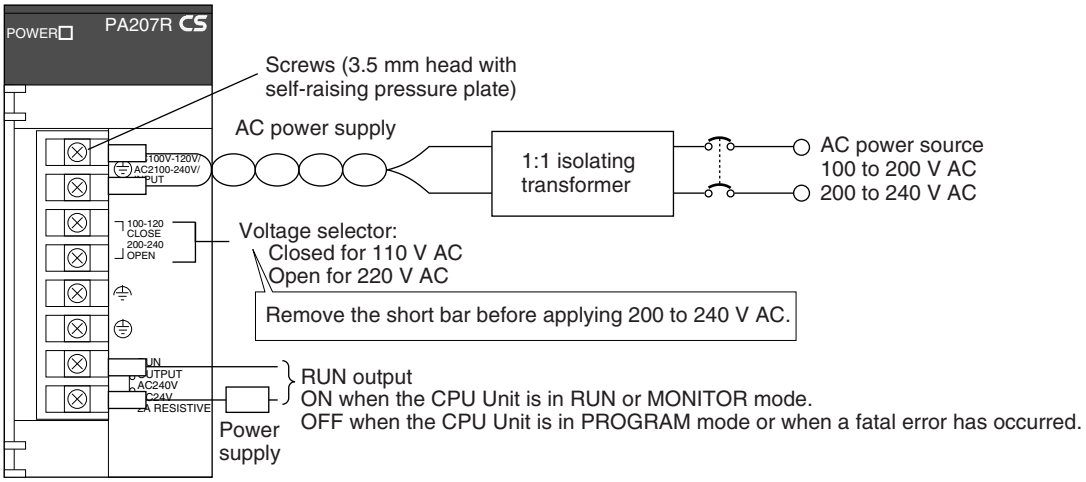
5. Check the replaced Unit's indicators and confirm that the Unit is operating properly to complete the replacement procedure.

11-5 Replacing Power Supply Unit

Use the following procedure to replace a Power Supply Unit when ever it is necessary to replace it, e.g., when an error is detected in the Power Supply Unit or for periodic maintenance.

1,2,3... 1. Turn OFF the power supply to the Unit to be replaced and remove the wiring. If the RUN output is being used in the external sequence circuits, either keep the RUN output shorted when removing the wires or prepare the sequence circuits so that they will be no adverse affects when the RUN output wires are removed.

⚠ **WARNING** Do not touch any live terminals. You will receive an electric shock.

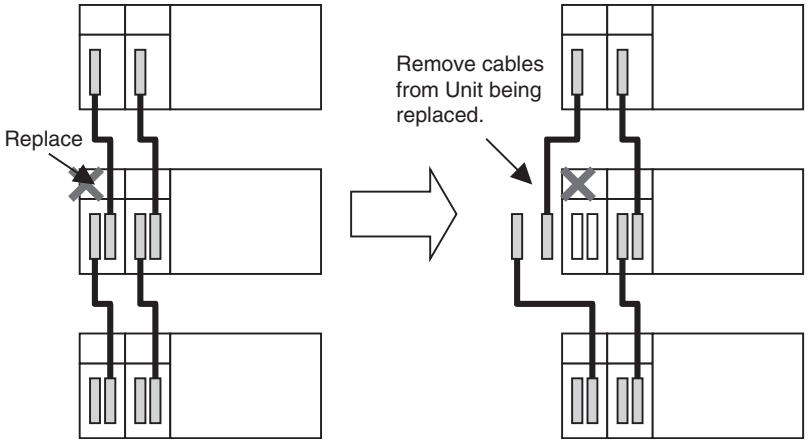


2. Remove the Power Supply Unit.
3. Mount a new Power Supply Unit, making sure it is the same model of CS1D Power Supply Unit.
4. Connect the wiring that was removed to the new Power Supply Unit.
5. Turn ON the power supply to the Unit and confirm that the POWER indicator lights.
6. Clear the error from the CPU Unit and check A31602 to confirm that there is no error in the Power Supply. If there is no error, then this completes the replacement procedure.

11-6 Replacement of Expansion Units

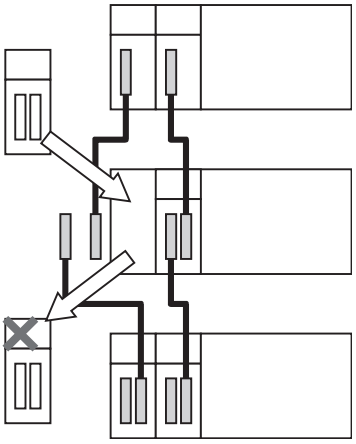
With a Duplex CPU Dual I/O Expansion System, a CS1D I/O Control Unit or CS1D I/O Interface Unit can be replaced when an error occurs in the Unit or during periodic maintenance. Use the following procedure to replace an Expansion Unit.

1,2,3... 1. Disconnect the Connecting Cables from the Unit being replaced.



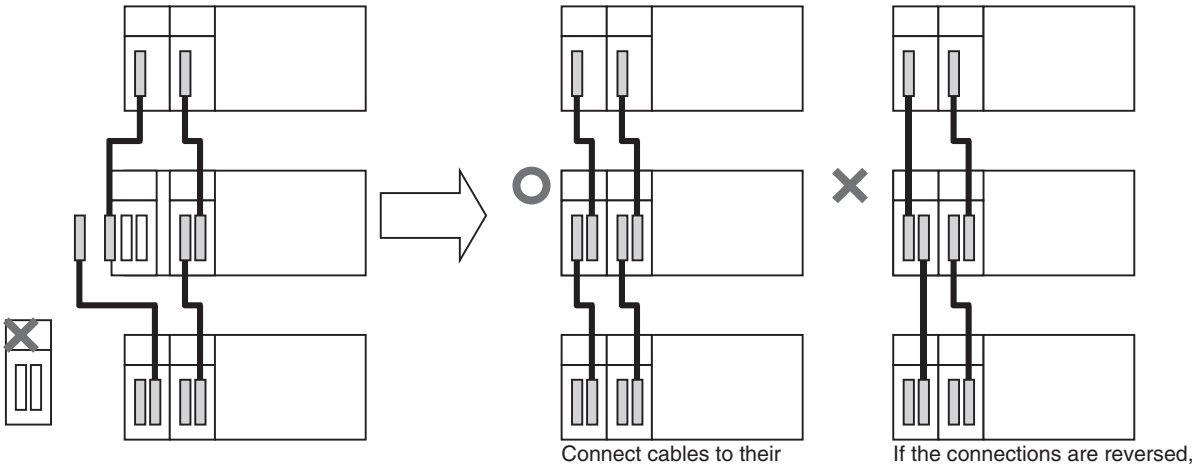
Note Before replacing an Expansion Unit, verify that the other Expansion Unit in the Rack is operating normally by checking the Duplex Communications Cable Error Flags in A270 as well as the LED Indicators on each Expansion Unit.

2. Remove the old Expansion Unit and mount the new Expansion Unit.



Note When removing and mounting a Unit, move the Unit smoothly so that it is not disconnected/reconnected repeatedly. After mounting a Unit, secure it by tightening the mounting screws to the proper torque.

3. Tighten the screws on the Expansion Unit, and once the Unit is secured, verify that the ERR indicator on the Expansion Unit is lit. Then connect the disconnected Expansion Cable to the new Expansion Unit. In this case, connect the Expansion Cable in its original condition.
Incorrect wiring may result in incorrect operation.



4. Verify that the Expansion Units RDY Indicator is lit and its ERR Indicator is not lit. If there are no errors, the Unit replacement is completed.

Note When replacing Expansion Units, system participation timing can be set manually when mounting the Units. This method is supported by CPU Units with production lot 101020 (i.e., produced October 20, 2010) or later.

Use the following procedure to perform replacement using this method.

1,2,3...

1. Write 11CF to A811 in the Auxiliary Area before performing Unit replacement.
   Note Writing to the Auxiliary Area can also be performed using a ladder program.
2. Disconnect the Expansion Cable from the Expansion Unit to be replaced.
3. Remove the Expansion Unit.
   Note Make sure that the Expansion Unit is not repeatedly removed and inserted.
4. Mount the new Expansion Unit and secure it by tightening the screws.
   Note The Expansion Unit will not operate in this condition. (Also, the indicators will not light.)
5. Wait for at least 5 seconds after mounting the Expansion Unit, and then turn ON Auxiliary Area Bit A812.15.
   Note This will start the mounting process (i.e., system participation) for the Expansion Unit.
6. The ERR indicator on the Expansion Unit will light. After it lights, connect the Expansion Cable.
7. Verify on the Expansion Unit that the RDY indicator is lit and the ERR indicator is not lit.
8. If there is no error, replacement has been completed.

11-7 Replacing the Duplex Unit

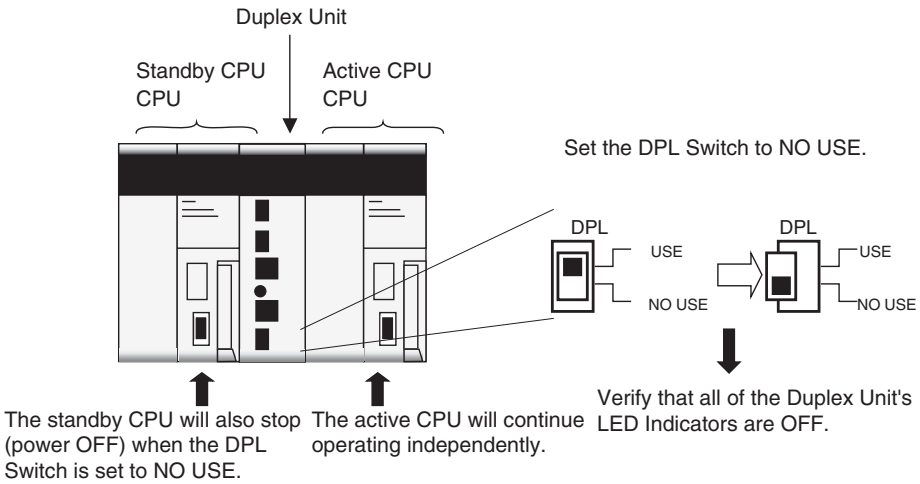
With a Duplex CPU Dual I/O Expansion System, the Duplex Unit can be replaced when an error occurs in the Unit or during periodic maintenance. Use the following procedure to replace an Duplex Unit.

Note The only Duplex Unit that can be replaced is the CS1D-DPL02D Duplex Unit, which is used in a Duplex CPU Dual I/O Expansion System. The CS1D-DPL01 Duplex Unit, which is used in a Duplex CPU Single I/O Expansion System, cannot be replaced. (The PLC will stop if a CS1D-DPL01 Duplex Unit is replaced.)

The CPU Unit will operate in Simplex Mode while the Duplex Unit is being replaced. If the active CPU Unit stops during replacement, the PLC will stop.

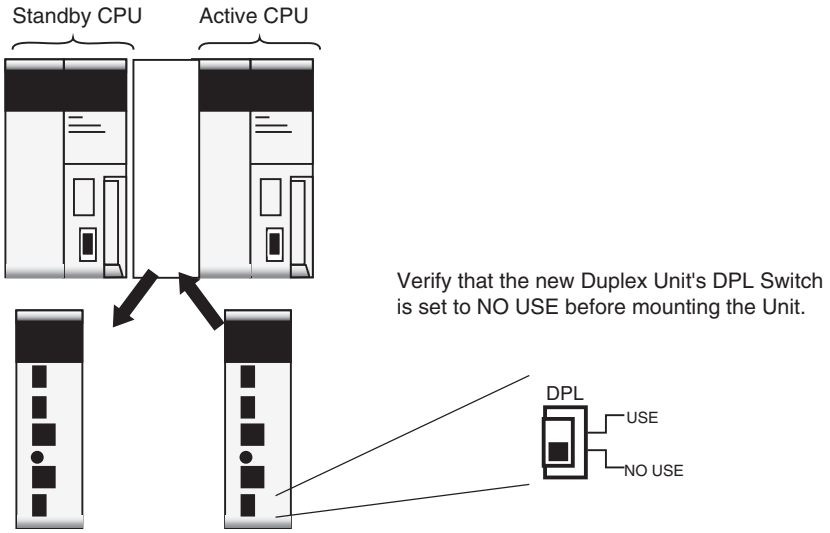
1,2,3... 1. Set the Duplex Unit's DPL Switch to NO USE.
When the DPL Switch is set to NO USE, the power supply to the Duplex Unit and standby CPU Unit will be turned OFF. All of the Duplex Unit indicators will be OFF (not lit).

⚠ **Caution** Before replacing the Duplex Unit, be sure to set the Duplex Unit's DPL Switch to NO USE. If the Unit is removed while the DPL Switch is set to USE, the CPU Backplane may fail or the PLC may operate unpredictably.



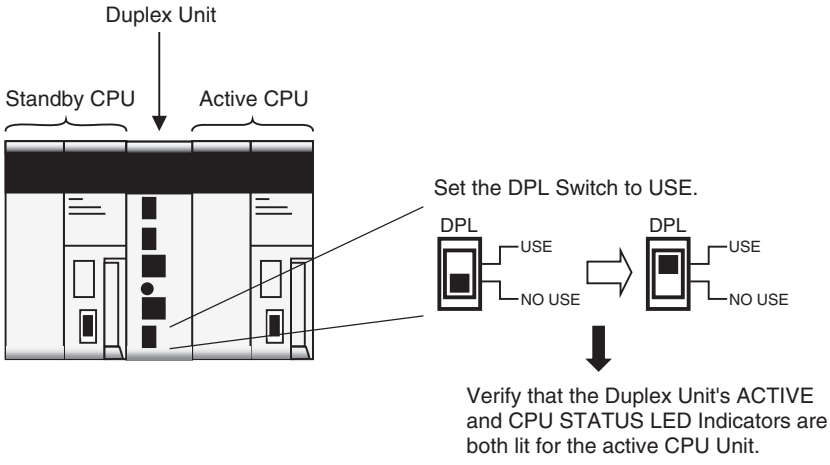
Note Once the DPL Switch is set to NO USE, the power to the Duplex Unit will remain OFF even if the DPL Switch is switched to USE unless the Duplex Unit has been removed. If you want to restart the same Duplex Unit, remove the Duplex Unit, mount it again, and proceed to step 4.

2. Remove the Duplex Unit. Verify that the new Duplex Unit's DPL Switch is set to NO USE and mount the new Duplex Unit.

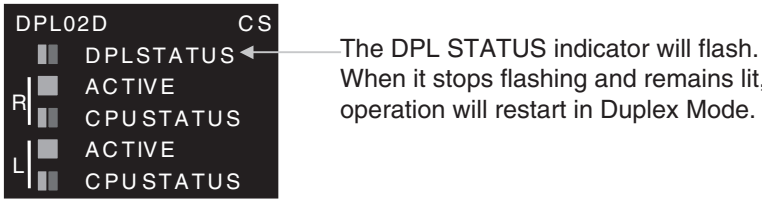


Note When removing and mounting the Unit, move the Unit smoothly so that it is not disconnected/reconnected repeatedly. After mounting the Unit, secure it by tightening the mounting screws to the proper torque.

3. Verify that the new Duplex Unit's LEFT CPU and RIGHT CPU Operating Switches are both set to USE (supply power to the CPU Units).
4. Set the Duplex Unit's DPL Switch to USE. Verify that the ACTIVE and CPU STATUS Indicators for the active CPU Unit are both lit on the front of the Duplex Unit.



5. Verify that the new Duplex Unit's Duplex Setting Switches (DPL SW) are set to DPL, and press the Initial (INIT) Button. When the Initial Button is pressed, the DPL STATUS and CPU STATUS Indicators flash green and then stay lit when operation restarts in Duplex Mode.



Appendix A
Specifications of Basic I/O Units and High-density I/O Units

List of Basic I/O Units

Input Units

Category	Name	Specifications	Model	Page
CS-series Basic Input Units with Terminal Blocks	AC Input Units	100 to 120 V AC/V DC, 16 inputs, 50/60 Hz	CS1W-IA111	485
		200 to 240 V AC, 16 inputs, 50/60 Hz	CS1W-IA211	485
	DC Input Units	24 V DC, 16 inputs	CS1W-ID211	486
	Interrupt Input Units	24 V DC, 16 inputs	CS1W-INT01 (See note.)	488
	High-speed Input Unit	24 V DC, 16 inputs	CS1W-IDP01	489
CS-series Basic Input Units with Connectors	DC Input Units	24 V DC, 32 inputs	CS1W-ID231	490
		24 V DC, 64 inputs	CS1W-ID261	491
		24 V DC, 96 inputs	CS1W-ID291	492
		Simultaneously ON 24-V DC inputs for CS1W-ID291/MD291/MD292		518

Note The Interrupt Input Unit can be used to input interrupts with a Single CPU System. With a Duplex CPU System, the Interrupt Input Unit will function only as a standard Input Unit.

Output Units

Category	Name	Specifications	Model	Page
CS-series Basic Outputs Units with Terminal Blocks	Relay Output Units	250V AC/24 V DC, 2 A; 120 V DC, 0.1 A; independent contacts, 8 outputs	CS1W-OC201	495
		250V AC/24 V DC, 2 A; 120 V DC, 0.1 A; 16 outputs	CS1W-OC211	494
		Relay contact outputs		519
	Triac Output Units	250 V AC, 1.2 A, with fuse burnout detection circuit, 8 outputs	CS1W-OA201	497
		250 V AC, 0.5 A, 16 outputs	CS1W-OA211	496
	Transistor Output Units, sinking	12 to 24 V DC, 0.5 A, 16 outputs	CS1W-OD211	498
		12 to 24 V DC, 0.5 A, 32 outputs	CS1W-OD231	499
		12 to 24 V DC, 0.3 A, 64 outputs	CS1W-OD261	500
		12 to 24 V DC, 0.1 A, with fuse burnout detection circuit, 96 outputs	CS1W-OD291	501
	Transistor Output Units, sourcing outputs	24 V DC, 0.5 A, load short-circuit protection, 16 outputs	CS1W-OD212	503
		Load short-circuit protection for CS1W-OD212/OD232/OD262/MD262		521
		24 V DC, 0.5 A, load short-circuit protection, 32 outputs	CS1W-OD232	504
		24 V DC, 0.3 A, load short-circuit protection, 64 outputs	CS1W-OD262	506
		24 V DC, with fuse burnout detection circuit, 0.1 A, 96 outputs	CS1W-OD292	507

Mixed I/O Units

Category	Name	Specifications	Model	Page
CS-series Basic I/O Units with Connectors	DC Input/Transistor Output Units	24 V DC inputs; 12 to 24 V DC, 0.3-A, sinking outputs; 32 inputs, 32 outputs	CS1W-MD261	509
		24 V DC inputs; 12 to 24 V DC, 0.1 A, sinking outputs with fuse burnout detection circuit; 48 inputs, 48 outputs	CS1W-MD291	511
		24 V DC inputs 24 V DC, 0.3 A, sourcing outputs with load short-circuit protection; 32 inputs, 32 outputs	CS1W-MD262	513
		24 V DC inputs 24 V DC, 0.1 A, sourcing outputs with fuse burnout detection circuit; 48 inputs, 48 outputs	CS1W-MD292	515
	TTL I/O Units	Inputs: 5 V DC, 3.5 mA Outputs: 5 V DC, 35 mA 32 inputs, 32 outputs	CS1W-MD561	517

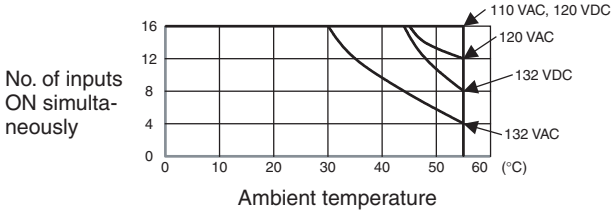
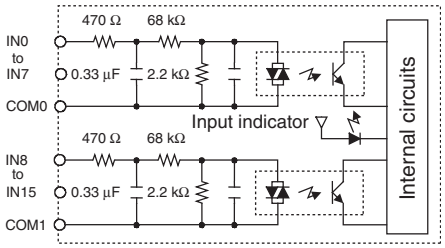
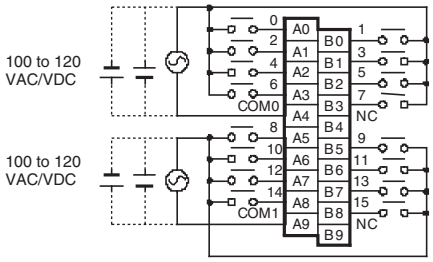
Reading Terminal Connection Diagrams

- I/O terminals in terminal connection diagrams are shown as viewed from the front panel of the Unit.
- Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on all Units.
- A0 to A20 and B0 to B20 are printed on the Units.

Basic I/O Units

Basic Input Units

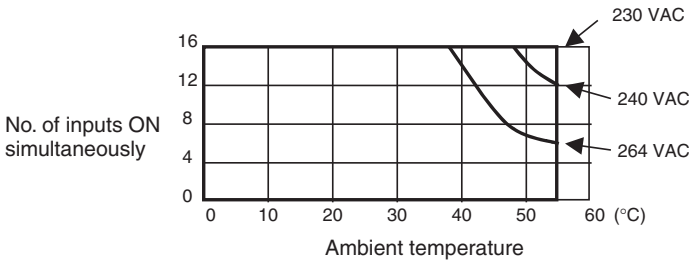
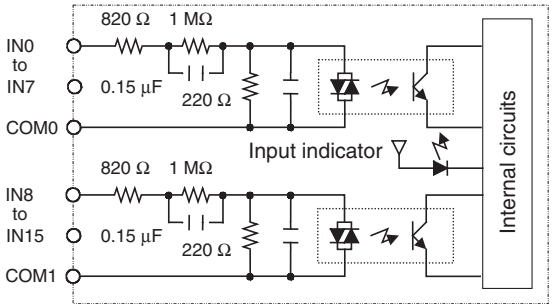
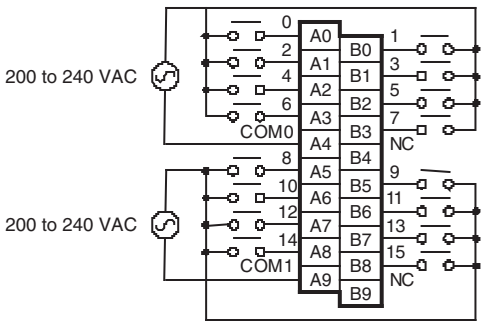
CS1W-IA111 100 V AC Input Unit (16 points)

Rated Input Voltage	100 to 120 V AC, 50/60 Hz, 100 to 120 V DC
Allowable Input Voltage Range	85 to 132 V AC (50/60 Hz), 85 to 132 V DC
Input Impedance	10 kΩ (50 Hz), 8 kΩ (60 Hz), 69 kΩ (DC)
Input Current	100 mA typical (at 100 V AC), 1.5 mA typical (at 100 V DC)
ON Voltage	65 V AC min., 75 V DC min.
OFF Voltage	20 V AC max., 25 V DC max.
ON Response Time	18 ms max. when PLC Setup on default setting (8 ms) (See note 1.)
OFF Response Time	63 ms max. when PLC Setup on default setting (8 ms) (See note 1.)
Insulation Resistance	20 MΩ between external terminals and the GR terminal (500 V DC)
Dielectric Strength	2,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	16 points (8 points/common, 2 commons)
Number of Inputs ON Simultaneously	100% simultaneously ON (for 110 V AC, 120 V DC) Refer to the diagram below. 
Internal Current Consumption	110 mA 5 V DC max.
Weight	260 g max.
Circuit Layout	
Terminal Connections	

Note 1. The Input ON and OFF response times for Basic I/O Units can be set to 0 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, or 32 ms in the PLC Setup. When the response times have been set to 0 ms, the ON response time will be 10 ms maximum and the OFF response time will be 40 ms maximum due to internal element delays.

2. Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on the Unit.

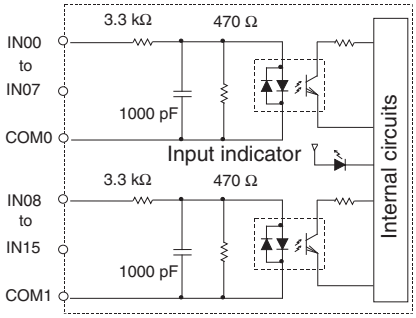
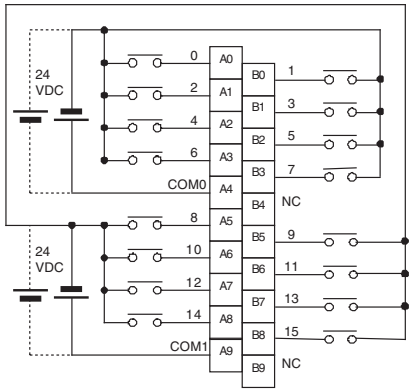
CS1W-IA211 200-V AC Input Unit (16 points)

Rated Input Voltage	200 to 240 V AC, 50/60 Hz
Allowable Input Voltage Range	170 to 264 V AC (50/60 Hz)
Input Impedance	21 kΩ (50 Hz), 18 kΩ (60 Hz)
Input Current	10 mA typical (at 200 V AC)
ON Voltage/ON current	120 V AC min.
OFF Voltage/OFF current	40 V AC max.
ON Response Time	18 ms max. when PLC Setup on default setting (8 ms) (See note.)
OFF Response Time	48 ms max. when PLC Setup on default setting (8 ms) (See note.)
No. of Circuits	16 points (8 points/common, 2 commons)
Number of Inputs ON Simultaneously	100% simultaneously ON (for 230 V AC). Refer to the diagram below. 
Insulation Resistance	20 MΩ between external terminals and the GR terminal (500 V DC)
Dielectric Strength	2,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	110 mA 5 V DC max.
Weight	260 g max.
Circuit Configuration	
Terminal Connections	

Note 1. The Input ON and OFF response times for Basic I/O Units can be set to 0 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, or 32 ms in the PLC Setup. When the response times have been set to 0 ms, the ON response time will be 10 ms maximum and the OFF response time will be 40 ms maximum due to internal element delays.

2. Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on the Unit.

CS1W-ID211 24-V DC Input Unit (16 Points)

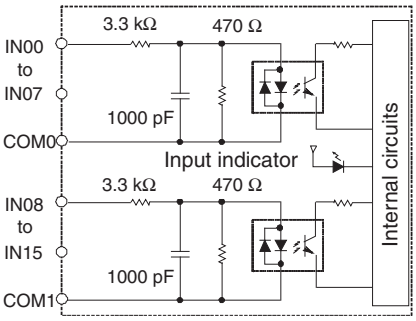
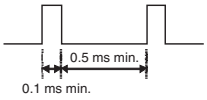
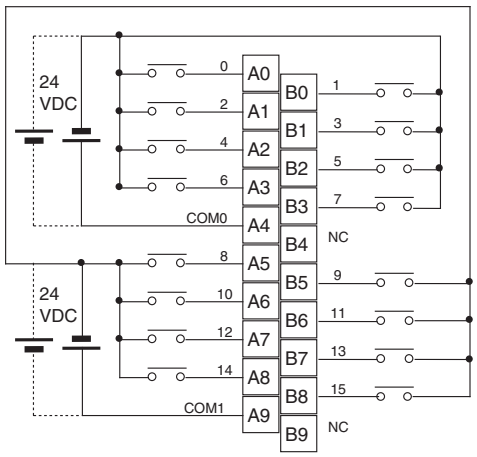
Rated Input Voltage	24 V DC
Allowable Input Voltage Range	20.4 to 26.4 V DC
Input Impedance	3.3 kΩ
Input Current	7 mA typical (at 24 V DC)
ON Voltage/ON Current	14.4 V DC min./3 mA min.
OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	8.0 ms max. (Possible to set to between 0 and 32 ms in the PLC Setup.) (See note.)
OFF Response Time	8.0 ms max. (Possible to set to between 0 and 32 ms using PLC) (See note.)
No. of Circuits	16 (8 points/common, 2 circuits)
Number of Simultaneously ON Points	100% simultaneously ON
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	100 mA max.
Weight	270 g max.
Circuit Configuration	
Terminal Connections	

Note 1. The ON response time will be 20 μs maximum and OFF response time will be 300 μs maximum even if the response times are set to 0 ms due to internal element delays.

2. Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on all Units.

3. Terminal numbers A0 to A20 and B0 to B20 are printed on all Units.

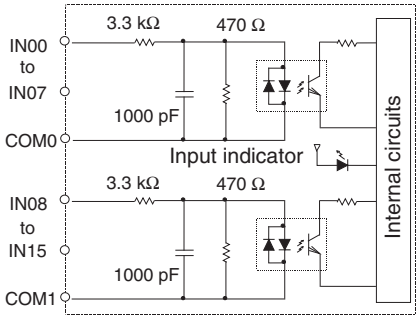
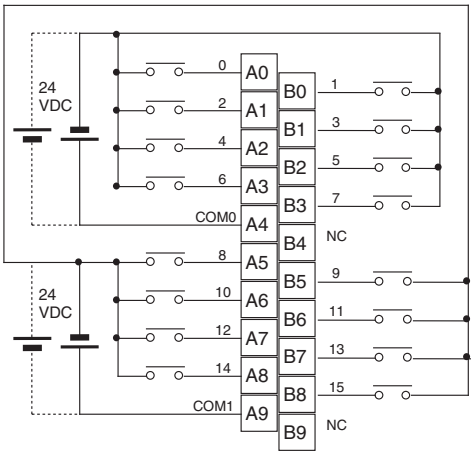
CS1W-INT01 Interrupt Input Unit (16 Points)

Rated Input Voltage	24 V DC
Allowable Input Voltage Range	20.4 to 26.4 V DC
Input Impedance	3.3 kΩ
Input Current	7 mA typical (at 24 V DC)
ON Voltage/ON Current	14.4 V DC min./3 mA min.
OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	0.1 ms max.
OFF Response Time	0.5 ms max.
No. of Circuits	16 (8 points/common, 2 circuits)
Number of Simultaneously ON Points	100% simultaneously ON
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	100 mA max.
Weight	270 g max.
Circuit Configuration	 • Up to two Interrupt Input Units can be mounted to the CPU Rack. • Interrupts cannot be used when an Interrupt Input Unit is mounted to an Expansion I/O Rack, i.e., it will be treated as a 16-point Input Unit. • Set the pulse width of signals input to the Interrupt Input Unit so they satisfy the above conditions. 
Terminal Connections	 Polarity of the input power supply can connected in either direction.

Note 1. Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on the Unit.

2. The Interrupt Input Unit can be used to input interrupts with a Single CPU System. With a Duplex CPU System, the Interrupt Input Unit will function only as a standard Input Unit.

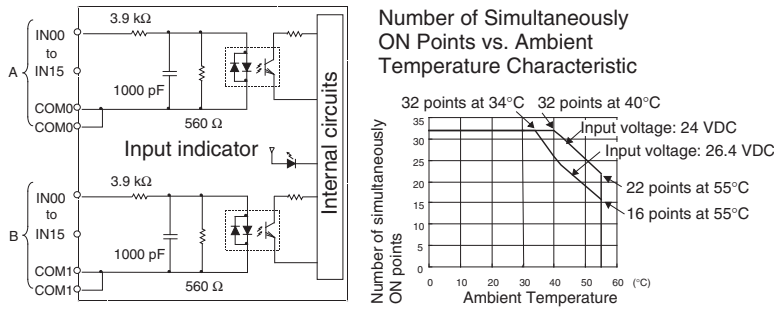
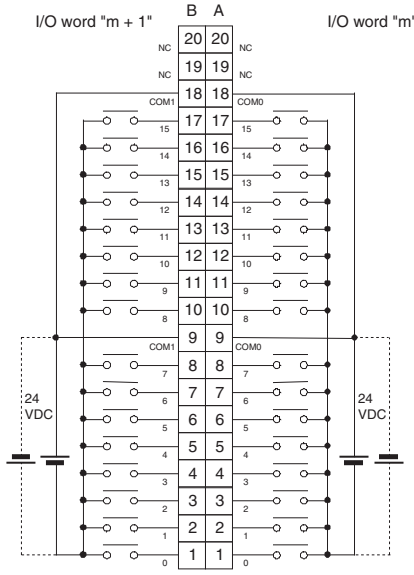
CS1W-IDP01 High-speed Input Unit (16 Points)

Rated Input Voltage	24 V DC
Allowable Input Voltage Range	20.4 to 26.4 V DC
Input Impedance	3.3 kΩ
Input Current	7 mA typical (at 24 V DC)
ON Voltage/ON Current	14.4 V DC min./3 mA min.
OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	0.1 ms max.
OFF Response Time	0.5 ms max.
No. of Circuits	16 (8 points/common, 2 circuits)
Number of Simultaneously ON Points	100% simultaneously ON
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	100 mA max.
Weight	270 g max.
Circuit Configuration	
Terminal Connections	 Polarity of the input power supply can be connected in either direction.

- With a High-speed Input Unit, pulse inputs shorter than the cycle time of the CPU Unit can be read.
- The minimum pulse width (ON time) that can be read by the High-speed Input Unit is 0.1 ms.
- Input data in the internal circuits is cleared during the input refresh period.

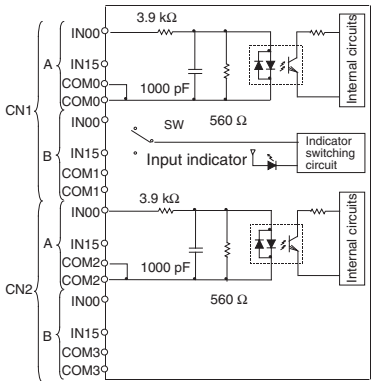
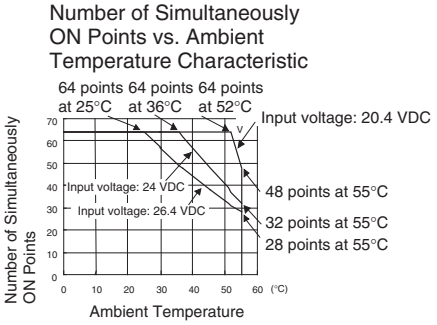
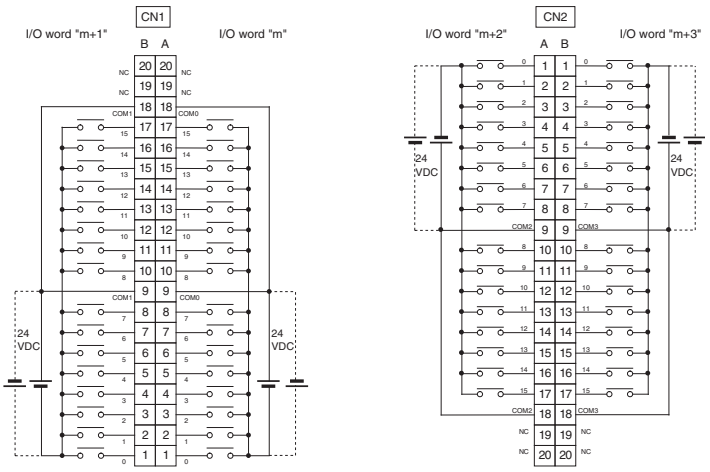
Note Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on the Unit.

CS1W-ID231 DC Input Unit (32 Points)

Rated Input Voltage	24 V DC
Allowable Input Voltage Range	20.4 to 26.4 V DC
Input Impedance	3.9 kΩ
Input Current	6 mA typical (at 24 V DC)
ON Voltage/ON Current	15.4 V DC min./3 mA min.
OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PLC Setup.) (See note.)
OFF Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PLC Setup) (See note.)
No. of Circuits	32 (16 points/common, 2 circuits)
Number of Simultaneously ON Points	70% (11 points/common) (at 24 V DC) (Refer to the following illustrations.)
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	150 mA max.
Weight	200 g max.
Accessories	One connector for external wiring (soldered)
Circuit Configuration	
Terminal Connections	 • The input power polarity can be connected in either direction provided that the same polarity is set for rows A and B. • Both COM0 and COM1 have two pins each. Although they are internally connected, wire all points completely.

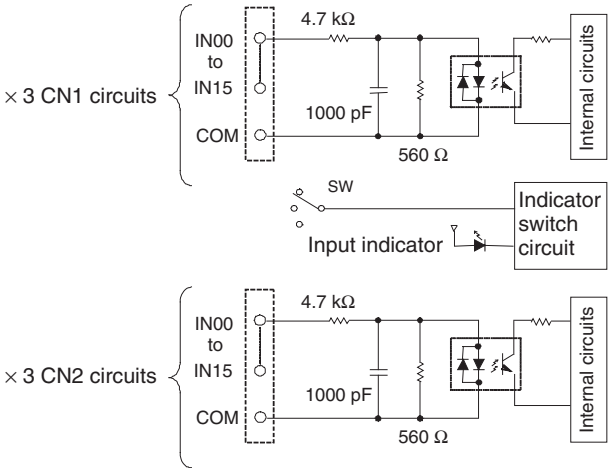
Note The ON response time will be 20 μs maximum and OFF response time will be 300 μs maximum even if the response times are set to 0 ms due to internal element delays.

CS1W-ID261 DC Input Unit (64 Points)

Rated Input Voltage	24 V DC
Allowable Input Voltage Range	20.4 to 26.4 V DC
Input Impedance	3.9 kΩ
Input Current	6 mA typical (at 24 V DC)
ON Voltage/ON Current	15.4 V DC min./3 mA min.
OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PLC Setup.) (See note.)
OFF Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PLC Setup.) (See note.)
No. of Circuits	64 (16 points/common, 4 circuits)
Number of Simultaneously ON Points	50% (8 points/common) (at 24 V DC) (Refer to the following illustrations.)
Insulation Resistance	20 MΩ between external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	150 mA max.
Weight	260 g max.
Accessories	Two connectors for external wiring (soldered)
Circuit Configuration	 
Terminal Connections	 • The input power polarity can be connected in either direction provided that the same polarity be set for rows A and B. • COM0, COM1, COM2, and COM3 have two pins each. Although they are internally connected, wire all points completely.

Note The ON response time will be 120 μs maximum and OFF response time will be 300 μs maximum even if the response times are set to 0 ms due to internal element delays.

CS1W-ID291 DC Input Unit (96 Points)

Rated Input Voltage	24 V DC
Allowable Input Voltage Range	20.4 to 26.4 V DC
Input Impedance	4.7 kΩ
Input Current	Approx. 5 mA (at 24 V DC)
ON Voltage/ON Current	17 V DC min./3 mA min.
OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	8.0 ms max. (Possible to select one out of eight times from 0 to 32 ms in the PLC Setup.) (See note 1.)
OFF Response Time	8.0 ms max. (Possible to select one out of eight times from 0 to 32 ms in the PLC Setup.) (See note 1.)
No. of Circuits	96 points (16 points/common, 6 commons)
Number of Inputs ON Simultaneously	50% (8 points/common) (at 24 V DC) (Depends on ambient temperature) (See note 2.)
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	200 mA max.
Weight	320 g max.
Accessories	Two connectors for external wiring (soldered)
Circuit Configuration	The ON response time will be 120 μs maximum and OFF response time will be 300 μs maximum even if the response times are set to 0 ms due to internal element delays. (See note below.) 
Terminal Connections	See *Figure 1.* The polarity of the input power supply can be in either direction.

Note 1. The Input ON and OFF response times for Basic I/O Units can be set to 0 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, or 32 ms in the PLC Setup.

2. The number of allowable simultaneously ON inputs depends on the ambient temperature. Refer to page 518.

Terminal Connections

The polarity of the input power supply can be in either direction, as indicated by the dotted lines.

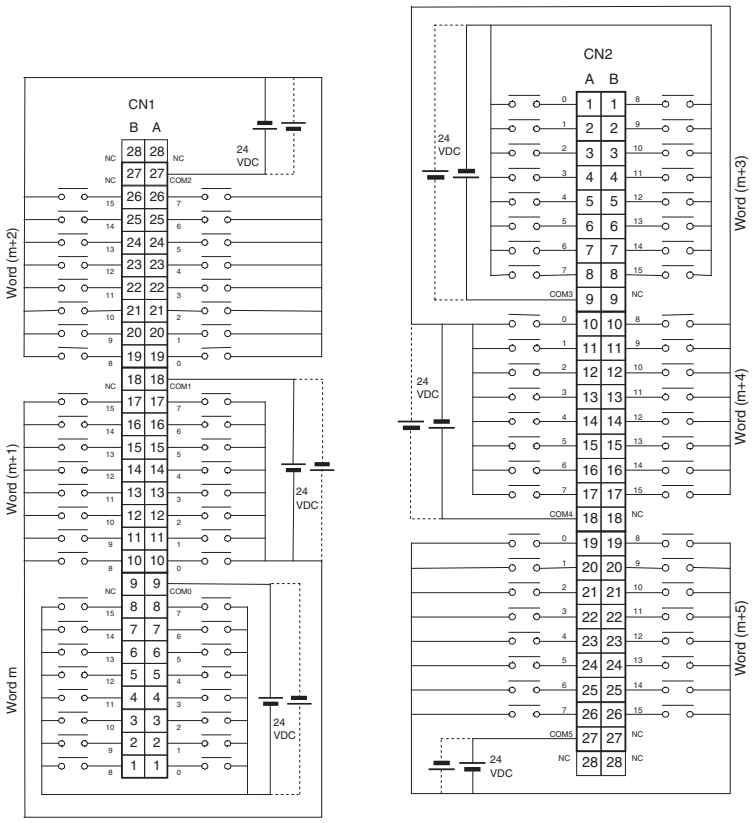
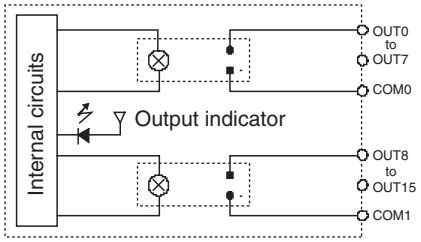
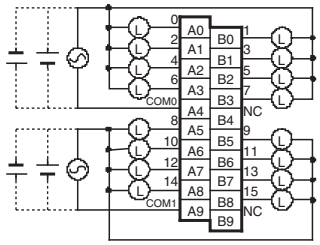


Figure 1 Terminal Connections: CS1W-ID291 24-V DC 96-point Input Unit

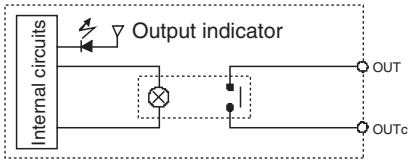
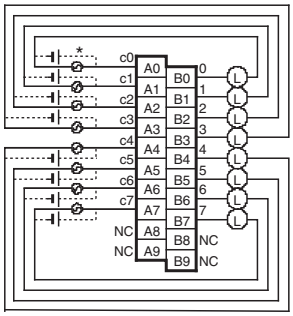
Basic Output Units

CS1W-OC211 Contact Output Unit (16 points)

Max. Switching Capacity	2 A 250 V AC (cosϕ = 1), 2 A 24 V DC (8 A/common, 16 A/Unit), 0.1 A 120 V DC
Min. Switching Capacity	1 mA 5 V DC
Relay Replacement	NY-24W-K-IE (Fujitsu Takamizawa Component Ltd.) Relays cannot be replaced by users.
Service Life of Relay	Electrical: 150,000 operations (resistive load)/100,000 operations (inductive load) Mechanical: 20,000,000 operations Service life will vary depending on the connected load. Refer to page 519 for information on service life according to the load.
ON Response Time	15 ms max.
OFF Response Time	15 ms max.
No. of Circuits	16 points (8 points/common, 2 commons)
Number of Inputs ON Simultaneously	16
Surge Protector	None
Fuses	None
Insulation Resistance	20 MΩ between external terminals and the GR terminal (500 V DC)
Dielectric Strength	2,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	130 mA 5 V DC max. 96 mA 26 V DC (6 mA × No. points ON)
Weight	290 g max.
Circuit Configuration	
Terminal Connections	2 A 250 VAC, 2 A 24 VDC, 0.1 A 120 VDC max. 

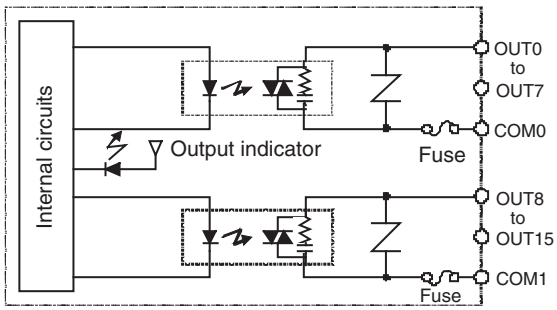
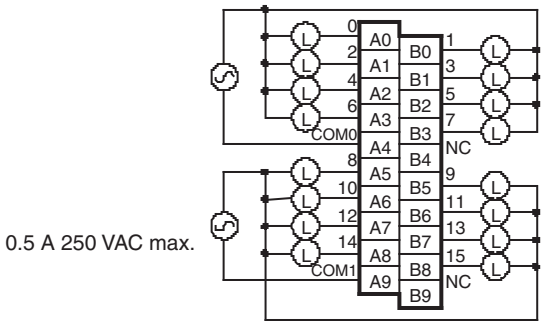
Note Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on the Unit.

CS1W-OC201 Contact Output Unit (8 points)

Max. Switching Capacity	2 A 250 V AC (cosϕ = 1), 2 A 24 V DC (16 A/Unit), 0.1 A 120 V DC
Min. Switching Capacity	1 mA 5 V DC
Relay replacement	NY-24W-K-IE (Fujitsu Takamizawa Component Ltd.) Relays cannot be replaced by users.
Service Life of Relay	Electrical: 150,000 operations (resistive load)/100,000 operations (inductive load) Mechanical: 20,000,000 operations Service life will vary depending on the connected load. Refer to page 519 for information on service life according to the load.
ON Response Time	15 ms max.
OFF Response Time	15 ms max.
No. of Circuits	8 independent contacts
Number of Inputs ON Simultaneously	8
Surge Protector	None
Fuses	None
Insulation Resistance	20 MΩ between external terminals and the GR terminal (500 V DC)
Dielectric Strength	2,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	100 mA 5 V DC max. 48 mA 26 V DC (6 mA × No. points ON)
Weight	260 g max.
Circuit Configuration	
Terminal Connections	 2 A 250 VAC, 2 A 24 VDC, 0.1 A 120 VDC max. * A relay contact is used, so there is no polarity when a DC power supply is used.

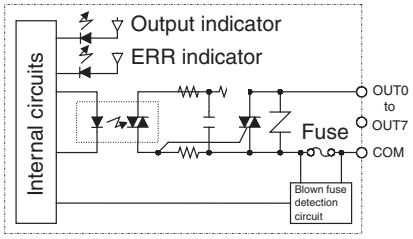
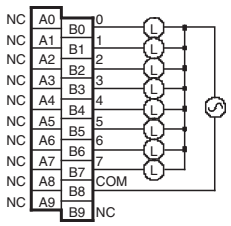
Note Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on the Unit.

CS1W-OA211 Triac Output Unit (16 Points)

Max. Switching Capacity	0.5 A 250 V AC, 50/60 Hz (2 A/common, 4 A/Unit)
Max. Inrush Current	15 A (pulse width: 10 ms)
Min. Switching Capacity	50 mA 75 V AC
Leakage Current	1.5 mA (200 V AC) max.
Residual Voltage	1.6 V AC max.
ON Response Time	1 ms max.
OFF Response Time	1/2 of load frequency+1 ms or less.
No. of Circuits	16 points (8 points/common, 2 commons)
Surge Protector	C.R Absorber + Surge Absorber
Fuses	2 × 4 A (1 per common) The fuse cannot be replaced by the user.
Blown Fuse Detection Circuit	None
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (500 V DC)
Dielectric Strength	2,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	406 mA 5 V DC max. (70 mA + 21 mA × No. of ON points)
Weight	300 g max.
Circuit Configuration	
Terminal Connections	

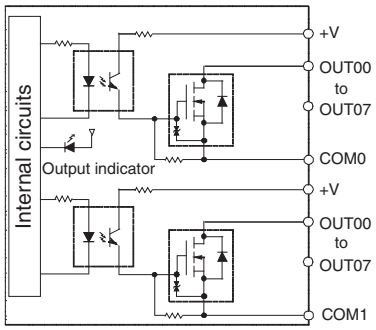
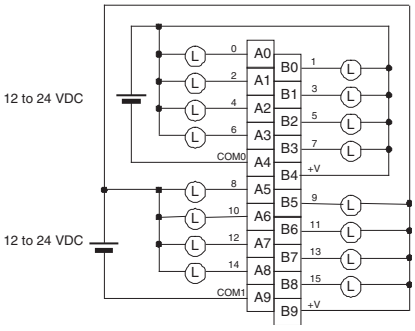
Note Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on the Unit.

CS1W-OA201 Triac Output Unit (8 Points)

Max. Switching Capacity	1.2 A 250 V AC, 50/60 Hz (4.8 A/Unit)
Max. Inrush Current	10 A (pulse width: 100 ms), 20 A (pulse width: 10 ms)
Min. Switching Capacity	100 mA 10 V AC, 50 mA 24 V AC, 10 mA 100 V AC min.
Leakage Current	1.5 mA (120 V AC) max., 3.0 mA (240 V AC) max.
Residual Voltage	1.5 V AC max. (50 to 500 mA), 5.0 V AC max. (10 to 50 mA)
ON Response Time	1 ms max.
OFF Response Time	1/2 of load frequency+1 ms or less.
No. of Circuits	8 points (8 points/common, 1 common)
Surge Protector	C.R Absorber + Surge Absorber
Fuses	8 A The fuse cannot be replaced by the user.
Blown Fuse Detection Circuit	ERR indicator lit when fuse blown. Also, the corresponding Flag in the Basic I/O Unit Information Area (A050 to A089) will turn ON.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (500 V DC)
Dielectric Strength	2,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
Internal Current Consumption	230 mA 5 V DC max. (70 mA + 20 mA × No. of ON points)
Weight	300 g max.
Circuit Configuration	
Terminal Connections	 1.2 A 250 VAC max.

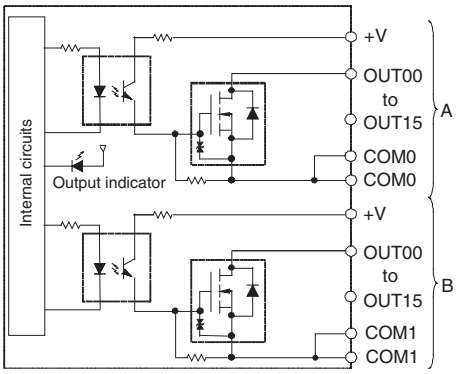
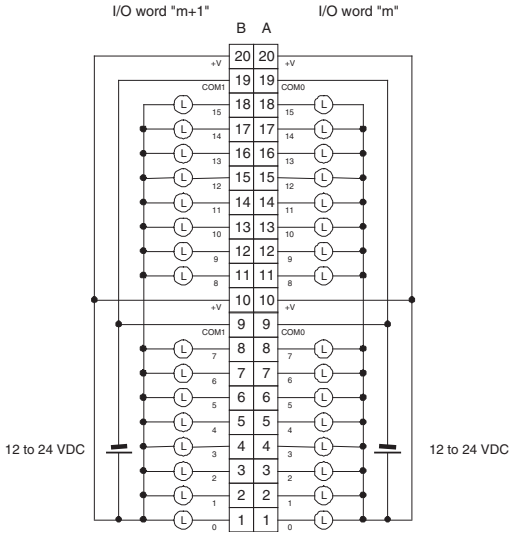
Note Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on the Unit.

CS1W-OD211 Transistor Output Unit (16 Points, Sinking)

Rated Voltage	12 to 24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC
Maximum Load Current	0.5 A/point, 4.0 A/common, 8.0 A/Unit
Maximum Inrush Current	4.0 A/point, 10 ms max.
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	16 (8 points/common, 2 circuits)
Internal Current Consumption	5 V DC 170 mA max.
Fuses	None
External Power Supply	10.2 to 26.4 V DC, 20 mA max.
Weight	270 g max.
Circuit Configuration	
Terminal Connections	 • When wiring, pay careful attention to the polarity. • The load may operate incorrectly if the polarity is reversed.

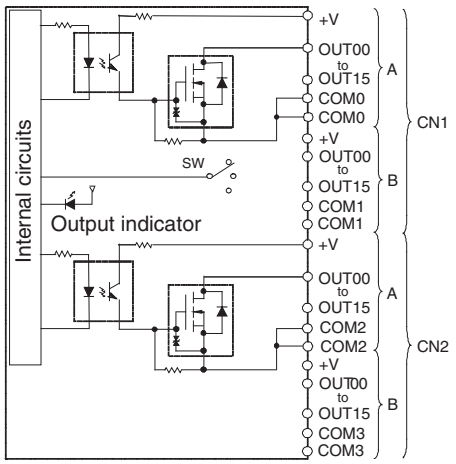
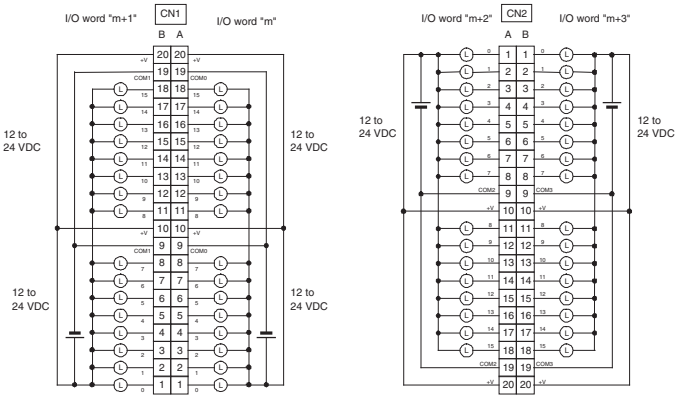
Note Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on the Unit.

CS1W-OD231 Transistor Output Unit (32 Points, Sinking)

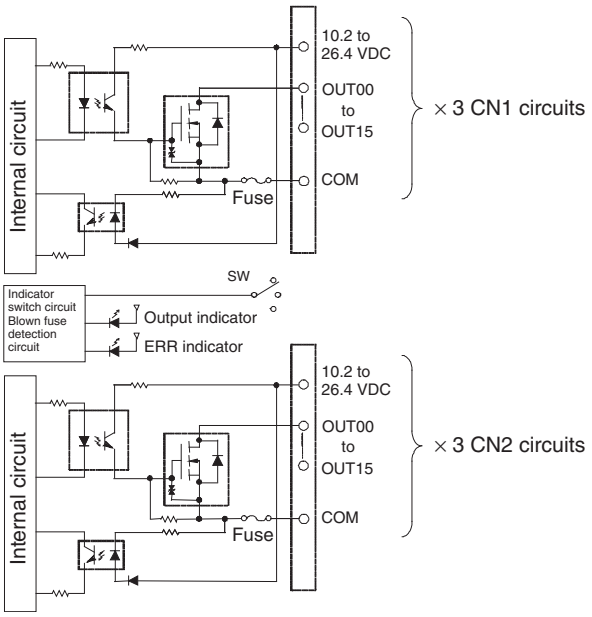
Rated Voltage	12 to 24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC
Maximum Load Current	0.5 A/point, 2.5 A/common, 5.0 A/Unit (See note.)
Maximum Inrush Current	4.0 A/point, 10 ms max.
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	32 (16 points/common, 2 circuits)
Internal Current Consumption	5 V DC 270 mA max.
Fuses	None
External Power Supply	10.2 to 26.4 V DC, 30 mA max.
Weight	200 g max.
Accessories	One connector for external wiring (soldered)
Circuit Configuration	
Terminal Connections	 • When wiring, pay careful attention to the polarity. The load may operate if the polarity is reversed. • Although the +V and COM terminals of rows A and B are internally connected, wire all points completely.

Note The maximum load currents will be 2.0 A/common and 4.0 A/Unit if a pressure-welded connector is used.

CS1W-OD261 Transistor Output Unit (64 Points, Sinking)

Rated Voltage	12 to 24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC
Maximum Load Current	0.3 A/point, 1.6 A/common, 6.4 A/Unit
Maximum Inrush Current	3.0 A/point, 10 ms max.
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	64 (16 points/common, 4 circuits)
Internal Current Consumption	5 V DC 390 mA max.
Fuses	None
External Power Supply	10.2 to 26.4 V DC, 50 mA max.
Weight	260 g max.
Accessories	Two connectors for external wiring (soldered)
Circuit Configuration	
Terminal Connections	 • When wiring, pay careful attention to the polarity. The load may operate if the polarity is reversed. • Although the +V and COM terminals of rows A and B of CN1 and CN2 are internally connected, wire all points completely.

CS1W-OD291 Transistor Output Unit (96 Points, Sinking)

Rated Voltage	12 to 24 V DC
Operating Load Voltage	10.2 to 26.4 V DC
Maximum Load Current	0.1 A/point, 1.2 A/common, 7.2 A/Unit (See note.)
Maximum Inrush Current	1.0 A/point, 10 ms max. 8.0 A/common, 10 ms max.
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	96 points (16 points/common, 6 commons)
Internal Current Consumption	480 mA max. at 5 V DC
Fuses	3 A (1 per common, 6 total) The fuse cannot be replaced by the user.
External Power Supply	10.2 to 26.4 V DC, 100 mA max.
Weight	320 g max.
Accessories	Two connectors for external wiring (soldered)
Circuit Configuration	 The ERR indicator will light if a fuse blows or if the external power supply is turned OFF, and the corresponding Flag in the Basic I/O Unit Information Area (A050 to A089) will turn ON.
Terminal Connections	Refer to *Figure 2.* When wiring, pay careful attention to the polarity. The load may operate if the polarity is reversed.

Note The maximum load currents will be 1.0 A/common and 6.0 A/Unit if a pressure-welded connector is used.

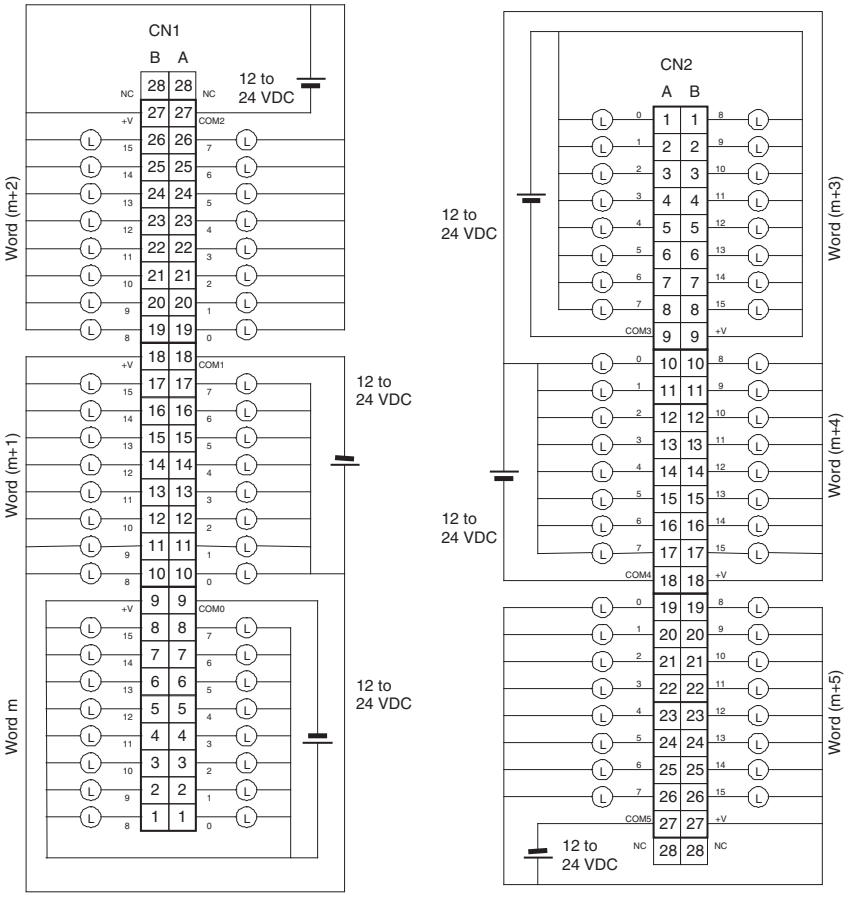
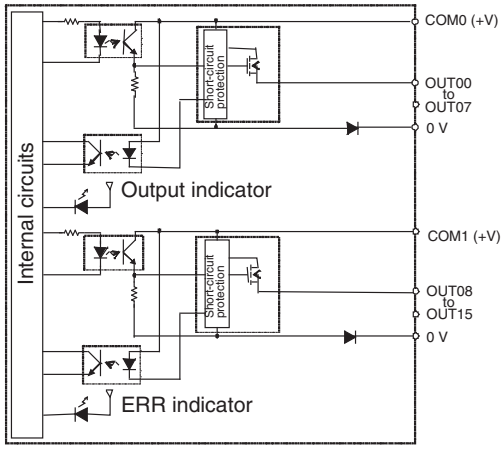
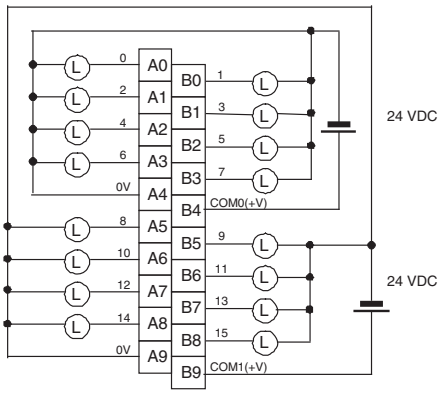


Figure 2 Terminal Connections: CS1W-OD291 24-V DC 96-point Transistor Output Unit (Sinking Outputs)

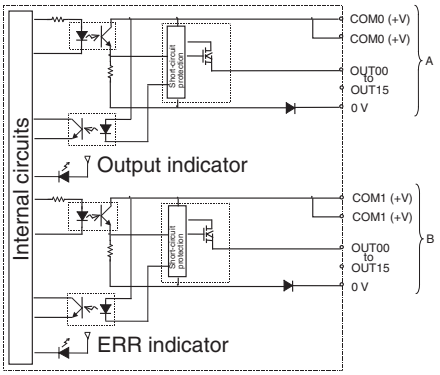
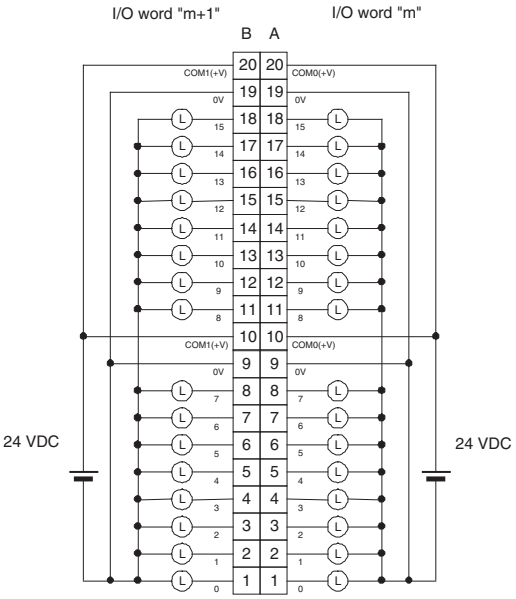
CS1W-OD212 Transistor Output Unit (16 Points, Sourcing)

Rated Voltage	24 V DC
Operating Load Voltage Range	20.4 to 26.4 V DC
Maximum Load Current	0.5 A/point, 2.5 A/common, 5.0 A/Unit
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Load Short-circuit Prevention	Detection current: 0.7 to 2.5 A Automatic restart after error clearance. (Refer to page 521.)
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	16 (8 points/common, 2 circuits)
Internal Current Consumption	5 V DC 170 mA max.
External Power Supply	20.4 to 26.4 V DC, 40 mA max.
Weight	270 g max.
Circuit Configuration	 When overcurrent is detected, the ERR indicator will light, and the corresponding flag in the Basic I/O Unit Information Area (A050 to A089) will turn ON.
Terminal Connections	 When wiring, pay careful attention to the polarity of the external power supply. The load may operate if the polarity is reversed.

Note Terminal numbers A0 to A9 and B0 to B9 are used in this manual, but they are not printed on the Unit.

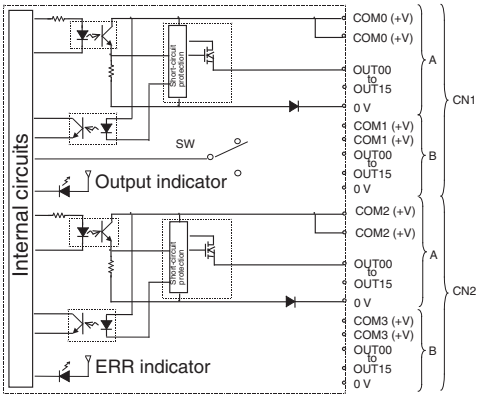
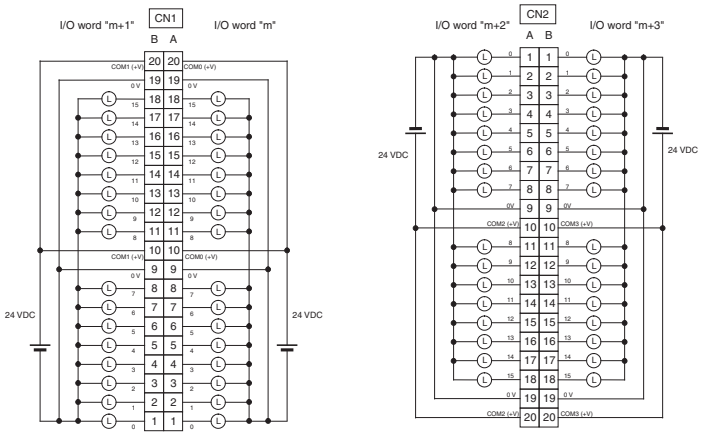
CS1W-OD232 Transistor Output Unit (32 Points, Sourcing)

Rated Voltage	24 V DC
Operating Load Voltage Range	20.4 to 26.4 V DC
Maximum Load Current	0.5 A/point, 2.5 A/common, 5.0 A/Unit (See note.)
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Load Short-circuit Prevention	Detection current: 0.7 to 2.5 A Automatic restart after error clearance. (Refer to page 521.)
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	32 (16 points/common, 2 circuits)
Internal Current Consumption	5 V DC 270 mA max.
External Power Supply	20.4 to 26.4 V DC, 70 mA max.
Weight	210 g max.
Accessories	One connector for external wiring (soldered)

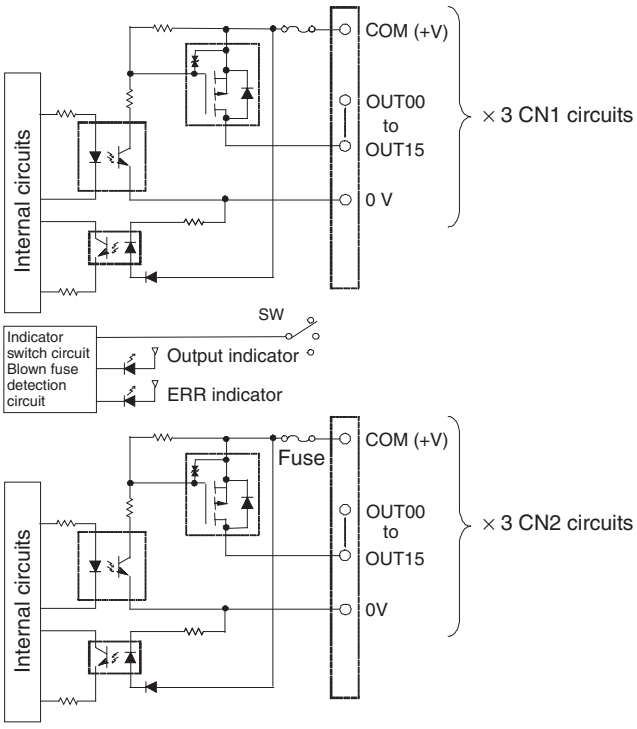
Circuit Configuration	 When the output current of any output exceeds the detection current, the output for that point will turn OFF. At the same time, the ERR indicator will light and the corresponding flag (one for each common) in the Basic I/O Unit Information Area (A050 to A089) will turn ON.
Terminal Connections	 • When wiring, pay careful attention to the polarity of the external power supply. The load may operate if the polarity is reversed. • Although the COM(+V) and 0V of rows A and B are internally connected, wire all points completely.

Note The maximum load currents will be 2.0 A/common and 4.0 A/Unit if a pressure-welded connector is used.

CS1W-OD262 Transistor Output Unit (64 Points, Sourcing)

Rated Voltage	24 V DC
Operating Load Voltage Range	20.4 to 26.4 V DC
Maximum Load Current	0.3 A/point, 1.6 A/common, 6.4 A/Unit
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Load Short-circuit Prevention	Detection current: 0.7 to 2.5 A Automatic restart after error clearance. (Refer to page 521.)
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	64 (16 points/common, 4 circuits)
Internal Current Consumption	5 V DC 390 mA max.
External Power Supply	20.4 to 26.4 V DC, 130 mA max.
Weight	270 g max.
Accessories	Two connectors for external wiring (soldered)
Circuit Configuration	 When overcurrent is detected, the ERR indicator will light. At the same time, the corresponding flag (one for each common) in the Basic I/O Unit Information Area (A050 to A089) will turn ON.
Terminal Connections	 • When wiring, pay careful attention to the polarity of the external power supply. The load may operate if the polarity is reversed. • Although the COM(+V) and 0V of rows A and B of CN1 and CN2 are internally connected, wire all points completely.

CS1W-OD292 Transistor Output Unit (96 Points, Sourcing)

Rated Voltage	12 to 24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC
Maximum Load Current	0.1 A/point, 1.2 A/common, 7.2 A/Unit (See note.)
Maximum Inrush Current	1.0 A/point, 10 ms max. 8.0 A/common, 10 ms max.
Leakage Current	0.1 mA max.
Residual Voltage	1.5 V max.
ON Response Time	0.5 ms max.
OFF Response Time	1.0 ms max.
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.
No. of Circuits	96 points (16 points/common, 6 commons)
Internal Current Consumption	480 mA max. at 5 V DC
Fuses	3 A (1 per common, 6 total) The fuse cannot be replaced by the user.
External Power Supply	10.2 to 26.4 V DC, 100 mA max.
Weight	320 g max.
Accessories	Two connectors for external wiring (soldered)
Circuit Configuration	 The ERR indicator will light if a fuse blows or if the external power supply is turned OFF, and the corresponding Flag in the Basic I/O Unit Information Area (A050 to A089) will turn ON.
Terminal Connections	When wiring, pay careful attention to the polarity of the external power supply. The load may operate if the polarity is reversed.

Note The maximum load currents will be 1.0 A/command and 6.0 A/Unit if a pressure-welded connector is used.

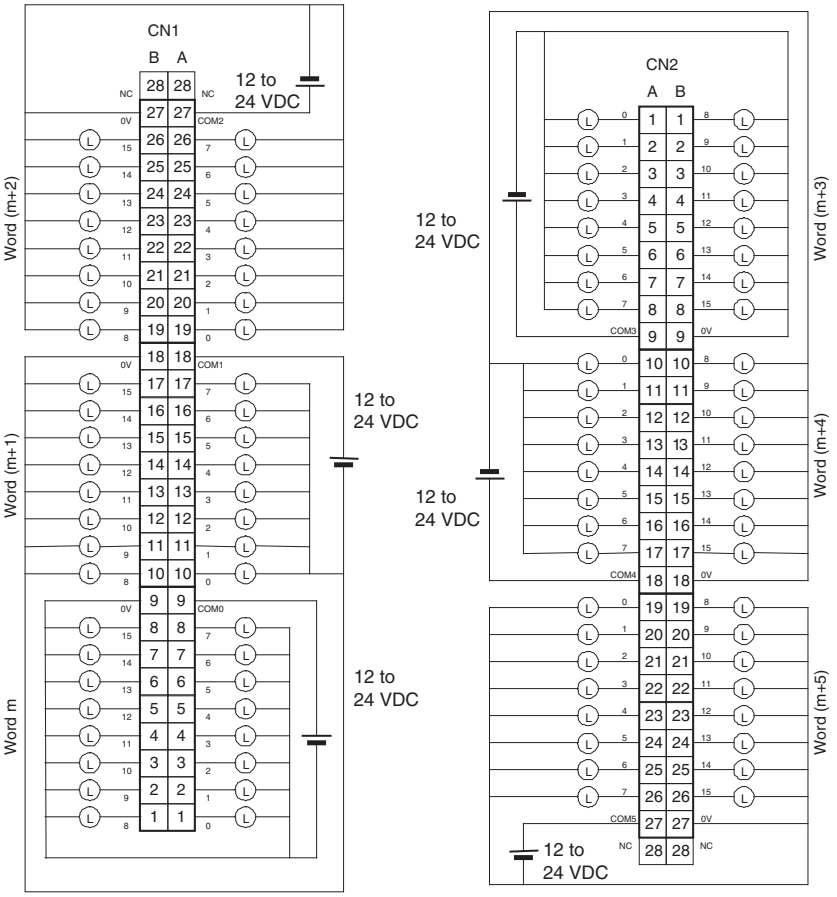
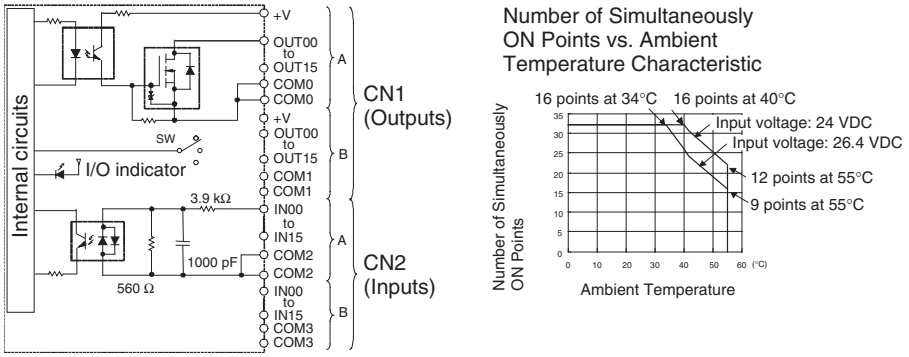
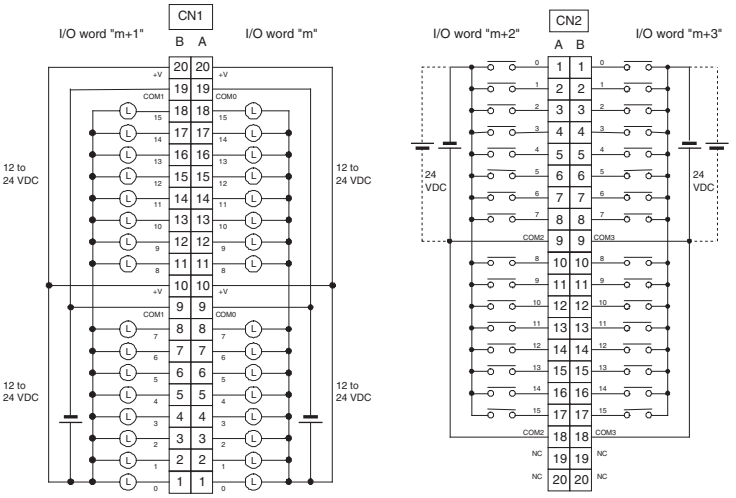


Figure 3 Terminal Connections: CS1W-OD292 24-V DC 96-point Transistor Output Unit (Sourcing Outputs)

CS1W-MD261 24-V DC Input/Transistor Output Unit (32/32 Points, Sinking)

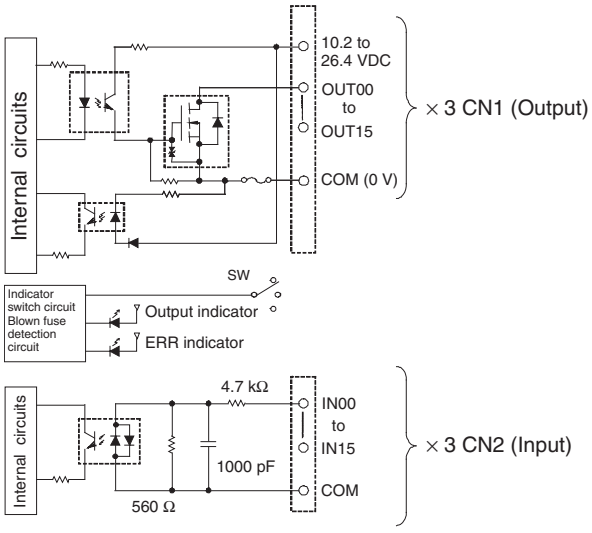
Output section (CN1)		**Input section (CN2)**	
Rated Voltage	12 to 24 V DC	Rated Input Voltage	24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC	Allowable Input Voltage Range	20.4 to 26.4 V DC
Maximum Load Current	0.3 A/point, 1.6 A/common, 3.2 A/Unit	Input Impedance	3.9 kΩ
Maximum Inrush Current	3.0 A/point, 10 ms max.	Input Current	6 mA typical (at 24 V DC)
Leakage Current	0.1 mA max.	ON Voltage/ON Current	15.4 V DC min./3 mA min.
Residual Voltage	1.5 V max.	OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	0.5 ms max.	ON Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PLC Setup.) (See note.)
OFF Response Time	1.0 ms max.		
No. of Circuits	32 (16 points/common, 2 circuits)	OFF Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PLC Setup.) (See note.)
Fuses	None		
External Power Supply	10.2 to 26.4 V DC, 30 mA min.	No. of Circuits	32 (16 points/common, 2 circuits)
		Number of Simultaneously ON Points	70% (11 points/common) (at 24 V DC)
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)		
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.		
Internal Current Consumption	5 V DC 270 mA max.		
Weight	260 g max.		
Accessories	Two connectors for external wiring (soldered)		

Circuit Configuration	
Terminal Connections	 • When wiring, pay careful attention to the polarity. The load may operate is polarity is reversed. • Although the +V and COM terminals of rows A and B of CN1 and CN2 are internally connected, wire all points completely.

Note 1. The ON response time will be 120 μs maximum and OFF response time will be 300 μs maximum even if the response times are set to 0 ms due to internal element delays.

2. The input ON and OFF response times for Basic I/O Units can be set to 0 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, or 32 ms in the PLC Setup.

CS1W-MD291 DC Input/Transistor Output Unit (48/48 Points, Sinking)

Outputs (CN1)		**Inputs (CN2)**	
Rated Voltage	12 to 24 V DC	Rated Input Voltage	24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC	Allowable Input Voltage Range	20.4 to 26.4 V DC
Maximum Load Current	0.1 A/point, 1.2 A/common, 3.6 A/Unit (See note 2.)	Input Impedance	4.7 kΩ
Maximum Inrush Current	1.0 A/point, 10 ms max. 8.0 A/common, 10 ms max.	Input Current	Approx. 5 mA (at 24 V DC)
Leakage Current	0.1 mA max.	ON Voltage/ON Current	17 V DC min./3 mA min.
Residual Voltage	1.5 V max.	OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	0.5 ms max.	ON Response Time	8.0 ms max. (Possible to select one out of eight times from 0 to 32 ms in the PLC Setup.) (See note 1.)
OFF Response Time	1.0 ms max.		
No. of Circuits	48 points (16 points/common, 3 commons)	OFF Response Time	8.0 ms max. (Possible to select one out of eight times from 0 to 32 ms in the PLC Setup.) (See note 1.)
Fuses	3 A (1 per common, 3 total) The fuse cannot be replaced by the user.		
External Power Supply	10.2 to 26.4 V DC, 50 mA max.	No. of Circuits	48 points (16 points/common, 3 commons)
		Number of Inputs Simultaneous ON	50% (8 points/common) (at 24 V DC) (Depends on ambient temperature.)
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)		
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.		
Internal Current Consumption	350 mA max. at 5 V DC		
Weight	320 g max.		
Accessories	Two connectors for external wiring (soldered)		
	 The ERR indicator will light if a fuse blows or if the external power supply is turned OFF, and the corresponding Flag in the Basic I/O Unit Information Area (A050 to A089) will turn ON.		
Terminal Connections	Refer to *Figure 4.* When wiring, pay careful attention to the polarity. The load may operate is polarity is reversed.		

Note 1. The input ON and OFF response times for Basic I/O Units can be set to 0 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, or 32 ms in the PLC Setup. The ON response time will be 120 μs maximum and OFF response time will be 300 μs maximum even if the response times are set to 0 ms due to internal element delays.

2. The maximum load currents will be 1.0 A/common and 3.0 A/Unit if a pressure-welded connector is used.

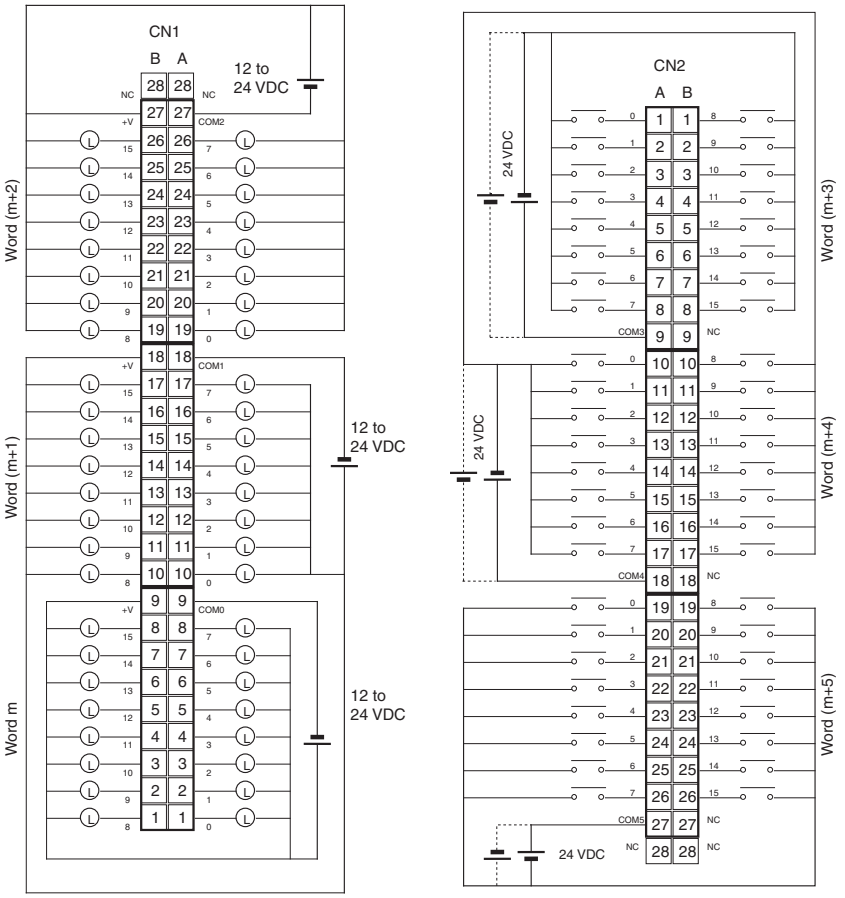
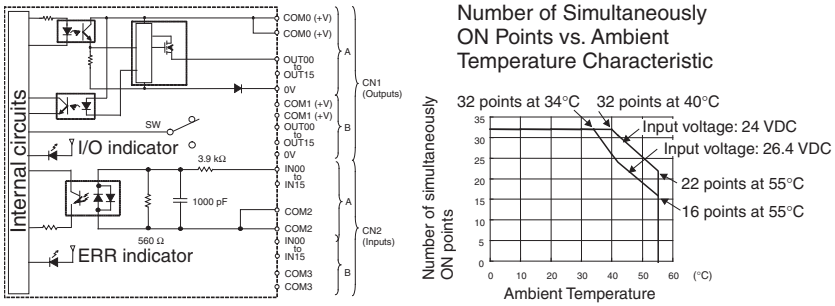
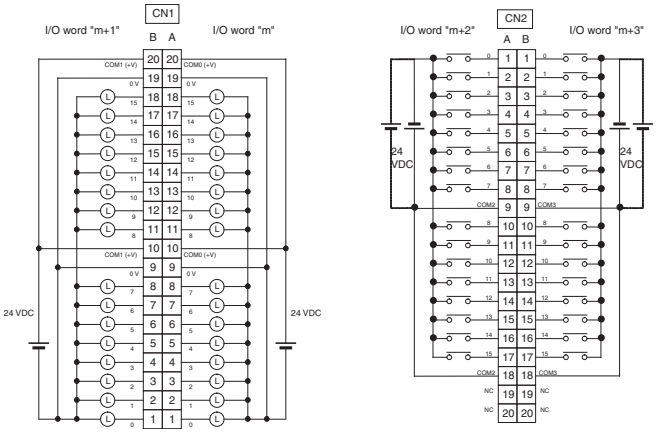


Figure 4 Terminal Connections: CS1W-MD291 24-V DC 48-point Input/48-point Output Unit (Sinking Outputs)

CS1W-MD262 24-V DC Input/Transistor Output Unit (32/32 Points, Sourcing)

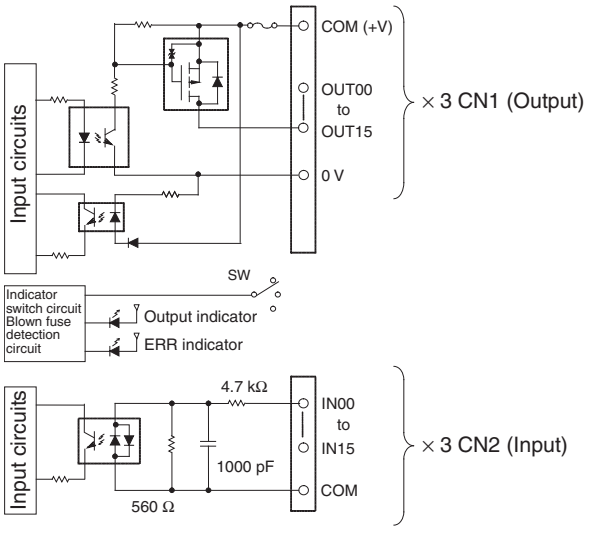
Output section (CN1)		**Input section (CN2)**	
Rated Voltage	24 V DC	Rated Input Voltage	24 V DC
Operating Load Voltage Range	20.4 to 26.4 V DC	Allowable Input Voltage Range	20.4 to 26.4 V DC
Maximum Load Current	0.3 A/point, 1.6 A/common, 3.2 A/Unit	Input Impedance	3.9 kΩ
Leakage Current	0.1 mA max.	Input Current	6 mA typical (at 24 V DC)
Residual Voltage	1.5 V max.	ON Voltage/ON Current	15.4 V DC min./3 mA min.
ON Response Time	0.5 ms max.	OFF Voltage/OFF Current	5 V DC max./1 mA max.
OFF Response Time	1.0 ms max.	ON Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PLC Setup.) (See note.)
Load Short-circuit Prevention	Detection current: 0.7 to 2.5 A Automatic restart after error clearance. (Refer to page 521.)		
No. of Circuits	32 (16 points/common, 2 circuits)	OFF Response Time	8.0 ms max. (Can be set to between 0 and 32 in the PLC Setup.) (See note.)
External Power Supply	20.4 to 26.4 V DC, 70 mA min.	No. of Circuits	32 (16 points/common, 2 circuits)
		Number of Simultaneously ON Points	70% (11 points/common) (at 24 V DC)
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)		
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.		
Internal Current Consumption	5 V DC 270 mA max.		
Weight	270 g max.		
Accessories	Two connectors for external wiring (soldered)		

<table>
<tr><td>Circuit Configuration</td><td> 
</td></tr>
<tr><td>Terminal Connections</td><td> 

When wiring, pay careful attention to the polarity. The load may operate if the polarity is reversed.
Although the +V and COM terminals of rows A and B of CN1 and CN2 are internally connected, wire all points completely.
</td></tr>
</table>

Note The ON response time will be 120 μs maximum and OFF response time will be 300 μs maximum even if the response times are set to 0 ms due to internal element delays.

CS1W-MD292 24-V DC Input/Transistor Output Unit (48/48 Points, Sourcing)

Outputs (CN1)		**Inputs (CN2)**	
Rated Voltage	12 to 24 V DC	Rated Input Voltage	24 V DC
Operating Load Voltage Range	10.2 to 26.4 V DC	Allowable Input Voltage Range	20.4 to 26.4 V DC
Maximum Load Current	0.1 A/point, 1.2 A/common, 3.6 A/Unit (See note 2.)	Input Impedance	4.7 kΩ
Maximum Inrush Current	1.0 A/point, 10 ms max. 8.0 A/common, 10 ms max.	Input Current	Approx. 5 mA (at 24 V DC)
Leakage Current	0.1 mA max.	ON Voltage/ON Current	17 V DC min./3 mA min.
Residual Voltage	1.5 V max.	OFF Voltage/OFF Current	5 V DC max./1 mA max.
ON Response Time	0.5 ms max.	ON Response Time	8.0 ms max. (Possible to select one out of eight times from 0 to 32 ms in the PLC Setup.) (See note 1.)
OFF Response Time	1.0 ms max.		
No. of Circuits	48 points (16 points/common, 3 commons)	OFF Response Time	8.0 ms max. (Possible to select one out of eight times from 0 to 32 ms in the PLC Setup.) (See note 1.)
Fuses	3 A (1 per common, 3 total) The fuse cannot be replaced by the user.		
External Power Supply	10.2 to 26.4 V DC, 50 mA min.	No. of Circuits	48 points (16 points/common, 3 commons)
		Number of Input Simultaneous ON	50% (8 points/common) (at 24 V DC) (Depends on ambient temperature.)
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)		
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.		
Internal Current Consumption	350 mA max. at 5 V DC		
Weight	320 g max.		
Accessories	Two connectors for external wiring (soldered)		
	 The ERR indicator will light if a fuse blows or if the external power supply is turned OFF, and the corresponding Flag in the Basic I/O Unit Information Area (A050 to A089) will turn ON.		
Terminal Connections	Refer to *Figure 5.* When wiring, pay careful attention to the polarity. The load may operate if the polarity is reversed.		

Note 1. The input ON and OFF response times for Basic I/O Units can be set to 0 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, or 32 ms in the PLC Setup. The ON response time will be 120 μs maximum and OFF response time will be 300 μs maximum even if the response times are set to 0 ms due to internal element delays.

2. The maximum load currents will be 1.0 A/common and 3.0 A/Unit if a pressure-welded connector is used.

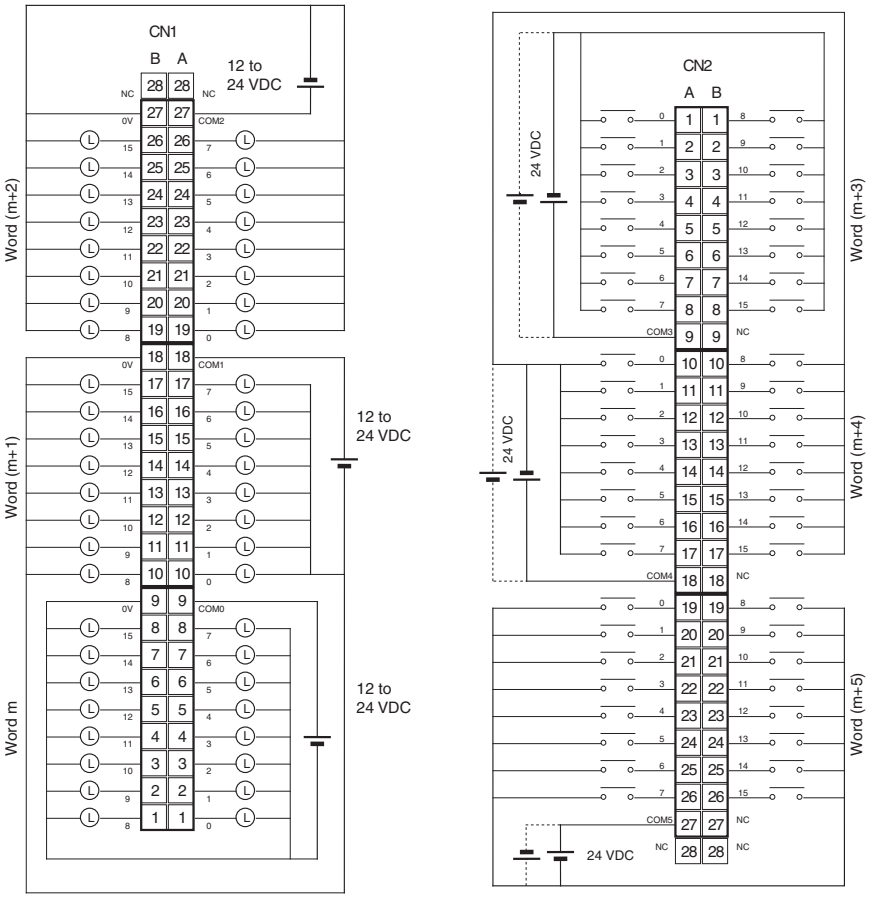
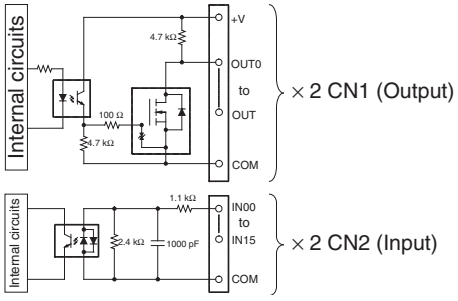
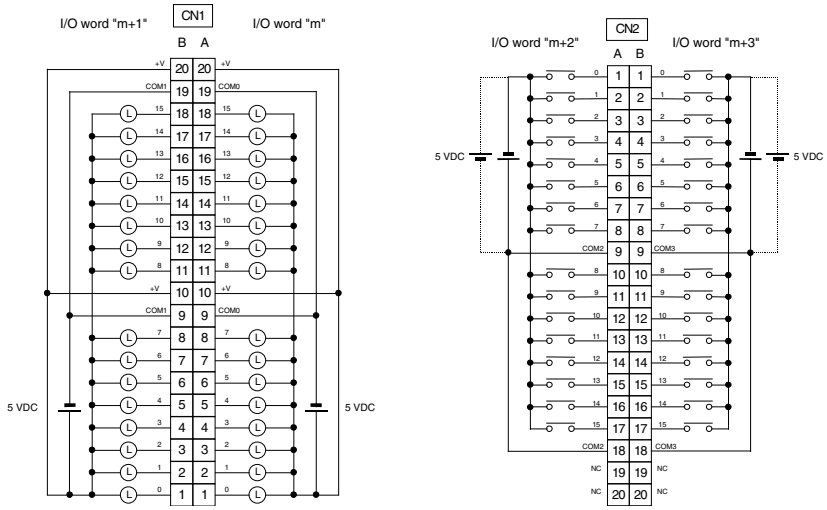


Figure 5 Terminal Connections: CS1W-MD292 24-V DC 48-point Input/48-point Transistor Output Unit (Sourcing Outputs)

CS1W-MD561 TTL I/O Unit (32 Inputs, 32 Outputs)

Outputs (CN1)		**Inputs (CN2)**	
Rated Voltage	5 V DC ±10%	Rated Input Voltage	5 V DC ±10%
Operating Load Voltage Range	4.5 to 5.5 V DC	Input Impedance	1.1 kΩ
Maximum Load Current	35 mA/point, 560 mA/common, 1.12 A/Unit	Input Current	Approx. 3.5 mA (at 5 V DC)
		ON Voltage	3.0 V DC min.
Leakage Current	0.1 mA max.	OFF Voltage	1.0 V DC max.
Residual Voltage	0.4 V max.	ON Response Time	8.0 ms max. (Possible to select one out of eight times from 0 to 32 ms in the PLC Setup.) (See notes 1 and 2.)
ON Response Time	0.2 ms max.		
OFF Response Time	0.3 ms max.	OFF Response Time	8.0 ms max. (Possible to select one out of eight times from 0 to 32 ms in the PLC Setup.) (See notes 1and 2.)
No. of Circuits	32 points (16 points/common, 2 commons)		
Fuses	None	No. of Circuits	32 points (16 points/common, 2 commons)
External Power Supply	5 V DC ±10% 40 mA min. (1.2 mA x number of ON pts)	Number of Input Simultaneous ON	No restrictions
Insulation Resistance	20 MΩ between the external terminals and the GR terminal (100 V DC)		
Dielectric Strength	1,000 V AC between the external terminals and the GR terminal for 1 minute at a leakage current of 10 mA max.		
Internal Current Consumption	270 mA max. at 5 V DC		
Weight	260 g max.		
Accessories	Two connectors for external wiring (soldered)		
Circuit Configuration			
Terminal Connections			

- When wiring, pay careful attention to the polarity. The load may operate if the polarity is reversed.
- Although the +V and COM terminals of rows A and B of CN1 and CN2 are internally connected, wire all points completely.

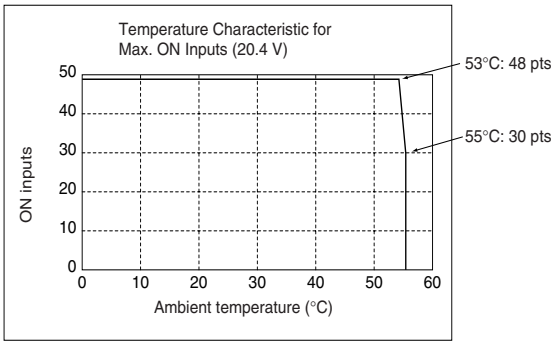
Note 1. The ON response time will be 120 μs maximum and OFF response time will be 300 μs maximum even if the response times are set to 0 ms due to internal element delays.
2. The input ON and OFF response times for Basic I/O Units can be set to 0 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, or 32 ms in the PLC Setup.

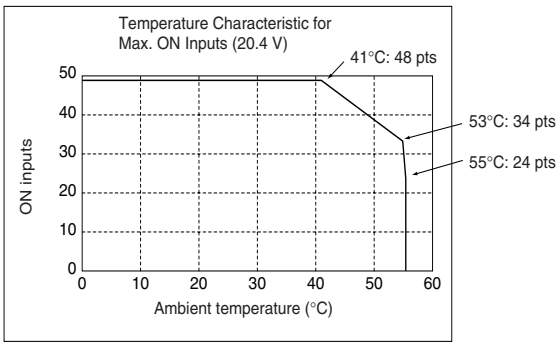
Maximum Number of ON Inputs for 24-V DC Inputs

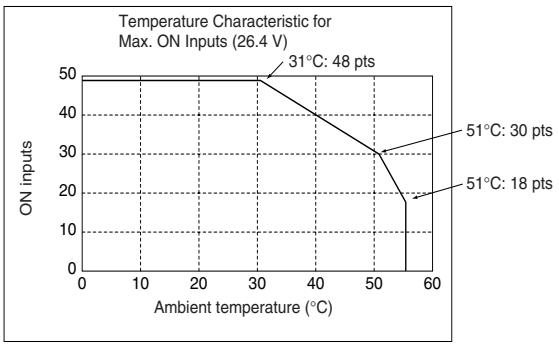
CS1W-ID291/MD291/MD292

The maximum number of 24-V DC inputs that can be ON simultaneously for the CS1W-ID291/MD291/MD292 depends on the ambient temperature, as shown in the following diagrams.

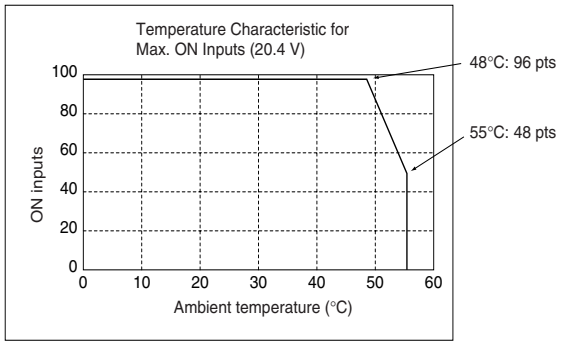
CS1W-MD291/292 Inputs

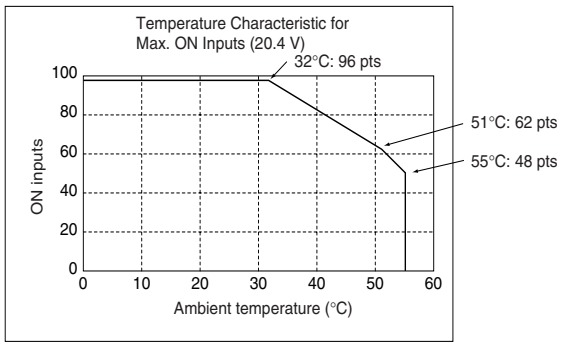


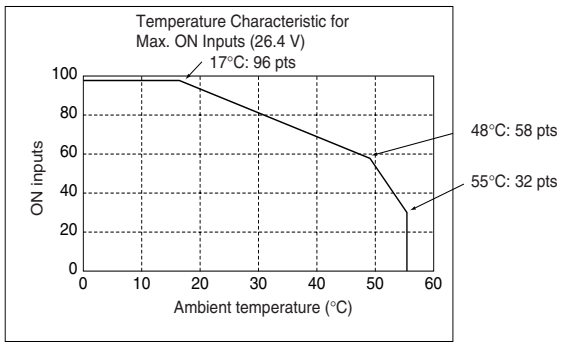




CS1W-ID291 Inputs







If the maximum number of ON points is exceeded for the CS1W-ID291/MD291/MD292, heat generated by electronic elements will increase the temperature of the electronic elements and the interior of the Unit. This will reduce the reliability and life of the electronic elements and cause Unit malfunctions. There will be a delay in the temperature increase, however, and there will be no problems if all inputs are ON for 10 minutes or less at the start of operations or any other time that all inputs have been off for at least 2 hours.

About Contact Output Units

When used in the ways shown below, there may be differences in the life expectancies of the relays.

- When using in excess of rated values
- When appropriate surge countermeasures are not taken
- When connected to a load (e.g., relay, solenoid, or motor) that generates a high counterelectromotive force when power is interrupted
- When connected to a load (e.g., capacitor or lamp) that generates a high inrush current when power is turned ON

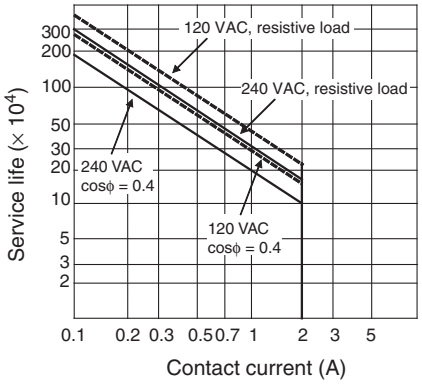
In the above cases, ensure the rated life expectancies of the relays by, for example, taking the appropriate surge countermeasures as explained in the manual, or using a switching device (as a relay) with ratings appropriate for the load.

Life Expectancy of CS1W-OC201/211 Relays

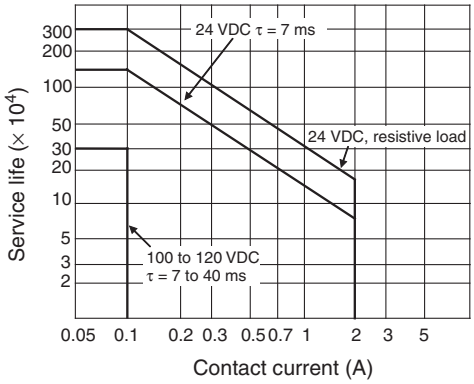
The life expectancy of the CS1W-OC201/211 Contact Output Unit is shown in the following diagrams. Use the diagrams to calculate the relay service life based on the operating conditions, and replace the relay before the end of its service life.

Note The diagrams show the life expectancy of the relay itself. Do not use a contact current, therefore, that exceeds the maximum switching capacity specified in the specifications for each Contact Output Unit. If a switching capacity exceeding the specifications is used, the reliability and life expectancy of other parts will be reduced and the Unit may malfunction.

Service Life with AC Load



Service Life with DC Load



Max. switching frequency: 1,800 times/h

Inductive Load

The life of the Relay varies with the load inductance. If any inductive load is connected to the Contact Output Unit, use an arc killer with the Contact Output Unit using an inductive load.

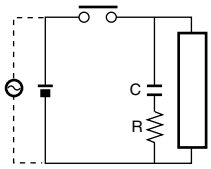
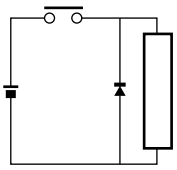
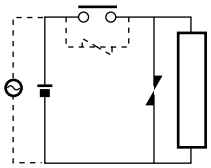
Be sure to connect a diode in parallel with every DC inductive load that is connected to the Contact Output Unit.

Contact Protection Circuit

Arc killers are used with the Contact Output Unit in order to prolong the life of each Relay mounted to the Contact Output Unit, prevent noise, and reduce the generation of carbide and nitrate deposits. Arc killers can, however, reduce relay life if not use correctly.

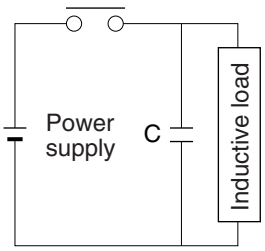
Note Arc killers used with the Contact Output Unit can delay the resetting time required by each Relay mounted to the Contact Output Unit.

Arc killer circuit examples are listed in the following table.

Circuit		Current		Characteristic	Required element
		AC	DC		
Using a CR		Yes	Yes	If the load is a relay or solenoid, there is a time lag between the moment the circuit is opened and the moment the load is reset. If the supply voltage is 24 or 48 V, insert the arc killer in parallel with the load. If the supply voltage is 100 to 200 V, insert the arc killer between the contacts.	The capacitance of the capacitor must be 1 to 0.5 μF per contact current of 1 A and resistance of the resistor must be 0.5 to 1 Ω per contact voltage of 1 V. These values, however, vary with the load and the characteristics of the relay. Decide these values from experiments, and take into consideration that the capacitance suppresses spark discharge when the contacts are separated and the resistance limits the current that flows into the load when the circuit is closed again. The dielectric strength of the capacitor must be 200 to 300 V. If the circuit is an AC circuit, use a capacitor with no polarity.
Using a diode		No	Yes	The diode connected in parallel with the load changes energy accumulated by the coil into a current, which then flows into the coil so that the current will be converted into Joule heat by the resistance of the inductive load. This time lag, between the moment the circuit is opened and the moment the load is reset, caused by this method is longer than that caused by the CR method.	The reversed dielectric strength value of the diode must be at least 10 times as large as the circuit voltage value. The forward current of the diode must be the same as or larger than the load current. The reversed dielectric strength value of the diode may be two to three times larger than the supply voltage if the arc killer is applied to electronic circuits with low circuit voltages.
Using a varistor		Yes	Yes	The varistor method prevents the imposition of high voltage between the contacts by using the constant voltage characteristic of the varistor. There is time lag between the moment the circuit is opened and the moment the load is reset. If the supply voltage is 24 or 48 V, insert the varistor in parallel with the load. If the supply voltage is 100 to 200 V, insert the varistor between the contacts.	---

Note Do not connect a capacitor as an arc killer in parallel with an inductive load as shown in the following diagram. This arc killer is very effective for preventing spark discharge at the moment when the circuit is opened. However when the contacts are closed, the contacts may be welded due to the current charged in the capacitor.

DC inductive loads can be more difficult to switch than resistive loads. If appropriate arc killers are used, however, DC inductive loads will be as easy to switch as resistive loads.

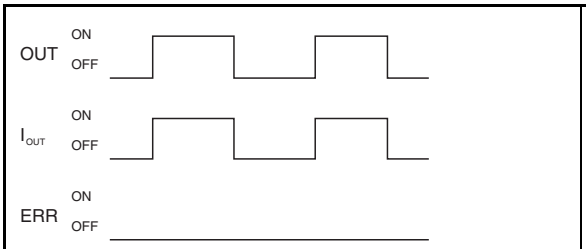


Load Short-circuit Protection

CS1W-OD212/OD232/OD262/MD262

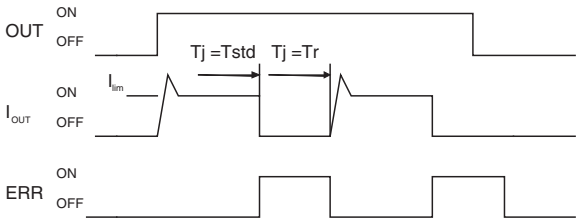
As shown below, normally when the output bit turns ON (OUT), the transistor will turn ON and then output current (Iout) will flow. If the output (Iout) is overloaded or short-circuited exceeding the detection current (Ilim), the output current (Iout) will be limited as shown in *Figure 2* below. When the junction temperature (Tj) of the output transistor reaches the thermal shutdown temperature (Tstd), the output will turn OFF to protect the transistor from being damaged, and the alarm output bit will turn ON to light the ERR indicator. When the junction temperature (Tj) of the transistor drops down to the reset temperature (Tr), the ERR indicator will be automatically reset and the output current will start flowing.

Figure 1: Normal Condition



OUT: OUTPUT instruction
I_{OUT}: Output current
ERR: Alarm output, ERR indicator
I_{lim}: Detection current
Tj: Junction temperature of transistor
Tstd: Thermal shutdown temperature
Tr: Reset temperature

Figure 2: Overload or Short-circuit



Operating Restrictions for the CS1W-OD212/OD232/OD262/MD262

Although the CS1W-OD212/OD232/OD262/MD262 are provided with short-circuit protection, these are for protecting internal circuits against momentary short-circuiting in the load. As shown in *Figure 2* below, the short-circuit protection is automatically released when the Tj equals to Tr. Therefore, unless the cause of short-circuit is removed, ON/OFF operations will be repeated in the output. Leaving short-circuits for any length of time will cause internal temperature rise, deterioration of elements, discoloration of the case or PCBs, etc. Therefore, observe the following restrictions.

Restrictions

If a short-circuit occurs in an external load, immediately turn OFF the corresponding output and remove the cause. The CS1W-OD212/OD232/OD262/MD262 turn ON an alarm output bit that corresponds to the external load output number. There is an alarm output bit for every common.

When an alarm output bit turns ON, use a self-holding bit for the alarm in the user program and turn OFF the corresponding output.

The alarm output bit is allocated in the Basic I/O Unit Information Area (A050 to A089) for every Unit mounting slot.

The following table shows the correspondence between output bits and bits in the Basic I/O Unit Information Area.

Output bit		m		m+1	m+2	m+3
		0 to 7	8 to 15	0 to 15	0 to 15	0 to 15
CS1W-OD212	Mounted in even slot	0	1	---	---	---
	Mounted in odd slot	8	9	---	---	---

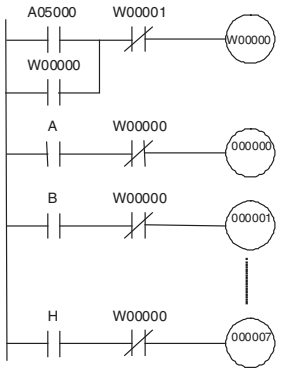
Output bit		m		m+1	m+2	m+3
		0 to 7	8 to 15	0 to 15	0 to 15	0 to 15
CS1W-OD232	Mounted in even slot	0		1	---	---
	Mounted in odd slot	8		9	---	---
CS1W-OD262	Mounted in even slot	0		1	2	3
	Mounted in odd slot	8		9	10	11
CS1W-MD262	Mounted in even slot	0		1	---	---
	Mounted in odd slot	8		9	---	---

For example, when the CS1W-OD212 is mounted in slot 0 on Rack 0, A05001 will turn ON if the output 8 is short-circuited. When the CS1W-OD262 is mounted in slot 1 of Rack 0, A05011 will turn ON if the output m+3 is short-circuited.

Programming Example

In this example, CS1W-OD212 is mounted in slot 0 of the Rack 0.

This example shows how to turn OFF output bits CIO 000000 to CIO 000007 immediately if the alarm output bit A05000 turns ON and how to keep the output bits OFF until the cause is removed and the bit is reset using work bit W000001.



Appendix B
Auxiliary Area Allocations

The tables list the functions of Auxiliary Area words and bits in order of their addresses. For a list of Auxiliary Area words and bit by function, refer to *SECTION 8 Memory Areas*.

The Auxiliary Area consists of read-only words A000 to A447 and read/write words A448 to A959.

Read-only Words

The following words and bits are written by the system to provide information on PLC operation.

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	Bits							
A000		10-ms Incrementing Free Running Timer (Supported in unit version 4.0 or later)	This word contains the system timer used after the power is turned ON. 0000 hex is set when the power is turned ON and this value is automatically incremented by 1 every 10 ms. The value returns to 0000 hex after reaching FFFF hex (655,350 ms), and then continues to be automatically incremented by 1 every 10 ms. **Note:** The timer will continue to be incremented when the operating mode is switched to RUN mode. Example: The interval can be counted between processing A and processing B without requiring timer instructions. This is achieved by calculating the difference between the value in A000 for processing A and the value in A000 for processing B. The interval is counted in 10 ms units.		Held	Cleared	Every 10 ms after the power is turned ON	
A001		100-ms Incrementing Free Running Timer (Supported in unit version 4.0 or later)	This word contains the system timer used after the power is turned ON. 0000 hex is set when the power is turned ON and this value is automatically incremented by 1 every 100 ms. The value returns to 0000 hex after reaching FFFF hex (655,350 ms), and then continues to be automatically incremented by 1 every 10 ms. **Note:** The timer will continue to be incremented when the operating mode is switched to RUN mode.		Held	Cleared	Every 100 ms after the power is turned ON	
A002		1-s Incrementing Free Running Timer (Supported in unit version 4.0 or later)	This word contains a system timer used after the power is turned ON 0000 hex is set when the power is turned ON and this value is automatically incremented by 1 every 1 s. The value returns to 0000 hex after reaching FFFF hex (65,535 s), and then continues to be automatically incremented by 1 every 1 s. **Note:** The timer will continue to be incremented when the operating mode is switched to RUN mode.		Held	Cleared	Every 1 s after the power is turned ON	

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A019	**Previous Cause of Switching to Simplex Operation (Duplex CPU Systems only)**							
	A01900	Duplex Verification Error Switch Flag	ON: A duplex verification error caused the previous switch from duplex to simplex operation.	ON: Switched to simplex operation for duplex verification error OFF: Normal	Held	Held	Data from A023 is stored when duplex operation is recovered.	---
	A01901	Duplex Bus Error Switch Flag	ON: A duplex bus error caused the previous switch from duplex to simplex operation.	ON: Switched to simplex operation for duplex bus error OFF: Normal				
	A01902	Duplex Initialization Error Switch Flag	ON: An error during duplex initialization caused the previous switch from duplex to simplex operation and duplex operation was never started.	ON: Switched to simplex operation for duplex initialization error OFF: Normal				
	A01903	CPU Unit Setting Switch Flag	ON: Changing the CPU Unit's switch from USE to NO USE caused the previous switch from duplex to simplex operation.	ON: Switched to simplex operation for CPU setting OFF: Normal				
	A01904	CPU Error (WDT) Switch Flag	ON: A CPU Unit error (WDT) caused the previous switch from duplex to simplex operation.	ON: Switched to simplex operation for CPU error OFF: Normal				
	A01906	FALS Instruction Error Switch Flag	ON: Execution of an FALS instruction caused the previous switch from duplex to simplex operation.	ON: Switched to simplex operation for FALS instruction OFF: Normal				
	A01908	Cycle Time Overrun Switch Flag	ON: Exceeding the cycle time caused the previous switch from duplex to simplex operation.	ON: Switched to simplex operation for cycle time error OFF: Normal				
	A01909	Program Error Switch Flag	ON: A program error caused the previous switch from duplex to simplex operation.	ON: Switched to simplex operation for program error OFF: Normal				
	A01912	Fatal Inner Board Error Switch Flag	ON: A fatal Inner Board error caused the previous switch from duplex to simplex operation. (Process-control CPU Units only)	ON: Switched to simplex operation for fatal Inner Board error OFF: Normal				
	A01915	Memory Error Switch Flag	ON: A memory error caused the previous switch from duplex to simplex operation.	ON: Switched to simplex operation for memory error OFF: Normal				

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A020 to A022	**Previous Cause of Switching to Simplex Operation (Duplex CPU Systems only)**							
	---	Time of Previous Switch from Duplex to Simplex Operation	The time of the previous switch from duplex to simplex operation is stored.	---	Held	Held	Data from A024 to A026 is stored when duplex operation is recovered.	---
	A02000 to A02007		Seconds (00 to 59)					
	A02008 to A02015		Minutes (00 to 59)					
	A02100 to A02107		Hours (00 to 23)					
	A02108 to A02115		Day of month (01 to 31)					
	A02200 to A02207		Month (01 to 12)					
	A02208 to A02215		Year (00 to 99)					
A023	**Current Cause of Switching to Simplex Operation (Duplex CPU Systems only)** (Check in new active CPU Unit after switch to simplex operation.)							
	A02300	Duplex Verification Error Switch Flag	ON: A duplex verification error caused a switch from duplex to simplex operation. Only operation is switched and the active CPU Unit will not be switched. This flag is turned OFF when duplex operation is restored.	ON: Switched to simplex operation for duplex verification error OFF: Normal	Held	Held	When operation is switched from duplex to simplex operation	A31600 in active and standby CPU Units
	A02301	Duplex Bus Error Switch Flag	ON: A duplex bus error caused a switch from duplex to simplex operation. Only operation is switched and the active CPU Unit will not be switched. This flag is turned OFF when duplex operation is restored.	ON: Switched to simplex operation for duplex bus error OFF: Normal				A31601 in active and standby CPU Units
	A02302	Duplex Initialization Error Switch Flag	ON: An error during duplex initialization caused a switch from duplex to simplex operation and duplex operation was never started. The active CPU Unit will not be switched. This flag is turned OFF when duplex operation is restored.	ON: Switched to simplex operation for duplex initialization error OFF: Normal				---
	A02303	CPU Unit Setting Switch Flag	ON: Changing the CPU Unit's switch from USE to NO USE caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	ON: Switched to simplex operation for CPU setting OFF: Normal				---
	A02304	CPU Error (WDT) Switch Flag	ON: A CPU Unit error (WDT) caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	ON: Switched to simplex operation for CPU error OFF: Normal				---
	A02306	FALS Instruction Error Switch Flag	ON: Execution of an FALS instruction caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	ON: Switched to simplex operation for FALS instruction OFF: Normal				A40106 in CPU Unit with error

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A023	A02308	Cycle Time Overrun Switch Flag	ON: Exceeding the cycle time caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	ON: Switched to simplex operation for cycle time error OFF: Normal	Held	Held	When operation is switched from duplex to simplex operation	A40108 in CPU Unit with error
	A02309	Program Error Switch Flag	ON: A program error caused a switch from duplex to simplex operation.The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	ON: Switched to simplex operation for program error OFF: Normal				A40109 in CPU Unit with error
	A02312	Fatal Inner Board Error Switch Flag (Process-control CPU Units only)	ON: A fatal Inner Board error caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	ON: Switched to simplex operation for fatal Inner Board error OFF: Normal				A40112 in CPU Unit with error
	A02315	Memory Error Switch Flag	ON: A memory error caused a switch from duplex to simplex operation. The active CPU Unit will be switched. This flag is turned OFF when duplex operation is restored.	ON: Switched to simplex operation for memory error OFF: Normal				A40115 in CPU Unit with error
A024 to A026	**Current Cause of Switching to Simplex Operation (Duplex CPU Systems only)** (Check in new active CPU Unit after switch to simplex operation.)							
	---	Time of Switch from Duplex to Simplex Operation (Check in new active CPU Unit after switch to simplex operation.)	The time operation was switched from duplex to simplex operation is stored.	---	Held	Held	When operation is switched from duplex to simplex operation	---
	A02400 to A02407		Seconds (00 to 59)					
	A02408 to A02415		Minutes (00 to 59)					
	A02500 to A02507		Hours (00 to 23)					
	A02508 to A02515		Day of month (01 to 31)					
	A02600 to A02607		Month (01 to 12)					
	A02608 to A02615		Year (00 to 99)					
A027	A02700 to A02715	Duplex Communications Unit Operating Flags	ON: The Communications Unit with the corresponding unit number is in duplex operation. Bits 00 to 15 correspond to unit numbers 0 to F.	ON: Duplex communications OFF: Not duplex communications	Held	Cleared	When duplex communications mode is changed	---
A031	A03115	Online Replacement Flag(See note 1.)	ON: A Basic I/O Unit, Special I/O Unit, or CPU Bus Unit is being replaced online on the CPU Rack, an Expansion Rack, or a Long-distance Expansion Rack. **Note:** This flag indicates removal of a Unit for one of the following functions. • Online Unit Replacement using a Programming Device • Unit Removal without a Programming Device • Removal/Addition of Units without a Programming Device	ON: Online replacement being performed OFF: Online replacement not being performed	Held	Cleared	When a Unit is replaced online	A034

Note 1. CS1D CPU Units for Duplex-CPU System only.

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	Bits							
A034	A03400 to A03415	Online Replacement Slot Flags for CPU Rack	ON: Online replacement is being performed for the slot that corresponds to the ON bit. A03400: Slot 0 A03401: Slot 1 A03402: Slot 2 A03403: Slot 3 A03404: Slot 4 A03405: Slot 5 A03406: Slot 6 A03407: Slot 7 A03415: Duplex Unit (Slots 5 to 7 are supported by Single CPU Systems only.)	ON: Online replacement being performed OFF: Online replacement not being performed	Held	Cleared	When online replacement operation is performed	A26110
A035	A03500 to A03508	Online Replacement Slot Flags for Expansion Rack 1	ON: Online replacement is being performed for the slot that corresponds to the ON bit. Bits 00 to 08 correspond to slots 0 to 8 for each Expansion Slot	ON: Online replacement being performed OFF: Online replacement not being performed	Held	Cleared	When online replacement operation is performed	A26110
A036	A03600 to A03608	Online Replacement Slot Flags for Expansion Rack 2						
A037	A03700 to A03708	Online Replacement Slot Flags for Expansion Rack 3						
A038	A03800 to A03808	Online Replacement Slot Flags for Expansion Rack 4						
A039	A03900 to A03908	Online Replacement Slot Flags for Expansion Rack 5						
A040	A04000 to A04008	Online Replacement Slot Flags for Expansion Rack 6						
A041	A04100 to A04108	Online Replacement Slot Flags for Expansion Rack 7						

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A042	A04200 to A04207	Duplex Communications Switch Cause Flags	Duplex Communications Switch Cause Flag for Communication Unit with unit number 0 Active/Standby Communications Units When an error occurs in the active Communications Unit and operation is switched to the standby Communications Unit, an error code will be stored to show the cause of the error in the active Communications Unit. An error code is not stored when an error occurs in the standby Communications Unit. Primary/Secondary Communications Units (See Note) When an error occurs in the primary Communications Unit and operation is switched to the secondary Communications Unit, an error code will be stored to show the cause of the error in the primary Communications Unit. When an error occurs in the secondary Communications Unit, an error code is stored in the words for one unit number higher than the primary Communications Unit. All Communications Units The corresponding bit in A436 (Duplex Communications Switched Flags) will also turn ON. Refer to the Operation Manual for the Communications Unit for details on error codes. **Note:** Primary/Secondary Communications Units are supported by CPU Unit Ver. 1.1 or later.	Refer to the Operation Manual for the Communications Unit for details on error codes.	Held	Cleared	When duplex communications error occurs	A43600
	A04208 to A04215		Communications Unit with unit number 1 Primary/Secondary Communications Units The error information of the secondary Unit when an error occurs in the secondary Unit will be stored in the bits for unit number 2 (A0400 to A0407).					A43601
A043 to A049	A04300 to A04915		Communications Units with unit numbers 2 to 15 Primary/Secondary Communications Units The error information of the secondary Unit when an error occurs in the secondary Unit will be stored in the bits for the unit number one higher than that of the primary Unit.					A43602 to A43615

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A050	A05000 to A05007	Basic I/O Unit Information, Rack 0 Slot 0	A bit will turn ON to indicate when a fuse has blows. The bit numbers correspond to the fuse number on the Unit.	ON: Fuse blown OFF: Normal	---	---	Every cycle	---
	A05008 to A05015	Basic I/O Unit Information, Rack 0 Slot 1			---	---		---
A051 to A089	A05100 to A08915	Basic I/O Unit Information, Racks 2 to 7			---	---		---
A090 to A093	---	User Program Date	These words contain in BCD the date and time that the user program was last overwritten. A09000 to A09007: Seconds (00 to 59) A09008 to A09015: Minutes (00 to 59) A09100 to A09107: Hour (00 to 23) A09108 to A09115: Day of month (01 to 31) A09200 to A09207: Month (01 to 12) A09208 to A09215: Year (00 to 99) A09308 to A09307: Day of the week (00: Sunday, 01: Monday, 02: Tuesday, 03: Wednesday, 04: Thursday, 05: Friday, 06: Saturday)	---	Held	Held	---	---
A094 to A097	---	Parameter Date	These words contain in BCD the date and time that the parameters were last overwritten. The format is the same as above.	---	Held	Held	---	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A099	A09900	UM Read Protection Status (CPU Units for Single CPU Systems or CPU Units for CS1D Duplex-CPU Systems with unit version 1.4 or later)	Indicates whether the entire user program in the PLC is read-protected.	0: UM not read-protected. 1: UM read-protected.	Retained	Retained	When protection is set or cleared	---
	A09901	Task Read Protection Status (Single CPU Systems only)	Indicates whether read protection is set for individual tasks.	0: Tasks not read-protected. 1: Tasks read-protected.	Retained	Retained	When protection is set or cleared	---
	A09902	Program Write Protection Status when Read Protection Is Set (Single CPU Systems only)	Indicates whether the program is write-protected.	0: Write-enabled. 1: Write-protected.	Retained	Retained	When protection is set or cleared	---
	A09903	Enable/ Disable Status for Backing Up the Program to a Memory Card	Indicates whether creating a backup program file (.OBJ) is enabled or disabled.	0: Enabled 1: Disabled	Retained	Retained	When protection is set or cleared	---
	A09911	Unit Replacement without a Programming Device Enabled Flag	This flag is ON when the Unit Removal without a Programming Device or Removal/Addition of Units without a Programming Device function has been enabled in the PLC Setup.	ON: Enabled OFF: Disabled	Held	Cleared	Written every cycle.	---
	A09914	IR/DR Operation between Tasks	Turn ON this bit to share index and data registers between all tasks. Turn OFF this bit to use separate index and data registers between in each task.	ON: Shared (default) OFF: Independent	Held	Cleared	---	---
	A09915	Timer/ Counter PV Refresh Mode Flag	Indicates whether the CPU Unit is storing timer/counter PV in BCD or binary.	0: BCD mode 1: Binary mode	Held	Held	---	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A100 to A199	All	Error Log Area	When an error has occurred, the error code, error contents, and error's time and date are stored in the Error Log Area. Information on the 20 most recent errors can be stored. Each error record occupies 5 words; the function of these 5 words is as follows: Beginning word: Error code (bits 0 to 15) Beginning word +1: Error contents (bits 0 to 15) Beginning word +2: Minutes (bits 8 to 15), Seconds (bits 0 to 7) Beginning word +3: Day of month (bits 8 to 15), Hours (bits 0 to 7) Beginning word +4: Year (bits 8 to 15), Month (bits 0 to 7) Errors generated by FAL(006) and FALS(007) will also be stored in this Error Log. The Error Log Area can be reset from a Programming Device. If the Error Log Area is full (20 records) and another error occurs, the oldest record in A100 to A104 will be cleared, the other 19 records are shifted down, and the new record is stored in A195 to A199.	Error code Error contents: Address of Aux. Area word with details or 0000. Seconds: 00 to 59, BCD Minutes: 00 to 59, BCD Hours: 00 to 23, BCD Day of month: 01 to 31, BCD Year: 00 to 99, BCD	Held	Held	When error occurs	A50014 A300 A400
A200	A20011	First Cycle Flag	ON for one cycle after PLC operation begins (after the mode is switched from PROGRAM to RUN or MONITOR, for example).	ON for the first cycle	---	---	---	---
	A20012	Step Flag	ON for one cycle when step execution is started with STEP(008). This flag can be used for initialization processing at the beginning of a step.	ON for the first cycle after execution of STEP(008).	Cleared	---	---	---
	A20014	Task Started Flag	When a task switches from WAIT or INI to RUN status, this flag will be turned ON within the task for one cycle only. The only difference between this flag and A20015 is that this flag also turns ON when the task switches from WAIT to RUN status.	ON for the first cycle (including transitions from WAIT and IN)	Cleared	Cleared	---	---
	A20015	First Task Startup Flag	ON when a task is executed for the first time. This flag can be used to check whether the current task is being executed for the first time so that initialization processing can be performed if necessary.	ON: First execution OFF: Not executable for the first time or not being executed.	Cleared	---	---	---
A201	A20110	Online Editing Wait Flag	ON when an online editing process is waiting. (If another online editing command is received while waiting, the other command won't be recorded and an error will occur.)	ON: Waiting for online editing OFF: Not waiting for online editing	Cleared	Cleared	---	A527
	A20111	Online Editing Flag	ON when an online editing process is being executed.	ON: Online editing in progress OFF: Online editing not in progress	Cleared	Cleared	---	A527

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A202	A20200 to A20207	Communications Port Enabled Flags	ON when a network instruction (SEND, RECV, CMND, or PMCR) can be executed with the corresponding port number. Bits 00 to 07 correspond to communications ports 0 to 7. When two or more network instructions are programmed with the same port number, use the corresponding flag as an execution condition to prevent the instructions from being executed simultaneously. (The flag for a given port is turned OFF while a network instruction with that port number is being executed.) (When the simple backup operation is used to performed a write or compare operation for a Memory Card, a communications port will be automatically allocated, and the corresponding Flag will be turned OFF.)	ON: Network instruction is not being executed OFF: Network instruction is being executed (port busy)	Cleared	---	---	---
	A20215	Network Communications Port Allocation Enabled Flag	ON when a communications instruction can be executed with automatic port allocation and there is a communications port available for automatic allocation.	ON: Network communications with automatic allocation is possible. OFF: Network communications with automatic allocation is not possible.	Cleared	Cleared	---	---
A203 to A210	All	Communications Port Completion Codes	These words contain the completion codes for the corresponding port numbers when network instructions (SEND, RECV, CMND, or PMCR) has been executed. Words A203 to A210 correspond to communications ports 0 to 7. (The completion code for a given port is cleared to 0000 when a network instruction with that port number is executed.) (When the simple backup operation is used to performed a write or compare operation for a Memory Card, a communications port will be automatically allocated, and a completion code will be stored in the corresponding word.)	Non-zero: Error code 0000: Normal	Cleared	---	---	---
A213	A21300 to A21307	Explicit Communications Error Flag (Single CPU Systems only)	Turn ON when an error occurs in executing an Explicit Message Instruction (EXPLT, EGATR, ESATR, ECHRD, or ECHWR). Bits 00 to 07 correspond to communications ports 0 to 7. The corresponding bit will turn ON both when the explicit message cannot be sent and when an error response is returned for the explicit message. The status will be maintained until the next explicit message communication is executed. The bit will always turn OFF when the next Explicit Message Instruction is executed.	1: Error end 0: Normal end	Cleared	---	---	A21900 to A21907 A203 to A210

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A214	A21400 to A21407	First Cycle Flags after Network Communications Finished	When a communications instruction is executed with automatic port allocation, the corresponding flag is turned ON for just one cycle after communications have been completed. Bits 00 to 07 correspond to ports 0 to 7. Use the Used Communications Port Number stored in A218 to determine which flag to access. **Note:** These flags are not effective until the next cycle after the communications instruction is executed. Delay accessing them for at least one cycle.	ON for the first cycle after communications have been completed, otherwise OFF	Held	Cleared	---	---
A215	A21500 to A21507	First Cycle Flags after Network Communications Error Flags	When a communications instruction was executed with automatic port allocation and an error occurred, the corresponding flag is turned ON for just one cycle. Bits 00 to 07 correspond to ports 0 to 7. Use the Used Communications Port Number stored in A218 to determine which flag to access. The cause of the error can be determined with the Communications Port Completion Codes stored in A203 to A210. **Note:** These flags are not effective until the next cycle after the communications instruction is executed. Delay accessing them for at least one cycle.	ON for the first cycle after communications error end, otherwise OFF	Held	Cleared	---	---
A216 to A217	All	Network Communications Completion Code Storage Address	When a communications instruction was executed with automatic port allocation, the response (completion) code for the communications instruction is automatically stored in the word with the PLC memory address specified in these words. **Note:** The PLC memory address specified here can be transferred to an index register in order to indirectly address the specified word and read the code.	PLC memory address of the word where the network communications response code is stored	Held	Cleared	---	---
A218	All	Used Communications Port Numbers	When a communications instruction is executed with automatic port allocation, the allocated communications port number is stored in this word. Values 0000 to 0007 hex correspond to ports 0 to 7.	0000 to 0007 hex: Ports 0 to 7.	Held	Cleared	---	---
A219	A21900 to A21907	Communications Port Error Flags	ON when an error occurred during execution of a network instruction (SEND, RECV, CMND, or PMCR). Bits 00 to 07 correspond to communications ports 0 to 7. (All of these flags are turned OFF at the start of program execution and the flag for a given port is turned OFF when a network instruction with that port number is executed.) (When the simple backup operation is used to performed a write or compare operation for a Memory Card, a communications port will be automatically allocated, and the corresponding Flag will be turned OF if an error occurs.)	ON: Error occurred OFF: Normal	Cleared	---	---	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A220 to A259	A22000 to A25915	Basic I/O Unit Input Response Times	These words contain the actual input response times for CS-series Basic I/O Units. When the Basic I/O Unit input response time setting is changed in the PLC Setup while the PLC is in PROGRAM mode, the setting in the PLC Setup will not match the actual value in the Basic I/O Unit unless the power is turned OFF and then ON again. In that case, the actual value can be monitored in these words.	0 to 17 hexadecimal	Held	See function column.	---	PLC Setup (Basic I/O Unit Input response time settings)
A261	A26100	CPU Bus Unit Setup Area Initialization Error Flag	ON: Error in CPU Bus Unit Setup Turns OFF when I/O tables are generated normally.	ON: Error in CPU Bus Unit Setup OFF: I/O tables generated normally	Held	Cleared	When I/O tables are generated	---
	A26102	I/O Overflow Flag	ON: Overflow in maximum number of I/O points Turns OFF when I/O tables are generated normally.	ON: Overflow in maximum number of I/O points OFF: I/O tables generated normally				A40111 (Too many I/O points)
	A26103	Duplication Error Flag	ON: The same unit number was used more than once. Turns OFF when I/O tables are generated normally.	ON: The same unit number was used more than once. OFF: I/O tables generated normally				A40113 (duplicated number)
	A26104	I/O Bus Error Flag	ON: I/O bus error Turns OFF when I/O tables are generated normally.	ON: I/O bus error OFF: I/O tables generated normally				A40114 (I/O but error)
	A26107	Special I/O Unit Error Flag	ON: Error in a Special I/O Unit Turns OFF when I/O tables are generated normally.	ON: Error in a Special I/O Unit OFF: I/O tables generated normally				---
	A26109	I/O Unconfirmed Error Flag	ON: I/O detection has not been completed. Turns OFF when I/O tables are generated normally.	ON: I/O detection has not been completed. OFF: I/O tables generated normally				---
	A26110	Online Replacement and Replacement Error Flag	ON: An online replacement operation is being performed. (It is treated as an I/O table creation error). This flag will be turned OFF automatically when the online replacement operation has been completed. (Do not attempt to create the I/O tables while this flag is ON.)	ON: Online replacement in progress OFF: Normal				A034 to A041
	A26111	Duplex Communications Unit Error Flag	ON: Duplex Units are not mounted for a unit number specified for Duplex Communications Units (i.e., one Unit is missing or the mounted Units do not support duplex operation).	ON: Missing Unit or non-duplex Unit OFF: I/O tables generated normally	Held	Cleared	When I/O tables are generated	A43400 to A43415
	A26112	Duplex Communications Unit Verification Error Flag	ON: The duplex setting in the PLC Setup for a unit number specified for Duplex Communications Units does not agree with the setting on the Duplex Communications Units. The I/O tables will not be created and an I/O Table Creation Error will occur. Refer to the Operation Manual for the Communications Units for details on Unit settings.	ON: Duplex Communications Unit verification error OFF: I/O tables generated normally				A435

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A262 and A263	All	Maximum Cycle Time	These words contain the maximum cycle time since the start of PLC operation. The cycle time is recorded in 8-digit hexadecimal with the leftmost 4 digits in A263 and the rightmost 4 digits in A262. With a Single CPU System in Parallel Processing Mode, the maximum cycle time for instruction execution will be stored.	0 to FFFFFFFF: 0 to 429,496,729.5 ms (0.1ms units)	---	---	---	---
A264 and A265	All	Present Cycle Time	These words contain the present cycle time in 8-digit hexadecimal with the leftmost 4 digits in A265 and the rightmost 4 digits in A264. With a Single CPU System in Parallel Processing Mode, the present cycle time for instruction execution will be stored.	0 to FFFFFFFF: 0 to 429,496,729.5 ms	---	---	---	---
A266 and A267	All	Program Execution Time	These words contain the total time for program execution with the leftmost 4 digits in A267 and the rightmost 4 digits in A266. Stores for a Single CPU System when not in Parallel Processing Mode.	00000000 to FFFFFFFF hex 0.0 to 429,496,729.5 ms (0.1-ms increments)	---	---	---	---
A268	---	Peripheral Servicing Cycle Time (Single CPU Systems only)	In Parallel Processing with Synchronous or Asynchronous Memory Access, this word contains the peripheral servicing cycle time. The time is updated every cycle and is recorded in 16-bit binary.	0 to 4E20 hex, (0.0 to 2,000.0 ms in units of 0.1 ms)	---	---	Each cycle	A40515
A270	---	Duplex Communications Cable Error Flags	ON: An error has occurred at some point in the corresponding I/O Communications Cable.	ON: Duplex Communications Cable Error OFF: Normal	Cleared	Cleared	When error occurs	A271
	A27000		CPU Rack slot 0 to Expansion Rack 1					
	A27001		CPU Rack slot 1to Expansion Rack 1					
	A27002		Expansion Rack 1 slot 0 to Rack 2					
	A27003		Expansion Rack 1 slot 1 to Rack 2					
	A27004		Expansion Rack 2 slot 0 to Rack 3					
	A27005		Expansion Rack 2 slot 1 to Rack 3					
	A27006		Expansion Rack 3 slot 0 to Rack 4					
	A27007		Expansion Rack 3 slot 1 to Rack 4					
	A27008		Expansion Rack 4 slot 0 to Rack 5					
	A27009		Expansion Rack 4 slot 1 to Rack 5					
	A27010		Expansion Rack 5 slot 0 to Rack 6					
	A27011		Expansion Rack 5 slot 1 to Rack 6					
	A27012		Expansion Rack 6 slot 0 to Rack 7					
	A27013		Expansion Rack 6 slot 1 to Rack 7					
A271	---	Duplex Communications Cable Status Flags	Indicate when the corresponding I/O Communications Cable is duplexed. (ON when duplexed.)	ON: Communications Cable duplexed OFF: Communications Cable not duplexed	Cleared	Cleared	Each cycle	A270
	A27100		CPU Rack to Expansion Rack 1					
	A27101		Expansion Rack 1 to Rack 2					
	A27102		Expansion Rack 2 to Rack 3					
	A27103		Expansion Rack 3 to Rack 4					
	A27104		Expansion Rack 4 to Rack 5					
	A27105		Expansion Rack 5 to Rack 6					
	A27107		Expansion Rack 6 to Rack 7					

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A272	A27215	Online Addition Failed Flag	ON: An error occurred that prevented a Backplane and Unit from being added online.	OFF → ON: An error prevented a Backplane or Unit from being added online.	Cleared	Cleared	Each cycle	---
A273	---	Online Addition Failure Cause Flags	When an error occurred that prevented a Backplane and Unit from being added online, the relevant flag will be turned ON.	OFF → ON: The corresponding error prevented a Backplane or Unit from being added online.	Cleared	Cleared	Each cycle	---
	A27300		Transmitted I/O tables are invalid (changed or deleted).					
	A27301		Basic I/O Unit mounted in an invalid slot.					
	A27302		No Unit mounted in the added slot.					
	A27303		Specified an Expansion Backplane addition to an earlier CPU Backplane version.					
	A27304		A CPU Bus Unit was added.					
	A27305		The added Unit's model is different from the Unit that was specified to be mounted.					
	A27306		The added Basic I/O Unit's allocated words duplicate the words of an existing Unit.					
	A27307		The added unit number duplicates an existing unit number.					
	A27308		The number of I/O points exceeds the maximum (5,120 I/O points).					
	A27309		There is an error in the added Expansion Backplane (power supply OFF).					
A294	All	Task Number when Program Stopped	This word contains the task number of the task that was being executed when program execution was stopped because of a program error. (A298 and A299 contain the program address where program execution was stopped.)	Normal tasks: 0000 to 001F (task 0 to 31)	Cleared	Cleared	---	A298/ A299
A295	A29508	Instruction Processing Error Flag	This flag and the Error Flag (ER) will be turned ON when an instruction processing error has occurred and the PLC Setup has been set to stop operation for an instruction error. CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON. (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	ON: Error Flag ON OFF: Error Flag OFF	Cleared	Cleared	---	A294, A298/ A299 PLC Setup (Operation when instruction error has occurred)
	A29509	Indirect DM/EM BCD Error Flag	This flag and the Access Error Flag (AER) will be turned ON when an indirect DM/EM BCD error has occurred and the PLC Setup has been set to stop operation an indirect DM/EM BCD error. (This error occurs when the content of an indirectly addressed DM or EM word is not BCD although BCD mode has been selected.) CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON. (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	ON: Not BCD OFF: Normal	Cleared	Cleared	---	A294, A298/ A299 PLC Setup (Operation when instruction error has occurred)

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A295	A29510	Illegal Access Error Flag	This flag and the Access Error Flag (AER) will be turned ON when an illegal access error has occurred and the PLC Setup has been set to stop operation an illegal access error. (This error occurs when a region of memory is access illegally.) CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON. The following operations are considered illegal access: Reading/writing the system area Reading/writing EM File Memory Writing to a write-protected area Indirect DM/EM BCD error (in BCD mode) (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	ON: Illegal access occurred OFF: Normal	Cleared	Cleared	---	A294, A298/ A299 PLC Setup (Operation when instruction error has occurred)
	A29511	No END Error Flag	ON when there isn't an END(001) instruction in each program within a task. CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON. (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	ON: No END OFF: Normal	Cleared	Cleared	---	A294, A298/ A299
	A29512	Task Error Flag	ON when a task error has occurred. The following conditions generate a task error. •There isn't even one regular task that is executable (started). •There isn't a program allocated to the task. (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	ON: Error OFF: Normal	Cleared	Cleared	---	A294, A298/ A299
	A29513	Differentiation Overflow Error Flag	The allowed value for Differentiation Flags which correspond to differentiation instructions has been exceeded. CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON. (The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299.)	ON: Error OFF: Normal	Cleared	Cleared	---	A294, A298/ A299
	A29514	Illegal Instruction Error Flag	ON when a program that cannot be executed has been stored. CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON.	ON: Error OFF: Normal	Cleared	Cleared	---	A294, A298/ A299
	A29515	UM Overflow Error Flag	ON when the last address in UM (User Memory) has been exceeded. CPU Unit operation will stop and the ERR/ALM indicator will light when this flag goes ON.	ON: Error OFF: Normal	Cleared	Cleared	---	A294, A298/ A299

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	Bits							
A298	All	Program Address Where Program Stopped (Rightmost 4 digits)	These words contain the 8-digit binary program address of the instruction where program execution was stopped due to a program error. (A294 contains the task number of the task where program execution was stopped.)	Right 4 digits of the program address	Cleared	Cleared	---	A294
A299	All	Program Address Where Program Stopped (Leftmost 4 digits)		Left 4 digits of the program address	Cleared	Cleared	---	
A300	All	Error Log Pointer	When an error occurs, the Error Log Pointer is incremented by 1 to indicate the location where the next error record will be recorded as an offset from the beginning of the Error Log Area (A100 to A199). The Error Log Pointer can be cleared to 00 by turning A50014 (the Error Log Reset Bit) from OFF to ON. When the Error Log Pointer has reached 14 (20 decimal), the next record is stored in A195 to A199 when the next error occurs.	00 to 14 hexadecimal	Held	Held	When error occurs	A50014
A301	All	Current EM Bank	This word contains the current EM bank number in 4-digit hexadecimal. The current bank number can be changed with the EMBC(281) instruction.	0000 to 000C hex	Cleared	Cleared	---	---
A302	A30200 to A30215	CPU Bus Unit Initializing Flags	These flags are ON while the corresponding CPU Bus Unit is initializing after its CPU Bus Unit Restart Bit (A50100 to A50115) is turned from OFF to ON or the power is turned ON. Bits 00 to 15 correspond to unit numbers 0 to 15. Use these flags in the program to prevent the CPU Bus Unit's refresh data from being used while the Unit is initializing. IORF(097) cannot be executed while an CPU Bus Unit is initializing. These bits are turned OFF automatically when initialization is completed.	ON: Initializing (Reset to 0 automatically after initialization.) OFF: Not initializing	Held	Cleared	Written during initialization	A50100 to A50115

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A310		Rightmost Digits of Production Lot Number Information (CPU Units for Single CPU Systems with unit version 2.1 or later or CPU Units for CS1D Duplex-CPU Systems with unit version 1.4 or later)	These words contain the production lot number in 6 binary digits. Example: Lot No. 150701 A310 = 0701 A311 = 0015		Held	Held	When power is turned ON	
A311		Leftmost Digits of Production Lot Number Information (CPU Units for Single CPU Systems with unit version 2.1 or later or CPU Units for CS1D Duplex-CPU Systems with unit version 1.4 or later)						
A316	A31600	Duplex Verification Error Flag (Duplex CPU System only)	ON: An inconsistency exists between the program or memory of the active and standby CPU Units in Duplex Mode. (Refer to A317 and A804 for details.)	ON: Duplex verification error OFF: Normal	Cleared	Cleared	When error occurs	A317
	A31601	Duplex Bus Error Flag (Duplex CPU System only)	ON: An error occurred on the sync transfer bus in the duplex mode.	ON: Duplex bus error OFF: Normal				---
	A31602	Duplex Power Supply Unit Error Flag	ON: An error occurred in the Power Supply Unit or power supply system on a duplex CPU Rack, Expansion Rack, or Long-distance Expansion Rack. Error details are stored in A319 and A320.	ON: Duplex power error OFF: Normal				A319 A320
	A31603	Duplex Communications Error Flag	ON: One of the duplex Communications Units has failed. (Refer to A434 to A437 for details.)	ON: Communications error OFF: Normal				A434 to A437

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A317	**Duplex Verification Errors (Duplex CPU Systems only)** (When A31600 turns ON, the cause of the error will be indicated here.)							
	A31706	Other CPU Unit Duplex Verification Error Flag (Duplex CPU System only)	ON: A duplex error occurred in the other CPU Unit when entering Duplex Mode. The "other CPU Unit" indicates the standby CPU Unit for the active CPU Unit and the active CPU Unit for the standby CPU Unit.	ON: Verification error OFF: Normal	Cleared	Cleared	When error occurs	A31600
	A31707	CPU Unit Model Verification Error Flag	ON: The CPU Units were not the same model when entering Duplex Mode.	ON: Verification error OFF: Normal	Cleared	Cleared	When error occurs	
	A31708	CPU Unit Version Verification Error Flag	ON: The unit version of the standby CPU Unit is earlier than the unit version of the active CPU Unit and the active CPU Unit uses function not supported by the standby CPU Unit.	ON: Verification error OFF: Normal				
	A31710	Inner Board Model Verification Error Flag	ON: The duplex Inner Boards in the two Process-control CPU Units were not the same model when entering Duplex Mode.	ON: Verification error OFF: Normal				
	A31713	Parameter Area Verification Error Flag	ON: The parameter area in the two CPU Units in duplex mode do not have the same contents.	ON: Verification error OFF: Normal				
	A31714	No Active CPU Unit Error Flag (Duplex CPU System only)	ON: When the power is ON, the CPU Unit set to standby in duplex mode detected that the active CPU is missing. This happens in the following cases. • The active CPU Unit is not mounted. • The use active CPU setting switch is set to NO USE. • Because DIP Switch Pin 7 is ON on the active CPU Unit, simple backup (reading from memory card to CPU Unit) is set. • A DIP switch setting error has occurred on the active CPU Unit.	ON: No active CPU Unit OFF: Normal	Cleared	Cleared	When power is turned ON	
	A31715	User Program Verification Error Flag	ON: The user program in the two CPU Units in duplex mode do not have the same contents.	ON: Verification error OFF: Normal	Cleared	Cleared	When error occurs	

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A319	**Error Power Supply Unit Location** When an error in a Power Supply Unit results in an error in the 5-V/26-V output, one of the following bits will turn ON to show the location of the Power Supply Unit with the error. A31602 (Duplex Power Supply Unit Error Flag) can be used to determine if there is an error and the following bits can be used to locate the error.							
	A31900	Right Power Supply Unit on CPU Rack (Rack 0)		ON: Power Supply Unit error OFF: Normal	Cleared	Cleared	When error occurs	A31602
	A31901	Left Power Supply Unit on CPU Rack (Rack 0)						
	A31902	Right Power Supply Unit on CPU Rack (Rack 1)						
	A31903	Left Power Supply Unit on CPU Rack (Rack 1)						
	A31904	Right Power Supply Unit on CPU Rack (Rack 2)						
	A31905	Left Power Supply Unit on CPU Rack (Rack 2)						
	A31906	Right Power Supply Unit on CPU Rack (Rack 3)						
	A31907	Left Power Supply Unit on CPU Rack (Rack 3)						
	A31908	Right Power Supply Unit on CPU Rack (Rack 4)						
	A31909	Left Power Supply Unit on CPU Rack (Rack 4)						
	A31910	Right Power Supply Unit on CPU Rack (Rack 5)						
	A31911	Left Power Supply Unit on CPU Rack (Rack 5)						
	A31912	Right Power Supply Unit on CPU Rack (Rack 6)						
	A31913	Left Power Supply Unit on CPU Rack (Rack 6)						
	A31914	Right Power Supply Unit on CPU Rack (Rack 7)						
	A31915	Left Power Supply Unit on CPU Rack (Rack 7)						
A320	**Error Power Supply Unit Location** When the voltage on the primary side of the Power Supply Unit drops or is interrupted, one of the following bits will turn ON to show the location of the Power Supply Unit with the error. A31602 (Duplex Power Supply Unit Error Flag) can be used to determine if there is an error and the following bits can be used to locate the error.							
	A32000	Right Power Supply Unit on CPU Rack (Rack 0)		ON: Primary-side input power error OFF: Normal	Cleared	Cleared	When error occurs	A31602
	A32001	Left Power Supply Unit on CPU Rack (Rack 0)						
	A32002	Right Power Supply Unit on CPU Rack (Rack 1)						
	A32003	Left Power Supply Unit on CPU Rack (Rack 1)						
	A32004	Right Power Supply Unit on CPU Rack (Rack 2)						
	A32005	Left Power Supply Unit on CPU Rack (Rack 2)						
	A32006	Right Power Supply Unit on CPU Rack (Rack 3)						
	A32007	Left Power Supply Unit on CPU Rack (Rack 3)						
	A32008	Right Power Supply Unit on CPU Rack (Rack 4)						
	A32009	Left Power Supply Unit on CPU Rack (Rack 4)						
	A32010	Right Power Supply Unit on CPU Rack (Rack 5)						
	A32011	Left Power Supply Unit on CPU Rack (Rack 5)						
	A32012	Right Power Supply Unit on CPU Rack (Rack 6)						
	A32013	Left Power Supply Unit on CPU Rack (Rack 6)						
	A32014	Right Power Supply Unit on CPU Rack (Rack 7)						
	A32015	Left Power Supply Unit on CPU Rack (Rack 7)						

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A322	**CPU Standby Information**							
	A32203	CPU Bus/ Special I/O Unit Startup Flag	ON: The CPU Unit is on standby waiting for CPU Bus or Special I/O Units to start.	ON: Standby OFF: Other	Held	Cleared	When CPU Unit goes on standby	---
	A32204	Duplex Bus Error Standby Flag	ON: The CPU Unit is on standby because a duplex bus error occurred at startup. (Duplex CPU System only)					
	A32205	Duplex Verification Error Standby Flag	ON: The CPU Unit is on standby because a duplex verification error occurred at startup. (Duplex CPU System only)					
	A32206	Waiting for Other CPU Unit Standby Flag	ON: The CPU Unit is on standby waiting for the other CPU Unit to start operation at startup. (Duplex CPU System only)					
	A32207	Inner Board Startup Flag	ON: The CPU Unit is on standby waiting for an Inner Board to start. (Single CPU Systems or Process-control CPU Units only)					
	A32208	Expansion Power OFF Standby Flag	ON: The CPU Unit is on standby because power is not being supplied to an Expansion Rack.					
A324	A32406	Inner Board Error Flags (Non-fatal error) (Duplex CPU System only)	ON if A40208 turns ON for the right Inner Board.	ON: Non-fatal Inner Board Error OFF: Normal	Cleared	Cleared	When error occurs	A402
	A32407		ON if A40208 turns ON for the left Inner Board.					
	A32411	Right/Left CPU Unit Battery Error Flags (Duplex CPU System only)	ON if A40204 is ON in the right CPU Unit.	ON: Battery error OFF: Normal	Cleared	Cleared	When error occurs	A402
	A32413		ON if A40204 is ON in the left CPU Unit.					A402
A325	A32515	This CPU Unit Location Flag	Indicates where this CPU Unit is mounted. (Duplex CPU System only)	ON: Right side OFF: Left side	Held	---	When power is turned ON	---
A327	A32700 to A32703	Duplex CPU Compatible Setting Operating Mode (CS1D-CPU67HA only)	Indicates the mode in which the CPU Unit is currently operating in the Duplex CPU compatible setting.	0 hex: CPU model which does not support Duplex CPU compatible setting 1 hex: Not set 2 hex: CPU65H mode 3 hex: CPU67H mode	Held	Cleared	When power is turned ON	A40315
	A32704 to A32707	Duplex CPU Compatible Setting DIP Switch Setting (CS1D-CPU67HA only)	The Duplex CPU compatible setting set by the DIP switches is saved.	0 hex: CPU model which does not support Duplex CPU compatible setting 1 hex: Not set 2 hex: CPU65H mode 3 hex: CPU67H mode	Held	Cleared	When power is turned ON	A40315

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A328	A32808	Duplex/ Simplex Mode Flag (Duplex CPU Systems only)	Indicates the current mode. A32808 is turned OFF in duplex initialization and thus cannot be used alone to detect errors causing a switch to Simplex Mode. Use A32808 together with A43915 as shown below. The Duplex Initialization Flag is also used for write processing in online editing, when the initialize switch is pressed, when processing commands from communications or Programming Devices, etc.	ON: Duplex OFF: Simplex	Held	---	When power is turned ON or duplex operation started	---
	A32809	Active CPU Unit Location Flag	Indicates which CPU Unit is the active CPU Unit.	ON: Right CPU Unit OFF: Left CPU Unit		---		---
	A32810 A32811	Duplex System Configuration Flags	Indicates the system configuration, CS1H CPU Units or CS1D CPU Units. A32810 OFF, A32811 OFF: CS1-H CPU Unit A32810 ON, A32811 OFF: CS1D CPU Unit for Single CPU System A32810 ON, A32811 ON: CS1D CPU Unit for Duplex CPU System		Held	---	When power is turned ON	---
	A32814	Right CPU Unit Duplex Recovery Failed Flag (Duplex CPU Systems only)	ON: The right CPU Unit failed to recover duplex operation in Duplex Mode even after the error was cleared and an attempt was made to recover duplex operation automatically.	ON: Automatic recovery failed OFF: Automatic recovery successful or switch not made to simplex operation	Held	Cleared	When duplex operation is recovered	---
	A32815	Left CPU Unit Duplex Recovery Failed Flag (Duplex CPU Systems only)	ON: The left CPU Unit failed to recover duplex operation in Duplex Mode even after the error was cleared and an attempt was made to recover duplex operation automatically.					---
A330 to A335	A33000 to A33515	Special I/O Unit Initializing Flags	These flags are ON while the corresponding Special I/O Unit is initializing after its Special I/O Unit Restart Bit (A50200 to A50715) is turned from OFF to ON or the power is turned ON. The bits in these words correspond to unit numbers 0 to 95 as follows: A33000 to A33015: Units 0 to 15 A33100 to A33115: Units 16 to 31 ---- A33500 to A33515: Units 80 to 95 Use these flags in the program to prevent the Special I/O Unit's refresh data from being used while the Unit is initializing. Also, IORF(097) cannot be executed while a Special I/O Unit is initializing. These bits are turned OFF automatically when initialization is completed.	ON: Initializing OFF: Not initializing (Turned OFF automatically after initialization.)	Held	Cleared	---	A50200 to A50715
A339 and A340	All	Maximum Differentiation Flag Number	These words contain the maximum value of the differentiation flag numbers being used by differentiation instructions.	---	See Function column.	Cleared	Written at the start of operation	A29513

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A341	**File Memory Information for Left CPU Unit (Duplex CPU Systems only)**							
	A34100 to A34102	Memory Card Type	Indicates the type of Memory Card, if any, installed in the left CPU Unit.	0 hex: None 4 hex: Flash ROM	Held	---	When power is turned ON or Card power switch is pressed	A34300 to A34302
	A34106	EM File Memory Format Error Flag	Turns ON when a format error occurs in the first EM bank allocated for file memory in the left CPU Unit. Turns OFF when formatting is completed normally.	ON: Format error OFF: No format error	Held	Cleared	---	A34306
	A34107	Memory Card Format Error Flag	ON when the Memory Card is not formatted or a formatting error has occurred in the left CPU Unit. This flag turns OFF when the Memory Card is formatted normally.	ON: Format error OFF: No format error	Retained	---	When power is turned ON or Card power switch is pressed	A34307
	A34108	File Transfer Error Flag	ON when an error occurred while writing data to file memory in the left CPU Unit. This flag turns OFF when data is written normally.	ON: Error OFF: No error	Held	Cleared	When a file is written	A34308
	A34109	File Write Error Flag	ON when data cannot be written to file memory because it is write-protected or the data exceeds the capacity of the file memory in the left CPU Unit. This flag turns OFF when data is written normally.	ON: Write not possible OFF: Normal	Held	Cleared	When a file is written	A34309
	A34110	File Read Error	ON when a file could not be read because of a malfunction (file is damaged or data is corrupted) in the left CPU Unit. This flag turns OFF when a file is read normally	ON: Read not possible OFF: Normal	Held	Cleared	When a file is read	A34310
	A34111	File Missing Flag	ON when an attempt is made to read a file that doesn't exist or an attempt is made to write to a file in a directory that doesn't exist in the left CPU Unit. This flag turns OFF when a file is read normally.	ON: Specified file or directory is missing OFF: Normal	Held	Cleared	When a file is read	A34311
	A34113	File Memory Operation Flag	ON while any of the following operations is being executed in the left CPU Unit. OFF when none of them are being executed. CMND instruction sending a FINS command to the local CPU Unit. FREAD/FWRIT instructions. Program replacement using the control bit in the Auxiliary Area. Simple backup operation.	ON: Instruction being executed. OFF: Instruction not being executed.	Held	Cleared	When a file memory instruction is executed	A34313
	A34114	Accessing File Data Flag	ON while file data is being accessed in the left CPU Unit for one of the following: Only one instruction can be executed at a time for the file memory. Use this flag to control execution exclusively.	ON: File being accessed OFF: File not being accessed	Held	Cleared	---	A34314
	A34115	Memory Card Detected Flag	ON when a Memory Card has been detected in the left CPU Unit. OFF when a Memory Card has not been detected.	ON: Memory Card detected OFF: Memory Card not detected	Held	Cleared	When Memory Card is mounted or power is turned ON	A34315

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A342	**File Memory Information for Right CPU Unit (Duplex CPU Systems only)**							
	A34200 to A34202	Memory Card Type	Indicates the type of Memory Card, if any, installed in the right CPU Unit.	0 hex: None 4 hex: Flash ROM (A34202 is ON for flash ROM.)	Held	---	When power is turned ON or Card power switch is pressed	A34300 to A34302
	A34206	EM File Memory Format Error Flag	Turns ON when a format error occurs in the first EM bank allocated for file memory in the right CPU Unit. Turns OFF when formatting is completed normally.	ON: Format error OFF: No format error	Held	Cleared	---	A34306
	A34207	Memory Card Format Error Flag	ON when the Memory Card is not formatted or a formatting error has occurred in the right CPU Unit. This flag turns OFF when the Memory Card is formatted normally.	ON: Format error OFF: No format error	Retained	---	When power is turned ON or Card power switch is pressed	A34307
	A34208	File Transfer Error Flag	ON when an error occurred while writing data to file memory in the right CPU Unit. This flag turns OFF when data is written normally.	ON: Error OFF: No error	Held	Cleared	When a file is written	A34308
	A34209	File Write Error Flag	ON when data cannot be written to file memory because it is write-protected or the data exceeds the capacity of the file memory in the right CPU Unit. This flag turns OFF when data is written normally.	ON: Write not possible OFF: Normal	Held	Cleared	When a file is written	A34309
	A34210	File Read Error	ON when a file could not be read because of a malfunction (file is damaged or data is corrupted) in the right CPU Unit. This flag turns OFF when a file is read normally	ON: Read not possible OFF: Normal	Held	Cleared	When a file is read	A34310
	A34211	File Missing Flag	ON when an attempt is made to read a file that doesn't exist or an attempt is made to write to a file in a directory that doesn't exist in the right CPU Unit. This flag turns OFF when a file is read normally.	ON: Specified file or directory is missing OFF: Normal	Held	Cleared	When a file is read	A34311
	A34213	File Memory Operation Flag	ON while any of the following operations is being executed in the right CPU Unit. OFF when none of them are being executed. Memory Card detection started. CMND instruction sending a FINS command to the local CPU Unit. FREAD/FWRIT instructions. Program replacement using the control bit in the Auxiliary Area. Simple backup operation. If this flag is ON, write and comparison operations to the Memory Card cannot be executed.	ON: Instruction being executed. OFF: Instruction not being executed.	Held	Cleared	When a file memory instruction is executed	A34313
	A34214	Accessing File Data Flag	ON while file data is being accessed in the right CPU Unit. Only one instruction can be executed at a time for the file memory. Use this flag to control execution exclusively.	ON: File being accessed OFF: File not being accessed	Held	Cleared	---	A34314
	A34215	Memory Card Detected Flag	ON when a Memory Card has been detected in the right CPU Unit. OFF when a Memory Card has not been detected.	ON: Memory Card detected OFF: Memory Card not detected	Held	Cleared	When Memory Card is mounted or power is turned ON	A34315

Address		Name	Function			Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**									
A343	A34300 to A34302	File Memory Status With Duplex CPU Systems, Active CPU Unit File Memory Status **Note:** For duplex Memory Card operation with Duplex CPU Systems, the file-memory status is given for the active and standby CPU Units.	**Memory Card Type** The type of Memory Card mounted in the CPU Unit is stored. With Duplex CPU Systems Memory Card duplex operation disabled: Memory Card type for active CPU Unit is stored. Memory Card duplex operation enabled: Memory Card type is stored only when mounted in both CPU Units.	Flash ROM	A343 00	0	Held	---	When power is turned ON or when Memory Card power is turned ON	---
					A343 01	0				
					A343 02	1				
				Not mounted	A343 00	0				
					A343 01	0				
					A343 02	0				
	A34306		**EM File Memory Area Format Error Flag** ON when a format error occurs in the area from the EM file memory beginning bank number. **Note:** Turns OFF when format is normal.		ON when A341 06 or A342 06 turns ON	1: Format error 0: Normal	Held	Cleared	---	---
	A34307		**Memory Card Format Error Flag** ON when a Memory Card is mounted if the Memory Card is not formatted, or if there is an error in the format. With Duplex CPU Systems Memory Card duplex operation disabled: ON when an error occurs at the active CPU Unit. Memory Card duplex operation enabled: ON when an error occurs at either the active or standby CPU Unit. **Note:** Turns OFF when format is normal.		ON when A341 07 or A342 07 turns ON	1: Format error 0: Normal	Held	---	When power is turned ON or when Memory Card power is turned ON	---
	A34308		**File Write Error Flag** ON when an error occurs while writing a file to the active CPU Unit. With Duplex CPU Systems Memory Card duplex operation disabled: ON when an error occurs at the active CPU Unit. Memory Card duplex operation enabled: ON when an error occurs at either the active or standby CPU Unit. **Note:** Turns OFF when operation begins or when a file is written normally.		ON when A341 08 or A342 08 turns ON	1: Write error 0: Normal	Held	Cleared	When writing a file	---

Address		Name	Function		Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**								
A343	A34309	File Memory Status With Duplex CPU Systems, Active CPU Unit File Memory Status **Note:** For duplex Memory Card operation with Duplex CPU Systems, the file-memory status is given for the active and standby CPU Units.	**Cannot Write File Flag** ON when data cannot be written to file memory because it is write-protected or the data exceeds the capacity of the file memory. With Duplex CPU Systems Memory Card duplex operation disabled: ON when writing is impossible at the active CPU Unit. Memory Card duplex operation enabled: ON when writing is impossible at the active or at the standby CPU Unit. **Note:** Turns OFF when operation begins or when a file is written normally.	ON when A34109 or A34209 turns ON	1: Write not possible 0: Normal	Held	Cleared	When writing a file	---
	A34310		**File Read Error Flag** ON when a file could not be read (file is damaged or data is corrupted). With Duplex CPU Systems Memory Card duplex operation disabled: ON when an error occurs at the active CPU Unit. Memory Card duplex operation enabled: ON when an error occurs at either the active or standby CPU Unit. **Note:** Turns OFF when operation begins or when a file is read normally.	ON when A34110 or A34210 turns ON	1: Read error 0: Normal	Held	Cleared	When reading a file	---
	A34311		**File Missing Flag** ON when an attempt is made to read a file that doesn't exist or an attempt is made to write to a file in a directory that doesn't exist. With Duplex CPU Systems Memory Card duplex operation disabled: ON when an error occurs at the active CPU Unit. Memory Card duplex operation enabled: ON when an error occurs at either the active or standby CPU Unit. **Note:** Turns OFF when operation begins or when a file is read normally.	ON when A34111 or A34211 turns ON	ON: Specified file or directory is missing OFF: Normal	Held	Cleared	When reading a file	---

Address		Name	Function		Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**								
A343	A34313	File Memory Status With Duplex CPU Systems, Active CPU Unit File Memory Status **Note:** For duplex Memory Card operation with Duplex CPU Systems, the file-memory status is given for the active and standby CPU Units.	**File Memory Operation Flag** ON while any of the following operations is being executed. OFF when none of them are being executed. CMND instruction sending a command to the local CPU Unit. FREAD/FWRIT instructions. Program replacement using the control bit in the Auxiliary Area. Simple backup operation. With Duplex CPU Systems Memory Card duplex operation disabled: ON during operation at the active CPU Unit. Memory Card duplex operation enabled: ON during operation at either the active or standby CPU Unit. **Note:** Turns OFF when operation begins.	ON when A341 13 or A342 13 turns ON	ON: Instruction being executed. OFF: Instruction not being executed.	Held	Cleared	When file memory instructions are executed	---
	A34314		**Accessing File Data Flag** ON while file data is being accessed. With Duplex CPU Systems Memory Card duplex operation disabled: ON when file data is being accessed at the active CPU Unit. Memory Card duplex operation enabled: ON when file data is being accessed at either the active or standby CPU Unit. **Note:** Only one instruction can be executed at a time for the file memory. Use this flag to control execution exclusively. **Note:** Turns OFF when operation begins.	ON when A341 14 or A342 14 turns ON	ON: File being accessed OFF: File not being accessed	Held	Cleared	---	---
	A34315		**Memory Card Detected Flag** ON when a Memory Card has been detected. With Duplex CPU Systems OFF when a Memory Card has not been detected. Standby write disabled: ON when a Memory Card has been detected at the active CPU Unit. Standby write enabled: ON when a Memory Card has been detected at either CPU Unit.		ON: Memory Card detected OFF: Memory Card not detected	Held	Cleared	When Memory Card is mounted or when power is turned ON	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A344	All	EM File Memory Starting Bank	Contains the starting bank number of EM file memory (bank number of the first formatted bank). All EM banks from this starting bank to the last bank in EM are formatted for use as file memory. To convert the EM Area for use as file memory, first set the PLC Setup's EM File Memory Function setting to 1, set the PLC Setup's EM File Memory Starting Bank setting (0 to 18), and then format the EM Area from a Programming Device The PLC Setup's EM file memory settings won't agree with the actual settings unless the EM Area is formatted after the PLC Setup's EM file memory settings have been changed. In that case, the actual settings can be determined with this word.	0000 to 0018 hex Bank 0 to 18	Held	Held	When EM file formatting is performed	PLC Setup (EM File Memory Function setting and EM File Memory Starting Bank setting)
A345	A34500	FB Program Data Flag (Unit version 4.0 or later)	Turns ON if the FB program memory contains FB program data.		Held	Held	When the program is downloaded	
	A34501	Symbol Table File Flag (Unit version 4.0 or later)	Turns ON when the comment memory contains a symbol table file.					
	A34502	Comment File Flag (Unit version 4.0 or later)	Turns ON when the comment memory contains a comment file.					
	A34503	Program Index File Flag (Unit version 4.0 or later)	Turns ON when the comment memory contains a program index file.					
A346 and A347	All	Number of Remaining Words to Transfer	These words contain the 8-digit hexadecimal number of words remaining to be transferred by FREAD(700) or FWRIT(701). When one of these instructions is executed, the number of words to be transferred is written to A346 and A347. While the data is being transferred, the value in these words is decremented. A326 contains the rightmost 4-digits and A347 contains the leftmost 4-digits. Check the content of these words to determine whether or not the planned number of words have been transferred successfully.	Data remaining in transfer	Held	Cleared	Written as FREAD or FWRIT is being executed. Decremented as data is actually transferred.	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A351 to A354	All	Calendar/ Clock Area	These words contain the CPU Unit's internal clock data in BCD. The clock can be set from a Programming Device such as a Programming Console, with the DATE(735) instruction, or with a FINS command (CLOCK WRITE, 0702).	---	Held	Held	Written every cycle	---
	A35100 to A35107		Seconds (00 to 59) (BCD)					
	A35108 to A35115		Minutes (00 to 59) (BCD)					
	A35200 to A35207		Hours (00 to 23) (BCD)					
	A35208 to A35215		Day of the month (01 to 31) (BCD)					
	A35300 to A35307		Month (01 to 12) (BCD)					
	A35308 to A35315		Year (00 to 99) (BCD)					
	A35400 to A35407		Day of the week (00 to 06) (BCD) 00: SUN, 01: MON, 02: TUE, 03: WED, 04: THU,05: FRI, 06: SAT					
A355	A35500 to A35515	Inner Board Monitoring Area (Single CPU Systems or Process-control CPU Units only)	The function of these words is defined by the Inner Board.	---	Determined by Inner Board	Determined by Inner Board	---	---
A360 to A391	A36001 to A39115	Executed FAL Number Flags	The flag corresponding to the specified FAL number will be turned ON when FAL(006) is executed. Bits A36001 to A39115 correspond to FAL numbers 001 to 511. The flag will be turned OFF when the error is cleared.	ON: That FAL was executed OFF: That FAL wasn't executed	Held	Cleared	When error occurs	A40215

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A392	A39204	RS-232C Port Error Flag	ON when an error has occurred at the RS-232C port. (Not valid in peripheral bus mode or NT Link mode.)	ON: Error OFF: No error	Held	Cleared	When error occurs	A528
	A39205	RS-232C Port Send Ready Flag (No-protocol mode)	ON when the RS-232C port is able to send data in no-protocol mode.	ON: Able-to-send OFF: Unable-to-send	Held	Cleared	Written after transmission	---
	A39206	RS-232C Port Reception Completed Flag (No-protocol mode)	ON when the RS-232C port has completed the reception in no-protocol mode. When the number of bytes was specified: ON when the specified number of bytes is received. When the end code was specified: ON when the end code is received or 256 bytes are received.	ON: Reception completed OFF: Reception not completed	Held	Cleared	Written after reception	---
	A39207	RS-232C Port Reception Overflow Flag (No-protocol mode)	ON when a data overflow occurred during reception through the RS-232C port in no-protocol mode. When the number of bytes was specified: ON when more data is received after the reception was completed but before RXD(235) was executed. When the end code was specified: ON when more data is received after the end code was received but before RXD(235) was executed. ON when 257 bytes are received before the end code.	ON: Overflow OFF: No overflow	Held	Cleared	---	---
	A39212	Peripheral Port Communications Error Flag	ON when a communications error has occurred at the peripheral port. (Not valid in peripheral bus mode or NT Link mode.)	ON: Error OFF: No error	Held	Cleared	---	---
A393	A39300 to A39307	RS-232C Port PT Communications Flag	The corresponding bit will be ON when the RS-232C port is communicating with a PT in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	ON: Communicating OFF: Not communicating	Held	Cleared	When there is a normal response to the token	---
	A39308 to A39315	RS-232C Port PT Priority Registered Flags	The corresponding bit will be ON for the PT that has priority when the RS-232C port is communicating in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	ON: Priority registered OFF: Priority not registered	Held	Cleared	See *Function* column.	---
	A39300 to A39315	RS-232C Port Reception Counter (No-protocol mode)	Indicates (in binary) the number of bytes of data received when the RS-232C port is in no-protocol mode.	---	Held	Cleared	When data is received	---
A394	A39400 to A39407	Peripheral Port PT Communications Flag	The corresponding bit will be ON when the peripheral port is communicating with a PT in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	ON: Communicating OFF: Not communication	Held	Cleared	When there is a normal response to the token	---
	A39408 to A39415	Peripheral Port PT Priority Registered Flags	The corresponding bit will be ON for the PT that has priority when the peripheral port is communicating in NT link mode. Bits 0 to 7 correspond to units 0 to 7.	ON: Priority registered OFF: Priority not registered	Held	Cleared	See *Function* column.	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A395	A39506	File Deleted Flags	ON when the system deleted the remainder of a Memory Card file that was being updated when a power interruption occurred.	ON: File deleted OFF: No files deleted	Cleared	Cleared	When system deletes the file.	---
	A39507		ON when the system deleted the remainder of an EM file memory file that was being updated when a power interruption occurred.	ON: File deleted OFF: No files deleted	Cleared	Cleared	When system deletes the file.	---
	A39510	ER/AER Flag for Background Execution (Single CPU System only)	Turns ON if an error or illegal access occurs during background execution. Turns OFF when power is turned ON or operation is started.	1: Error 0: No error (Cleared when background execution is started.)	Cleared	Cleared	---	---
	A39511	Memory Corruption Detected Flag	ON when memory corruption is detected when the power supply is turned ON.	ON: Memory corruption OFF: Normal operation	Held	See Function column.	When power is turned ON.	---
	A39512	DIP Switch Status Flag	Shows the ON/OFF status of the following switches depending on the system. Duplex CPU Systems: Status of the "A39512" switch on the DIP switch on the front of the Duplex Unit. Single CPU Systems: Status of the pin 6 on the DIP switch on the front of the CPU Unit.	ON: Pin 6 ON OFF: Pin 6 OFF	Held	See Function column.	Written every cycle	---
A397	---	Simple Backup Write Capacity	If a write for a simple backup operation fails, A397 will contain the Memory Card capacity that would have been required to complete the write operation. The value is in Kbytes. (This indicates that the Memory Card did not have the specified capacity when the write operation was started.) A397 will be cleared to 0000 hex when the write is completed successfully for a simple backup operation.	0000 hex: Write completed normally 0001 to FFFF hex: Write error (value indicates required capacity from 1 to 65,535 Kbytes).	Held	Held	When write is executed	---
A400	All	Error code	When a non-fatal error (user-defined FALS(006) or system error) or a fatal error (user-defined FALS(007) or system error) occurs, the 4-digit hexadecimal error code is written to this word. When two or more errors occur simultaneously, the highest error code will be recorded. Refer to page 574 for details on error codes.	Error code	Cleared	Cleared	When error occurs	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A401	A40106	FALS Error Flag (Error causing switch to simplex operation)	ON when a non-fatal error is generated by the FALS(006) instruction. The ERR/ALM indicator will flash. The corresponding error code will be written to A400. Error codes C101 to C2FF correspond to FALS numbers 001 to 511. With a Single CPU System, CPU Unit operation will stop. With a Duplex CPU System in Duplex Mode, operation will switch to the standby CPU Unit and operation will continue. With a Duplex CPU System in Simplex Mode, CPU Unit operation will stop. This flag will be turned OFF when the FALS errors are cleared.	ON: FALS(006) executed OFF: FALS(006) not executed	Cleared	Cleared	When error occurs	A400
	A40108	Cycle Time Overrun Flag (Error causing switch to simplex operation)	ON if the cycle time exceeds the maximum cycle time set in the PLC Setup (the cycle time monitoring time). The ERR/ALM indicator will light. With a Single CPU System, CPU Unit operation will stop. With a Duplex CPU System in Duplex Mode, operation will switch to the standby CPU Unit and operation will continue. With a Duplex CPU System in Simplex Mode, CPU Unit operation will stop. This flag will be turned OFF when the error is cleared.	ON: Cycle time over max. OFF: Cycle time under max.	Cleared	Cleared	When cycle time exceeds max.	PLC Setup (Cycle time monitoring time)
	A40109	Program Error Flag (Error causing switch to simplex operation)	ON when program contents are incorrect. The ERR/ALM indicator will light. The task number where the error occurred will be stored in A294 and the program address will be stored in A298 and A299. The type of program error that occurred will be stored in bits 8 to 15 of A295. Refer to the description of A295 or to *2-3 Checking Programs* of *CS/CJ Series Programmable Controllers* (W394) for more details on program errors. With a Single CPU System, CPU Unit operation will stop. With a Duplex CPU System in Duplex Mode, operation will switch to the standby CPU Unit and operation will continue. With a Duplex CPU System in Simplex Mode, CPU Unit operation will stop. This flag will be turned OFF when the error is cleared.	ON: Error OFF: No error	Cleared	Cleared	---	A294, A295, A298 and A299
	A40110	I/O Setting Error Flag (Fatal error)	ON when an Input Unit has been installed in an Output Unit's slot or vice versa, so the Input and Output Units clash in the registered I/O table. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. This flag will be turned OFF when the error is cleared.	ON: Error OFF: No error	Cleared	Cleared	---	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A401	A40111	Too Many I/O Points Flag (Fatal error)	ON when the number of I/O points being used in Basic I/O Units exceeds the maximum allowed for the PLC. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. This flag will be turned OFF when the error is cleared.	ON: Error OFF: No error	Cleared	Cleared	---	A407
	A40112	Fatal Inner Board Error Flag (Error causing switch to simplex operation) (Single CPU Systems or Process-control CPU Unit)	ON when there is an Inner Board Error (Watchdog timer error). The ERR/ALM indicator will light. With a Single CPU System, CPU Unit operation will stop. With a Duplex CPU System in Duplex Mode, operation will switch to the standby CPU Unit and operation will continue. With a Duplex CPU System in Simplex Mode, CPU Unit operation will stop. This flag will be turned OFF when the error is cleared, but will be turned ON again unless the cause of the error is eliminated.	ON: Error OFF: No error	Cleared	Cleared	---	A242
	A40113	Duplication Error Flag (Fatal error)	ON in the following cases: Two CPU Bus Units have been assigned the same unit number. Two Special I/O Units have been assigned the same unit number. Two Basic I/O Units have been allocated the same data area words. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The duplicated unit number is indicated in A409 to A416. (This flag will be turned OFF when the error is cleared.)	ON: Duplication error OFF: No duplication	Cleared	Cleared	---	A410 to A416
	A40114	I/O Bus Error Flag (Fatal error)	ON when an error occurs in a data transfer between the CPU Unit and a Unit mounted to a slot. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The location of occurrence of the I/O bus error is reflected in A404. (This flag will be turned OFF when the error is cleared.)	ON: Error OFF: No error	Cleared	Cleared	---	A404
	A40115	Memory Error Flag (Fatal error)	ON when an error occurred in memory or there was an error in automatic transfer from the Memory Card when the power was turned ON. The ERR/ALM indicator on the front of the CPU Unit will light. With a Single CPU System, CPU Unit operation will stop. With a Duplex CPU System in Duplex Mode, operation will switch to the standby CPU Unit and operation will continue. With a Duplex CPU System in Simplex Mode, CPU Unit operation will stop. The cause of the memory error is reflected in A403. This flag will be turned OFF when the error is cleared. (The automatic transfer at start-up error cannot be cleared without turning off the PLC.)	ON: Error OFF: No error	Cleared	Cleared	---	A403

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A402	A40202	Special I/O Unit Setting Error Flag (Non-fatal error)	ON when an installed Special I/O Unit does not match the Special I/O Unit registered in the I/O table. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The unit number of the Unit where the setting error occurred is indicated in A428 to A433. (This flag will be turned OFF when the error is cleared.)	ON: Setting error detected OFF: No setting error	Cleared	Cleared	---	A428 to A433
	A40203	CPU Bus Unit Setting Error Flag (Non-fatal error)	ON when an installed CPU Bus Unit does not match the CPU Bus Unit registered in the I/O table. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The unit number of the Unit where the setting error occurred is written to A427. (This flag will be turned OFF when the error is cleared.)	ON: Setting error detected OFF: No setting error	Cleared	Cleared	---	A427
	A40204	Battery Error Flag (Non-fatal error)	ON if the CPU Unit's battery is disconnected or its voltage is low and the Detect Battery Error setting has been set in the PLC Setup. With a Duplex CPU System, this flag applies to both the left and right CPU Unit. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. This flag can be used to control an external warning light or other indicator to indicate that the battery needs to be replaced. (This flag will be turned OFF when the error is cleared.)	ON: Error OFF: No error	Cleared	Cleared	---	PLC Setup (Detect Battery Error) A324
	A40206	Special I/O Unit Error Flag (Non-fatal error)	ON when an error occurs in a data exchange between the CPU Unit and a Special I/O Unit (including an error in the Special I/O Unit itself). The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The Special I/O Unit where the error occurred will stop operating and the unit number of the Unit where the data exchange error occurred is indicated in A418 through A423. (This flag will be turned OFF when the error is cleared.)	ON: Error in one or more Units OFF: No errors in any Unit	Cleared	Cleared	---	A418 to A423
	A40207	CPU Bus Unit Error Flag (Non-fatal error)	ON when an error occurs in a data exchange between the CPU Unit and an CPU Bus Unit (including an error in the CPU Bus Unit itself). The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The CPU Bus Unit where the error occurred will stop operating and the unit number of the Unit where the data exchange error occurred is indicated in A417. (This flag will be turned OFF when the error is cleared.)	ON: Error in one or more Units OFF: No error in any Unit	Cleared	Cleared	---	A417

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A402	A40208	Inner Board Error Flag (Non-fatal error) (Single CPU Systems or Process-control CPU Units only)	ON when an error occurs in a data exchange between the CPU Unit and the Inner Board (including an error in the Inner Board itself). The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The Inner Board will stop operating and details on the error will be written to A424. (This flag will be turned OFF when the error is cleared.)	ON: Error OFF: No error	Cleared	Cleared	---	A424
	A40209	I/O Verification Error Flag (Non-fatal error)	ON when a Basic I/O Unit registered in the I/O Table does not match the Basic I/O Unit actually installed in the PLC because a Unit was added or removed. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (This flag will be turned OFF when the error is cleared.)	ON: Mismatch OFF: No mismatch	Cleared	Cleared	---	---
	A40210	PLC Setup Error Flag (Non-fatal error)	ON when there is a setting error in the PLC Setup. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The location of the error will be written to A406. (This flag will be turned OFF when the error is cleared.)	ON: Error OFF: No error	Cleared	Cleared	---	A406
	A40212	Basic I/O Unit Error Flag (Non-fatal error)	ON when an error has occurred in a Basic I/O Unit The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The location of the error will be written to A408. (This flag will be turned OFF when the error is cleared.)	ON: Error OFF: No error	Cleared	Cleared	---	A408
	A40213	Interrupt Task Error Flag (Non-fatal error) (Single CPU Systems)	ON when the Detect Interrupt Task Errors setting in the PLC Setup is set to “Detect” and an interrupt task is executed for more than 10 ms during I/O refreshing of a C200H Special I/O Unit or a SYSMAC BUS I/O Unit. This flag will also be turned ON if an attempt is made to refresh a Special I/O Unit’s I/O from an interrupt task with IORF(097) while the Unit’s I/O is being refreshed by cyclic I/O refreshing (duplicate refreshing). The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (This flag will be turned OFF when the error is cleared.)	1: Interrupt task error 0: No error	Cleared	Cleared	---	A426, PLC Setup (Detect Interrupt Task Errors setting)
	A40214	Non-fatal Duplex Error Flag	One of the following errors occurred: Duplex verification error (see note), duplex bus error (see note), duplex Power Supply Unit error, or duplex communications error **Note:** Duplex CPU Systems only.	ON: Duplex error OFF: No error	---	---	---	A31600, A31601, A31602, A31603

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	Bits							
A402	A40215	FAL Error Flag (Non-fatal error)	ON when a non-fatal error is generated by executing FAL(006). The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. The bit in A360 to A391 that corresponds to the FAL number specified in FALS(006) will be turned ON and the corresponding error code will be written to A400. Error codes 4101 to 42FF correspond to FAL numbers 001 to 2FF (0 to 511). (This flag will be turned OFF when the error is cleared.)	ON: FALS(006) error occurred OFF: FALS(006) not executed	Cleared	Cleared	When error occurs	A360 to A391, A400
A403	A40300 to A40308	Memory Error Location	When a memory error occurs, the Memory Error Flag (A40115) is turned ON and one of the following flags is turned ON to indicate the memory area where the error occurred. A40300: User program A40304: PLC Setup A40305: Registered I/O Table A40307: Routing Table A40308: CPU Bus Unit Settings When a memory error occurs, the CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (The corresponding flag will be turned OFF when the error is cleared.)	ON: Error OFF: No error	Cleared	Cleared	---	A40115
	A40309	Memory Card Start-up Transfer Error Flag	ON when automatic transfer at start-up has been selected and an error occurs during automatic transfer. An error will occur if there is a transfer error, the specified file does not exist, or the Memory Card is not installed. (This flag will be turned OFF when the error is cleared by turning the power off. The error cannot be cleared without turning the power off.)	ON: Error OFF: No error	Cleared	Cleared	When power is turned ON	---
	A40310	Flash Memory Error	Turns ON when the flash memory fails.	ON: Error OFF: No error	Clear	Clear	When error occurs	
	A40315	Duplex CPU Compatible Setting Change Error	1 (ON) when settings are changed without performing Memory All Clear on the CPU Unit during Duplex CPU compatible setting.	ON: Error OFF: No error	Held	Cleared	When power is turned ON	A327
A404	A40400 to A40407	I/O Bus Error Slot Number	Contains the 8-bit binary slot number (00 to 08) where an I/O Bus Error occurred. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The I/O Bus Error Flag (A40114) will be ON. (This flag will be turned OFF when the error is cleared.)	00 to 08 hex (slot No. 0 to 8)	Cleared	Cleared	---	A40114
	A40408 to A40415	I/O Bus Error Rack Number	Contains the 8-bit binary rack number (00 to 07) where an I/O Bus Error occurred. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The I/O Bus Error Flag (A40114) will be ON. (This flag will be turned OFF when the error is cleared.)	00 to 03 hex (Rack No. 0 to 3)	Cleared	Cleared	---	A40114

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	Bits							
A405	A40515	Peripheral Servicing Too Long Flag (Single CPU Systems onl7)	Turns ON when the peripheral servicing time in a Parallel Processing Mode exceeds 2 s. This will also cause a cycle time error and operation will stop.	1: Too long (Parallel processing cannot be used.) 0: Not too long (Parallel processing can be used.)	Cleared	Cleared	Written when error occurs	A268
A406	All	PLC Setup Error Location	When there is a setting error in the PLC Setup, the location of that error is written to A406 in 4-digit hexadecimal. The location is given as the address displayed on a Programming Console. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (A406 will be cleared when the cause of the error is eliminated.)	0000 to 01FF hex	Cleared	Cleared	When error occurs	A40210
A407	A40700 to A40712	Too Many I/O Points, Details	When there are too many I/O, CPU Unit operation will stop, the ERR/ALM indicator on the front of the CPU Unit will light, and one of the following values will be stored here. The total number of I/O points will be written here if the capacity of the CPU Unit is exceeded. The number of Racks will be written here when the number of Expansion I/O Racks exceeds the maximum. Number of interrupt input points when there are more than 32 (Single CPU Systems only) (These bits will be cleared when the error is cleared.)	0000 to 1FFF hex	Cleared	Cleared	When error occurs	A40111, A40713 to A40715
	A40713 to A40715	Too Many I/O Points, Cause	The 3-digit binary value of these bits indicates the cause of the Too Many I/O Points Error and shows the meaning of the value written to bits A40700 to A40712. (These bits will be cleared when the error is cleared.)	000: Too many I/O total 001: Too many interrupt input points 101: Too many Racks	Cleared	Cleared	When error occurs	---
A408	A40800 to A40807	Basic I/O Unit Error, Slot Number	When an error has occurred in a Basic I/O Unit, A40212 will be turned ON and the slot number where the error occurred will be written here in binary. (These bits will be cleared when the error is cleared.)	00 to 09 hex (Slots 0 to 9)	Cleared	Cleared	---	A40212
	A40808 to A40815	Basic I/O Unit Error, Rack Number	When an error has occurred in a Basic I/O Unit, A40212 will be turned ON and the Rack number where the error occurred will be written here in binary. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (These bits will be cleared when the error is cleared.)	00 to 07 hex (Racks 0 to 7)	Cleared	Cleared	---	A40212
A409	A40900 to A40907	Expansion I/O Rack Number Duplication Flags	The corresponding flag will be turned ON when an Expansion I/O Rack's starting word address was set from a Programming Device and two Racks have overlapping word allocations or a Rack's starting address exceeds CIO 0901. Bits 00 to 07 correspond to Racks 0 to 7. (The corresponding flag will be cleared when the error is cleared.)	ON: Error OFF: No error	Cleared	Cleared	---	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	Bits							
A410	A41000 to A41015	CPU Bus Unit Number Duplication Flags	The Duplication Error Flag (A40113) and the corresponding flag in A410 will be turned ON when an CPU Bus Unit's unit number has been duplicated. Bits 00 to 15 correspond to unit numbers 0 to F. CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light.	ON: Duplication detected OFF: No duplication	Cleared	Cleared	---	A40113
A411 to A416	A41100 to A41615	Special I/O Unit Number Duplication Flags	The Duplication Error Flag (A40113) and the corresponding flag in A411 through A416 will be turned ON when a Special I/O Unit's unit number has been duplicated. Bits 00 to 15 correspond to unit numbers 0 to F. (Bits A41100 to A41615 correspond to unit numbers 000 to 05F (0 to 95).) CPU Unit operation will stop and the ERR/ALM indicator on the front of the CPU Unit will light. The corresponding bit will also be turned ON when the Special I/O Unit's words are also allocated to a Basic I/O Unit on an Expansion I/O Rack because of the Expansion I/O Rack's starting word setting.	ON: Duplication detected OFF: No duplication	Cleared	Cleared	---	A40113
A417	A41700 to A41715	CPU Bus Unit Error, Unit Number Flags	When an error occurs in a data exchange between the CPU Unit and an CPU Bus Unit, the CPU Bus Unit Error Flag (A40207) is turned ON and the bit in A417 corresponding to the unit number of the Unit where the error occurred is turned ON. If the PLC Setup is set to turn ON the corresponding Error Unit Number Flag when a Special Unit (Special I/O Unit or CPU Bus Unit) is being replaced, the corresponding flag will be turned ON when the Unit is being replaced. If a duplexed CLK Unit is being replaced, the corresponding flag will be turned ON during replacement. Bits 00 to 15 correspond to unit numbers 0 to F. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash.	ON: Error or replacement OFF: No error	Cleared	Cleared	---	A40207
A418 to A423	A41800 to A42315	Special I/O Unit Error, Unit Number Flags	When an error occurs in a data exchange between the CPU Unit and a Special I/O Unit, the Special I/O Unit Error Flag (A40206) will be turned ON. Each bit corresponds to a unit number. Bit 00 in A418 to bit 15 in A423 correspond to unit numbers 0 to 95. If the PLC Setup is set to turn ON the corresponding Error Unit Number Flag when a Special Unit (Special I/O Unit or CPU Bus Unit) is being replaced, the corresponding flag will be turned ON when the Unit is being replaced. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. (Bits A41800 to A42315 correspond to unit numbers 000 to 05F (0 to 95).) If the unit number of the Unit is uncertain, none of the flags will be turned ON. (The flag will be turned OFF when the error is cleared.)	ON: Error or replacement OFF: No error	Cleared	Cleared	---	A40206

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	Bits							
A424	A42400 to A42415	Inner Board Error Information (Single CPU Systems or Process-control CPU Units only)	When an error occurs in a data exchange between the CPU Unit and the Inner Board, the Inner Board Error Flag (A40208) and the appropriate bits in A424 will be turned ON. The meaning of the bits in A424 depends upon the model of Inner Board that is being used. Refer to the Board's operation manual for details. A424 will be cleared when the error is cleared.	---	Cleared	Cleared	---	---
A426	A42600 to A42611	Interrupt Task Error, Task Number (Single CPU Systems only)	When A40213 is ON, the content of these bits depends upon the status of A42615 (the Interrupt Task Error Cause Flag). A42615 ON: An attempt was made to refresh a Special I/O Unit's I/O from an interrupt task with IORF(097) while the Unit's I/O is being refreshed by cyclic I/O refreshing (duplicate refreshing). A42600 to A42611: contain the Special I/O Unit's unit number. These bits will be cleared when the error is cleared.	Unit number: 000 to 05F (0 to 95)	Cleared	Cleared	---	A40213 A42615
	A42615	Interrupt Task Error Cause Flag (Single CPU Systems only)	When A40213 (the Interrupt Task Error Flag) is ON, this flag indicates the cause of the error. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash. A42615 will be ON if a Special I/O Unit was refreshed from the interrupt task while it was already being refreshed.	1: Duplicated refreshing 0: Interrupt task executed over 10 ms	Cleared	Cleared	---	A40213, A42600 to A42611
A427	A42700 to A42715	CPU Bus Unit Setting Error, Unit Number Flags	When an CPU Bus Unit Setting Error occurs, A40203 and the bit in this word corresponding to the Unit's unit number are turned ON. Bits 00 to 15 correspond to unit numbers 0 to F. The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash.	ON: Setting error OFF: No setting error	Cleared	Cleared	When power is turned ON or I/O is recognized	A40203
A428 to A433	A42800 to A43315	Special I/O Unit Setting Error, Unit Number Flags	When a Special I/O Unit Setting Error occurs, A40202 and the bit in these words corresponding to the Unit's unit number are turned ON. Bits 00 to 15 correspond to unit numbers 0 to F. (Bits A42800 to A43315 correspond to unit numbers 00 to 5F (0 to 95).) The CPU Unit will continue operating and the ERR/ALM indicator on the front of the CPU Unit will flash.	ON: Setting error OFF: No setting error	Cleared	Cleared	When power is turned ON or I/O is recognized	A40202
A434	A43400 to A43415	Duplex Communications Recognition Error Flags	ON: Duplex Communications Units for the corresponding unit number does not exist, i.e., it is not mounted, the Unit does not support duplex operation, or the unit number is illegal. Bits 00 to 15 correspond to unit numbers 0 to F.	ON: Duplex Unit not recognized OFF: Normal	Held	Cleared	When PLC Setup settings are made for duplex operation	A40214 A31603 A26111
A435	A43500 to A43515	Duplex Communications Setting Error Flags	ON: The settings of the pair of Units mounted for duplex communications are not the same. Refer to the Operation Manual for the Communications Unit for details on settings. Bits 00 to 15 correspond to unit numbers 0 to F.	ON: Duplex communications setting error OFF: Normal	Held	Cleared	When error occurs in duplex operation	A40214 A31603 A26112

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	**Bits**							
A436	A43600 to A43615	Duplex Communications Switched Flags (non-fatal communications error)	Active/Standby Communications Units ON: An error was detected in self-diagnosis in the active Communications Unit and operation was switched to the standby Communications Unit. Communications will be continued by the standby Communications Unit. Primary/Secondary Communications Units (See Note) ON: An error was detected in self-diagnosis in the primary Communications Unit and operation was switched to the secondary Communications Unit. Communications will be continued by the secondary Communications Unit. All Communications Units Bits 00 to 15 correspond to unit numbers 0 to F. This flag is turned OFF when online Unit replacement is performed for the faulty Communications Unit. **Note:** Primary/Secondary Communications Units are supported by CPU Unit Ver. 1.1 or later.	ON: Duplex Communications Units switched OFF: Normal	Held	Cleared	When communications are switched to simplex operation	A40214 A31603 A042 to A049
A437	A43700 to A43715	Duplex Communications Standby Unit Error Flags (non-fatal communications error)	Active/Standby Communications Units ON: An error was detected in self-diagnosis in the standby Communications Unit. Communications will be continued by the active Communications Unit. Primary/Secondary Communications Units (See Note) ON: An error was detected in self-diagnosis in the secondary Communications Unit. Communications will be continued by the primary Communications Unit. All Communications Units Bits 00 to 15 correspond to unit numbers 0 to F. This flag is turned OFF when online Unit replacement is performed for the faulty Communications Unit. **Note:** Primary/Secondary Communications Units are supported by CPU Unit Ver. 1.1 or later.	ON: Error OFF: Normal	Held	Cleared	When error occurs in Communications Unit	A40214 A31603
A439	A43915	Duplex Initialization Flag (Duplex CPU Systems only)	ON: Duplex operation being initialized.		Cleared	Cleared	---	A32808
A440	All	Max. Interrupt Task Processing Time (Single CPU Systems only)	Contains the Maximum Interrupt Task Processing Time in units of 0.1 ms. (This value is written after the interrupt task with the max. processing time is executed and cleared when PLC operation begins.)	0000 to FFFF hexadecimal	Cleared	Cleared	See Function column.	---

Address		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related flags, settings
Words	Bits							
A441	All	Interrupt Task With Max. Processing Time (Single CPU Systems only)	Contains the task number of the interrupt task with the maximum processing time. Hexadecimal values 8000 to 80FF correspond to task numbers 00 to FF. Bit 15 is turned ON when an interrupt has occurred. (This value is written after the interrupt task with the max. processing time is executed and cleared when PLC operation begins.)	8000 to 80FF hexadecimal	Cleared	Cleared	See Function column.	---

Read/Write Area

The following words and bits can be written by the user to control various aspect of PLC operation.

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A500	A50012	IOM Hold Bit	Turn this bit ON to preserve the status of the I/O Memory when shifting from PROGRAM to RUN or MONITOR mode or vice versa. (If the status of the IOM Hold Bit itself is preserved in the PLC Setup (IOM Hold Bit Status), the status of the I/O Memory Area will be retained when the PLC is turned ON or power is interrupted.)	ON: Held OFF: Not retained	Held	See Function column.	Read when power is turned ON	PLC Setup (IOM Hold Bit Status setting)
	A50013	Forced Status Hold Bit	Turn this bit ON to preserve the status of bits that have been force-set or force-reset when shifting between PROGRAM and MONITOR or when the power supply is turned ON. Always use this bit in combination with the IOM Hold Bit, i.e., A50012 must be turned ON before A50013 is effective. (If the status of the Forced Status Hold Bit itself is preserved in the PLC Setup (Forced Status Hold Bit Status), the status of force-set and force-reset bits will be retained when the PLC is turned ON or power is interrupted.)	ON: Held OFF: Not retained	Held	See Function column.	Read when power is turned ON	PLC Setup (Forced Status Hold Bit Status setting)
	A50014	Error Log Reset Bit	Turn this bit ON to reset the Error Log Pointer (A300) to 00. The contents of the Error Log Area itself (A100 to A199) are not cleared. (This bit is automatically reset to 0 after the Error Log Pointer is reset.)	OFF to ON: Clear	Held	Cleared	---	A100 to A199, A300
	A50015	Output OFF Bit	Turn this bit ON to turn OFF all outputs from Basic I/O Units and Special I/O Units. The INH indicator on the front of the CPU Unit will light while this bit is ON. (The status of the Output OFF Bit is retained through power interruptions.)	---	Held	Held	---	---
A501	A50100 to A50115	CPU Bus Unit Restart Bits	Turn these bits ON to restart (initialize) the CPU Bus Unit with the corresponding unit number. Bits 00 to 15 correspond to unit numbers 0 to F. When a restart bit is turned ON, the corresponding CPU Bus Unit Initializing Flag (A30200 to A30215) will be turned ON. Both the restart bit and initializing flag will be turned OFF automatically when initialization is completed. Do not turn the bit OFF from a Programming Device or the ladder program.	OFF to ON: Restart ON to OFF: Restart completed Turned OFF by the system when the Unit has been restarted.	Held	Cleared	---	A30200 to A30215

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A502 to A507	A50200 to A50715	Special I/O Unit Restart Bits	Turn these bits ON to restart (initialize) the Special I/O Unit with the corresponding unit number. Bits A50200 to A50715 correspond to unit numbers 0 to 95. When a restart bit is turned ON, the corresponding Special I/O Unit Initializing Flag (A33000 to A33515) will be turned ON. Both the restart bit and initializing flag will be turned OFF automatically when initialization is completed. Do not turn the bit OFF from a Programming Device or the ladder program.	OFF to ON: Restart ON to OFF: Restart completed Turned OFF by the system when the Unit has been restarted.	Held	Cleared	---	A33000 to A33515
A508	A50809	Differentiate Monitor Completed Flag	ON when the differentiate monitor condition has been established during execution of differentiation monitoring. (This flag will be cleared to 0 when differentiation monitoring starts.)	ON: Monitor condition established OFF: Not yet established	Held	Cleared	---	---
	A50811	TraceTrigger Monitor Flag	ON when a trigger condition is established by the Trace Start Bit (A50814). OFF when the next Data Trace is started by the Sampling Start bit (A50815).	ON: Trigger condition established OFF: Not yet established or not tracing	Held	Cleared	---	---
	A50812	Trace Completed Flag	ON when sampling of a region of trace memory has been completed during execution of a Trace. OFF when the next time the Sampling Start Bit (A50815) is turned from OFF to ON.	ON: Trace completed OFF: Not tracing or trace in progress	Held	Cleared	------	---
	A50813	Trace Busy Flag	ON when the Sampling Start Bit (A50815) is turned from OFF to ON. OFF when the trace is completed.	ON: Trace in progress OFF: Not tracing (not sampling)	Held	Cleared	---	---
	A50814	Trace Start Bit	Turn this bit from OFF to ON to establish the trigger condition. The offset indicated by the delay value (positive or negative) determines which data samples are valid.	ON: Trace trigger condition established OFF: Not established	Held	Cleared	---	---
	A50815	Sampling Start Bit	When a data trace is started by turning this bit from OFF to ON from a Programming Device, the PLC will begin storing data in Trace Memory by one of the three following methods: 1) Data is sampled at regular intervals (10 to 2,550 ms). 2) Data is sampled when TRSM(045) is executed in the program. 3) Data is sampled at the end of every cycle. The operation of A50815 can be controlled only from a Programming Device.	OFF to ON: Starts data trace (sampling) Turned ON from Programming Device.	Held	Cleared	---	---
A510 to A511	A51000 to A51115	Start-up Time	These words contain the time at which the power was turned ON. The contents are updated every time that the power is turned ON. The data is stored in BCD. A51000 to A51007: Second (00 to 59) A51008 to A51015: Minute (00 to 59) A51100 to A51107: Hour (00 to 23) A51108 to A51115: Day of month (01 to 31)	See Function column.	Held	See Function column.	When power is turned ON	---

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A512 to A513	A51200 to A51315	Power Interruption Time	These words contain the time at which the power was interrupted. The contents are updated every time that the power is interrupted. The data is stored in BCD. A51200 to A51207: Second (00 to 59) A51208 to A51215: Minute (00 to 59) A51300 to A51307: Hour (00 to 23) A51308 to A51315: Day of month (01 to 31) (These words are not cleared at start-up.)	See Function column.	Held	Held	Written at power interruption	---
A514	A51400 to A51415	Number of Power Interruptions	Contains the number of times that power has been interrupted since the power was first turned ON. The data is stored in binary. To reset this value, overwrite the current value with 0000. (This word is not cleared at start-up, but it is cleared when the Memory Corruption Detected Flag (A39511) goes ON.)	0000 to FFFF hex	Held	Held	When power is turned ON	A39511
A515 to A517		Operation Start Time	The time that operation started as a result of changing the operating mode to RUN or MONITOR mode is stored here in BCD. A51500 to A51507: Seconds (00 to 59) A51508 to A51515: Minutes (00 to 59) A51600 to A51607: Hour (00 to 23) A51608 to A51615: Day of month (01 to 31) A51700 to A51707: Month (01 to 12) A51708 to A51715: Year (00 to 99) **Note:** The previous start time is stored after turning ON the power supply until operation is started.	See at left.	Retained	Retained	See at left.	---
A518 to A520		Operation End Time	The time that operation stopped as a result of changing the operating mode to PROGRAM mode is stored here in BCD. A51800 to A51807: Seconds (00 to 59) A51808 to A51815: Minutes (00 to 59) A51900 to A51907: Hour (00 to 23) A51908 to A51915: Day of month (01 to 31) A52000 to A52007: Month (01 to 12) A52008 to A52015: Year (00 to 99) **Note:** If an error occurs in operation, the time of the error will be stored. If the operating mode is then changed to PROGRAM mode, the time that PROGRAM mode was entered will be stored.	See at left.	Retained	Retained	See at left.	---
A523	A52300 to A52315	Total Power ON Time	Contains the total time that the PLC has been on in 10-hour units. The data is stored in binary and it is updated every 10 hours. To reset this value, overwrite the current value with 0000. Once the value reaches FFFF, it will not be updated further and will remain at FFFF until reset. (This word is not cleared at start-up, but it is cleared to 0000 when the Memory Corruption Detected Flag (A39511) goes ON.)	0000 to FFFF hex	Held	Held	---	---

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A526	A52600	RS-232C Port Restart Bit	Turn this bit ON to restart the RS-232C port. (Do not use this bit when the port is operating in peripheral bus mode.) This bit is turned OFF automatically when the restart processing is completed.	OFF to ON: Restart	Held	Cleared	---	---
	A52601	Peripheral Port Restart Bit	Turn this bit ON to restart the peripheral port. This bit is turned OFF automatically when the restart processing is completed.	OFF to ON: Restart	Held	Cleared	---	---
A527	A52700 to A52707	Online Editing Disable Bit Validator	The Online Editing Disable Bit (A52709) is valid only when this byte contains 5A. To disable online editing from a Programming Device, set this byte to 5A and turn ON A52709. (Online editing refers to changing or adding to the program while the PLC is operating in MONITOR mode.)	5A: A52709 enabled Other value: A52709 disabled	Held	Cleared	---	A52709
	A52709	Online Editing Disable Bit	Turn this bit ON to disable online editing. The setting of this bit is valid only when A52700 to A52707 have been set to 5A.	ON: Disabled OFF: Not disabled	Held	Cleared	---	A52700 to A52707
A528	A52800 to A52807	RS-232C Port Error Flags	These flags indicate what kind of error has occurred at the RS-232C port; they are automatically turned OFF when the RS-232C port is restarted. (These flags are not valid in peripheral bus mode and only bit 5 is valid in NT Link mode.) Bits 0 and 1: Not used. Bit 2: ON when there was a parity error. Bit 3: ON when there was a framing error. Bit 4: ON when there was an overrun error. Bit 5: ON when there was a timeout error. Bits 6 and 7: Not used.	See Function column.	Held	Cleared	---	---
	A52808 to A52815	Peripheral Port Error Code	These flags indicate what kind of error has occurred at the peripheral port; they are automatically turned OFF when the peripheral port is restarted. Bits 8 and 9: Not used. Bit 10: ON when there was a parity error. Bit 11: ON when there was a framing error. Bit 12: ON when there was an overrun error. Bit 13: ON when there was a timeout error. Bits 14 and 15: Not used.	See Function column.	Held	Cleared	---	---
A529	A52900 to A52915	FAL/FALS Number for System Error Simulation	Set a dummy FAL/FALS number to use to simulate the system error using FAL(006) or FALS(007). When FAL(006) or FALS(007) is executed and the number in A529 is the same as the one specified in the operand of the instruction, the system error given in the operand of the instruction will be generated instead of a user-defined error.	0001 to 01FF hex: FAL/FALS numbers 1 to 511 0000 or 0200 to FFFF hex: No FAL/FALS number for system error simulation. (No error will be generated.)	Held	Cleared	---	---

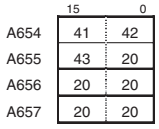
Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A530	A53000 to A53015	Power Interruption Disable Setting	Set to A5A5 hex to disable power interrupts between DI(693) and EI(694) instructions. Supported for Single CPU Systems only when the power OFF interrupt task is disabled.	A5A5 hex: Masking power interruption processing enabled Other: Masking power interruption processing not enabled.	Cleared	Cleared	---	---
A580 (See note.)	A58000 to A58003	FB Communications Instruction Retries (Unit version 4.0 or later)	Automatically stores the number of retries in the FB communications instruction settings specified in the PLC Setup.	0 to F hex	As set in PLC Setup	Cleared	Written at start of operation	
A581 (See note.)		FB Communications Instruction Response Monitoring Time (Unit version 4.0 or later)	Automatically stores the FB communications instruction response monitoring time set in the PLC Setup.	0001 to FFFF hex (Unit: 0.1 s; Range: 0.1 to 6553.5) 0000 hex: 2 s	As set in PLC Setup	Cleared		
A582 (See note.)		FB DeviceNet Communications Instruction Response Monitoring Time (Unit version 4.0 or later)	Automatically stores the FB DeviceNet communications instruction response monitoring time set in the PLC Setup.	0001 to FFFF hex (Unit: 0.1 s; Range: 0.1 to 6553.5) 0000 hex: 2 s	As set in PLC Setup	Cleared		
A595 and A596	---	IR00 Output for Background Execution (Single CPU Systems only)	When an index register is specified as the output for an instruction processed in the background, A595 and A596 receive the output instead of IR00.	0000 0000 to FFFF FFFF hex (A596 contains the leftmost digits.)	Cleared	Cleared	---	---
A597	---	DR00 Output for Background Execution (Single CPU Systems only)	When a data register is specified as the output for an instruction processed in the background, A597 receives the output instead of DR00.	0000 to FFFF hex	Cleared	Cleared	---	---

Note: These Auxiliary Area bits/words are not to be written by the user. The number of resends and response monitoring time must be set by the user in the FB communications instructions settings in the PLC Setup, particularly when using function blocks from the OMRON FB Library to execute FINS messages or DeviceNet explicit messages communications. The values set in the Settings for OMRON FB Library in the PLC Setup will be automatically stored in the related Auxiliary Area words A580 to A582 and used by the function blocks from the OMRON FB Library.

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A598	A59800	FPD Teaching Bit	Turn this bit ON to set the monitoring time automatically with the teaching function. While A59800 is ON, FPD(269) measures how long it takes for the diagnostic output to go ON after the execution condition goes ON. If the measured time exceeds the monitoring time, the measured time is multiplied by 1.5 and that value is stored as the new monitoring time. (The teaching function can be used only when a word address has been specified for the monitoring time operand.)	ON: Teach monitoring time OFF: Teaching function off	Cleared	Cleared	---	---
	A59801	Equals Flag for Background Execution (Single CPU Systems only)	Turns ON if matching data is found for an SRCH(181) instruction executed in the background.	1: Search data found in table 0: Search data not found	Cleared	Cleared	---	---
A600 to A603	A60000 to A60315	Macro Area Input Words	When MCRO(099) is executed, it copies the input data from the specified source words (input parameter words) to A600 through A603 and executes the specified subroutine with that input data.	Input data: 4 words	Cleared	Cleared	---	---
A604 to A607	A60400 to A60715	Macro Area Output Words	After the subroutine specified in MCRO(099) has been executed, the results of the subroutine are transferred from A604 through A607 to the specified destination words. (output parameter words).	Output data: 4 words	Cleared	Cleared	---	---
A608	A60800	Inner Board Restart Bit (Single CPU Systems or Process-control CPU Units only)	Turn the corresponding bit ON to restart (initialize) Inner Board 0 or 1. The bit is turned OFF automatically when the restart processing is completed.	---	Held	Cleared	---	---
A609 to A613	A60900 to A61315	Inner Board User Interface Area (Single CPU Systems or Process-control CPU Units only)	The data transferred from the CPU Unit to the Inner Board is defined and used at the Inner Board. The contents of these words is retained when the power is turned ON.	---	Held	Held	---	---
A619	A61901	Peripheral Port Settings Changing Flag	ON while the peripheral port's communications settings are being changed. This flag will be turned ON when STUP(237) is executed and it will be turned OFF after the settings have been changed.	ON: Changing OFF: Not changing	Held	Cleared	---	---
	A61902	RS-232C Port Settings Changing Flag	ON while the RS-232C port's communications settings are being changed. This flag will be turned ON when STUP(237) is executed and it will be turned OFF after the settings have been changed.	ON: Changing OFF: Not changing	Held	Cleared	---	---

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A620	A62001	Communications Unit 0, Port 1 Settings Changing Flag	The corresponding flag will be ON when the settings for that port are being changed. The flag will be turned ON when STUP(237) is executed and it will be turned OFF by an event issued from the Serial Communications Unit after the settings have been changed. It is also possible for the user to indicate a change in serial port settings by turning these flags ON.	ON: Changing OFF: Not changing	Held	Cleared	---	---
	A62002	Communications Unit 0, Port 2 Settings Changing Flag		ON: Changing OFF: Not changing	Held	Cleared	---	---
	A62003	Communications Unit 0, Port 3 Settings Changing Flag		ON: Changing OFF: Not changing	Held	Cleared	---	---
	A62004	Communications Unit 0, Port 4 Settings Changing Flag		ON: Changing OFF: Not changing	Held	Cleared	---	---
A621 to A635	A62100 to A63504	Communications Units 0 to 15, Ports 1 to 4 Settings Changing Flag	Same as above.	ON: Changing OFF: Not changing	Held	Cleared	---	---
A636	A63601	Communications Board Port 1 Settings Changing Flag	The corresponding flag will be ON when the settings for that port are being changed. The flag will be turned ON when STUP(237) is executed and it will be turned OFF by an event issued from the Serial Communications Board after the settings have been changed. It is also possible for the user to indicate a change in serial port settings by turning these flags ON. (Single CPU Systems only)	1: Changing 0: Not changing	Retained	Cleared	---	---
	A63602	Communications Board Port 2 Settings Changing Flag		1: Changing 0: Not changing	Retained	Cleared	---	---
	A63603	Communications Board Port 3 Settings Changing Flag		1: Changing 0: Not changing	Retained	Cleared	---	---
	A63604	Communications Board Port 4 Settings Changing Flag		1: Changing 0: Not changing	Retained	Cleared	---	---

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A650	A65000 to A65007	Program Replacement End Code (Not supported by CS1□-CPU□□ (-V1) Units)	• Normal End (i.e., when A65014 is OFF) 01 hex: Program file (.OBJ) replaced. • Error End (i.e., when A65014 is ON) 00 hex: Fatal error 01 hex: Memory error 11 hex: Write-protected 12 hex: Program replacement password error 21 hex: No Memory Card 22 hex: No such file 23 hex: Specified file exceeds capacity (memory error). 31 hex: One of the following in progress: • File memory operation • User program write • Operating mode change	---	Retained	Cleared	---	---
	A65014	Replacement Error Flag hex	ON when the Replacement Start Bit (A65015) is turned ON to replace the program, but there is an error. If the Replacement Start Bit is turned ON again, the Replacement Error Flag will be turned OFF.	ON: Replacement error OFF: No replacement error, or the Replacement Start Bit (A65015) is ON.	Held	Cleared	---	---
	A65015	Replacement Start Bit hex	Program replacement starts when the Replacement Start Bit is turned ON if the Program Password (A651) is valid (A5A5 hex). Do not turn OFF the Replacement Start Bit during program replacement. When the power is turned ON or program replacement is completed, the Replacement Start Bit will be turned OFF, regardless of whether replacement was completed normally or in error. It is possible to confirm if program replacement is being executed by reading the Replacement Start Bit using a Programming Device, PT, or host computer.	ON: Program replaced OFF: Replacement completed, or after power is turned ON	Held	Cleared	---	---
A651	---	Program Password hex	Type in the password to replace a program. A5A5 hex: Replacement Start Bit (A65015) is enabled. Any other value: Replacement Start Bit (A65015) is disabled. When the power is turned ON or program replacement is completed, the Replacement Start Bit will be turned OFF, regardless of whether replacement was completed normally or in error.	---	Held	Cleared	---	---

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A654 to A657	---	Program File Name hex	When program replacement starts, the program file name will be stored in ASCII. File names can be specified up to eight characters in length excluding the extension. File names are stored in the following order: A654 to A657 (i.e., from the lowest word to the highest), and from the highest byte to the lowest. If a file name is less than eight characters, the lowest remaining bytes and the highest remaining word will be filled with spaces (20 hex). Null characters and space characters cannot be used within file names. Example: File name is ABC.OBJ  	---	Held	Cleared	---	---
A720 to A722		Power ON Clock Data 1 (CS1D-CPU□□SA and CS1D Duplex-CPU Systems with unit version 1.2 or later)	This is the history data at Startup Time. A72000 to A72007: Second (00 to 59) A72008 to A72015: Minute (00 to 59) A72100 to A72107: Hour (00 to 23) A72108 to A72115: Day of month (01 to 31) A72200 to A72207: Month (01 to 12) A72208 to A72215: Year (00 to 99)	See at left	Held	Held	When power is turned ON	
A723 to A725		Power ON Clock Data 2 (CS1D-CPU□□SA and CS1D Duplex-CPU Systems with unit version 1.2 or later)	This is the history data at Startup Time. A72300 to A72307: Second (00 to 59) A72308 to A72315: Minute (00 to 59) A72400 to A72407: Hour (00 to 23) A72408 to A72415: Day of month (01 to 31) A72500 to A72507: Month (01 to 12) A72508 to A72515: Year (00 to 99)	See at left	Held	Held	When power is turned ON	
A726 to A728		Power ON Clock Data 3 (CS1D-CPU□□SA and CS1D Duplex-CPU Systems with unit version 1.2 or later)	This is the history data at Startup Time. A72600 to A72607: Second (00 to 59) A72608 to A72615: Minute (00 to 59) A72700 to A72707: Hour (00 to 23) A72708 to A72715: Day of month (01 to 31) A72800 to A72707: Month (01 to 12) A72808 to A72815: Year (00 to 99)	See at left	Held	Held	When power is turned ON	
A729 to A731		Power ON Clock Data 4 (CS1D-CPU□□SA and CS1D Duplex-CPU Systems with unit version 1.2 or later)	This is the history data at Startup Time. A72900 to A72907: Second (00 to 59) A72908 to A72915: Minute (00 to 59) A73000 to A73007: Hour (00 to 23) A73008 to A73015: Day of month (01 to 31) A73100 to A73107: Month (01 to 12) A73108 to A73115: Year (00 to 99)	See at left	Held	Held	When power is turned ON	

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A732 to A734		Power ON Clock Data 5 (CS1D-CPU□□SA and CS1D Duplex-CPU Systems with unit version 1.2 or later)	This is the history data at Startup Time. A73200 to A73207: Second (00 to 59) A73208 to A73215: Minute (00 to 59) A73300 to A73307: Hour (00 to 23) A73308 to A73315: Day of month (01 to 31) A73400 to A73407: Month (01 to 12) A73408 to A73415: Year (00 to 99)	See at left	Held	Held	When power is turned ON	
A735 to A737		Power ON Clock Data 6 (CS1D-CPU□□SA) Power OFF Time History Data #1 (CS1D Duplex-CPU Systems with unit version 1.2 or later)	For the CPU□□SA, this is the history data at Startup Time. For the CS1D Duplex-CPU Systems, this is the history data at Power OFF Time. A73500 to A73507: Second (00 to 59) A73508 to A73515: Minute (00 to 59) A73600 to A73607: Hour (00 to 23) A73608 to A73615: Day of month (01 to 31) A73700 to A73707: Month (01 to 12) A73708 to A73715: Year (00 to 99)	See at left	Held	Held	When power is turned ON	
A738 to A740		Power ON Clock Data 7 (CS1D-CPU□□SA) Power OFF Time History Data #2 (CS1D Duplex-CPU Systems with unit version 1.2 or later)	For the CPU□□SA, this is the history data at Startup Time. For the CS1D Duplex-CPU Systems, this is the history data at Power OFF Time. A73800 to A73807: Second (00 to 59) A73808 to A73815: Minute (00 to 59) A73900 to A73907: Hour (00 to 23) A73908 to A73915: Day of month (01 to 31) A74000 to A74007: Month (01 to 12) A74008 to A74015: Year (00 to 99)	See at left	Held	Held	When power is turned ON	
A741 to A743		Power ON Clock Data 8 (CS1D-CPU□□SA) Power OFF Time History Data #3 (CS1D Duplex-CPU Systems with unit version 1.2 or later)	For the CPU□□SA, this is the history data at Startup Time. For the CS1D Duplex-CPU Systems, this is the history data at Power OFF Time. A74100 to A74107: Second (00 to 59) A74108 to A74115: Minute (00 to 59) A74200 to A74207: Hour (00 to 23) A74208 to A74215: Day of month (01 to 31) A74300 to A74307: Month (01 to 12) A74308 to A74315: Year (00 to 99)	See at left	Held	Held	When power is turned ON	
A744 to A746		Power ON Clock Data 9 (CS1D-CPU□□SA) Power OFF Time History Data #4 (CS1D Duplex-CPU Systems with unit version 1.2 or later)	For the CPU□□SA, this is the history data at Startup Time. For the CS1D Duplex-CPU Systems, this is the history data at Power OFF Time. A74400 to A74407: Second (00 to 59) A74408 to A74415: Minute (00 to 59) A74500 to A74507: Hour (00 to 23) A74508 to A74515: Day of month (01 to 31) A74600 to A74607: Month (01 to 12) A74608 to A74615: Year (00 to 99)	See at left	Held	Held	When power is turned ON	

Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A747 to A749		Power ON Clock Data 10 (CS1D-CPU□□SA) Power OFF Time History Data #5 (CS1D Duplex-CPU Systems with unit version 1.2 or later)	For the CPU□□SA, this is the history data at Startup Time. For the CS1D Duplex-CPU Systems, this is the history data at Power OFF Time. A74700 to A74707: Second (00 to 59) A74708 to A74715: Minute (00 to 59) A74800 to A74807: Hour (00 to 23) A74808 to A74815: Day of month (01 to 31) A74900 to A74907: Month (01 to 12) A74908 to A74915: Year (00 to 99)	See at left	Held	Held	When power is turned ON	
A800	A80015	Maintenance Start Bit	When the Unit Removal without a Programming Device function is enabled and this bit is ON, a non-fatal Basic I/O Unit error, Special I/O Unit error, or CPU Bus Unit error will not occur when a Unit is removed. This bit is turned OFF automatically by the system when all of the online replacements are completed (data exchange restarts). This bit can also be turned OFF manually by the user before all of the online replacements have been completed.	ON: An error will not occur when a Unit is removed. (Errors will not be detected in other Units, either.) OFF: An error will occur when a Unit is removed. (Errors will be detected in other Units, too.)	Held	Cleared	Each cycle	---
A801	A80115	Online Replacement Completion Error Flag	This flag is turned ON when online replacement failed or OFF when online replacement was successful. The flag indicates the completion status of the last online Unit replacement, so it will be turned OFF when a Unit is successfully replaced even if there is still a Unit in the PLC which was not replaced successfully.	OFF → ON: Online replacement failed.	Held	Cleared	Each cycle	A803
A802	A80215	Online Replacement Completed Bit	When the Unit Removal without a Programming Device function is enabled, data exchange between the CPU Unit and the mounted Unit is restarted when this bit is turned ON.	OFF → ON: Complete Unit replacement processing. (Restart data exchange after mounting Unit.)	Held	Cleared	---	A80300 to A80315
A803	---	Online Replacement Completion Error Details	When an online replacement function failed, the relevant flag will be turned ON.	OFF → ON: Online replacement failed.	Held	Cleared	---	A80115
	A80300		No Unit mounted or Unit mounted in another slot.					
	A80301		Different unit types, unit numbers, or serial numbers on replaced and new unit.					
	A80302		Different node numbers on replaced and new Units (when replacing a duplex Communications Unit).					

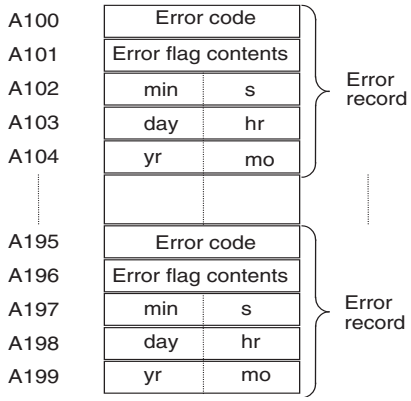
Addresses		Name	Function	Settings	Status after mode change	Status at startup	Timing	Related Flags, Settings
Word	Bit							
A804	---	Details on duplex verification error caused by different unit versions	The corresponding bit is turned ON when a duplex verification error occurred due to different unit versions.	ON: Mismatch OFF: Match	Held	Cleared	When duplex verification error occurs	A31600, A317
	A80400		Ethernet Duplex Setting Flag (PLC Setup)					
	A80401		Unit Removal without a Programming Device Function Setting Flag (PLC Setup)					
	A80402		Removal/Addition of Units without a Programming Device Setting Flag (PLC Setup)					
	A80403		Turn ON Error Unit Number Flag when Removing a Special Unit Setting Flag (PLC Setup)					
	A80404		Communications Port Auto-allocation Instruction (Instruction)					

Note In CS1D PLCs, the following flags are provided in a special read-only area and can be specified with the labels given in the table. These flags are not contained in the Auxiliary Area.

Flag area	Name	Label	Meaning
Condition Code Area	Error Flag	**ER**	Turns ON when an error occurs in processing an instructions, indicating an error end to the instruction.
	Access Error Flag	**AER**	Turns ON when an attempt is made to access an illegal area. The status of this flag is maintain only during the current cycle and only in the task in which it occurred.
	Carry Flag	**CY**	Turns ON when there is a carry or borrow in a math operation, when a bit is shifted into the Carry Flag, etc.
	Greater Than Flag	**>**	Turns ON when the result of comparing two values is “greater than,” when a value exceeds a specified range, etc.
	Equals Flag	**=**	Turns ON when the result of comparing two values is “equals,” when the result of a math operation is 0, etc.
	Less Than Flag	**<**	Turns ON when the result of comparing two values is “less than,” when a value is below a specified range, etc.
	Negative Flag	**N**	Turns ON when the MSB in the result of a math operation is 1.
	Overflow Flag	**OF**	Turns ON when the result of a math operation overflows.
	Underflow Flag	**UF**	Turns ON when the result of a math operation underflows.
	Greater Than or Equals Flag	**>=**	Turns ON when the result of comparing two values is “greater than or equals.”
	Not Equal Flag	**<>**	Turns ON when the result of comparing two values is “not equal.”
	Less than or Equals Flag	**<=**	Turns ON when the result of comparing two values is “less than or equals.”
	Always ON Flag	**A1**	This flag is always ON.
	Always OFF Flag	**A0**	This flag is always OFF.
Clock Pulse Area	0.02-s clock pulse	**0.02s**	Repeatedly turns ON for 0.02 s and OFF for 0.02 s.
	0.1-s clock pulse	**0.1s**	Repeatedly turns ON for 0.1 s and OFF for 0.1 s.
	0.2-s clock pulse	**0.2s**	Repeatedly turns ON for 0.2 s and OFF for 0.2 s.
	1-s clock pulse	**1s**	Repeatedly turns ON for 1 s and OFF for 1 s.
	1-min clock pulse	**1min**	Repeatedly turns ON for 1 min and OFF for 1 min.

Details on Auxiliary Area Operation

A100 to A199: Error Log Area



The following data would be generated in an error record if a memory error (error code 80F1) occurred on 1 April 2002 at 17:10:30 with the error located in the PLC Setup (0010 hex).

80 F1	
00 10	
10	30
01	17
02	04

The following data would be generated in an error record if an FALS error with FALS number 001 occurred on 2 May 2002 at 8:30:15.

C1 01	
00 00	
30	15
02	08
02	05

Error Codes and Error Flags

Classification	Error code	Meaning	Error flags
System-defined fatal errors	80F1	Memory error (See note 1.)	A403
	80F0	Program error (See note 1.)	A294 to 299 (See note 5.)
	809F	Cycle time overrun error (See note 1.)	---
	82F0	Fatal Inner Board error (See notes 1 and 9.)	A424
	80C0 to 80C7, 80CF	I/O bus error	A404
	80E9	Duplicate number error	A410, A411 to 416 (See note 4.)
	80E1	Too many I/O error	A407
	80E0	I/O setting error	---
	80EA	Duplicate Expansion Rack number error	A40900 to 40907
User-defined fatal errors	C101 to C2FF	FALS instruction executed (See notes 1 and 2.)	---
User-defined non-fatal errors	4101 to 42FF	FAL instruction executed (See note 3.)	---
System-defined non-fatal errors	009A	Basic I/O Unit error	A408
	009B	PLC Setup setting error	A406
	00E7	I/O verification error	---
	02F0	Non-fatal Inner Board error (See note 9.)	A424
	0200 to 020F	CPU Bus Unit error	A417
	0300 to 035F	Special I/O Unit error	A418 to 423 (See note 6.)
	00F7	Battery error	---
	0400 to 040F	CPU Bus Unit setup error	A427
	0500 to 055F	Special I/O Unit setup error	A428 to 433 (See note 6.)
	0011	Duplex verification error (See note 8.)	A31600, A317, A804
	0010	Duplex bus error (See note 8.)	A31601
	0003	Duplex power supply error	A31602, A319 (See note 10.)
	0600 to 060F	Duplex communications error (See note 7.)	A31603, A321, A434 to A437

Note 1. Operation will be switched to the standby CPU Unit in Duplex CPU Systems.

2. C101 to C2FF will be stored for FALS numbers 001 to 511.

3. 4101 to 42FF will be stored for FAL numbers 001 to 511.

4. The contents of the error flags for a duplicate number error are as follows: Bits 0 to 7: Unit number (binary), 00 to 5F hex for Special I/O Units, 00 to 0F hex for CPU Bus Units,
Bits 8 to 14: All zeros, Bit 15: Unit type, 0 for CPU Bus Units and 1 for Special I/O Units.

5. Only the contents of A295 is stored as the error flag contents for program errors.

6. 0000 hex will be stored as the error flag contents.

7. The rightmost digit of the error code (0 to F) for duplex communications error corresponds to CPU Bus Unit unit numbers 0 to F.

8. These error occur only for Duplex CPU Systems.

9. These error occur only for Single CPU Systems or Process-control CPU Units.

10. The contents of the error information relays of a Duplex power supply error are as described below. If a Duplex power supply error occurs at multiple locations, the location detected first is displayed.

    Bit 00: Right-side power supply secondary-side 5V error (1: Normal / 0: Error)

    Bit 01: Right-side power supply secondary-side 26V error (1: Normal / 0: Error)

    Bit 02: Right-side power supply primary-side power supply error (1: Normal / 0: Error)

    Bit 03: Left-side power supply secondary-side 5V error (1: Normal / 0: Error)

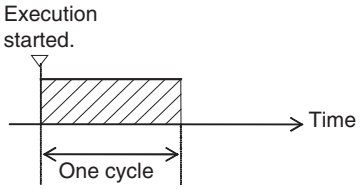
    Bit 04: Right-side power supply secondary-side 26V error (1: Normal / 0: Error)

    Bit 05: Left-side power supply primary-side power supply error (1: Normal / 0: Error)

Bit 06 to 07: Reserved

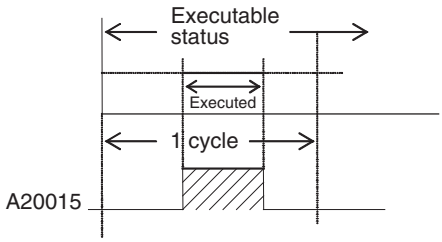
Bit 08 to 15: rack number (BIN data): 0 to 7

A20011: First Cycle Flag

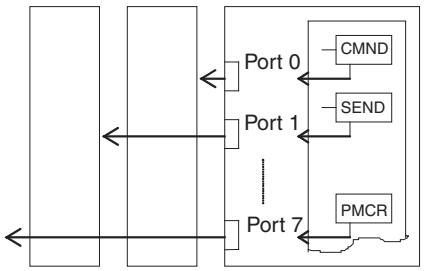


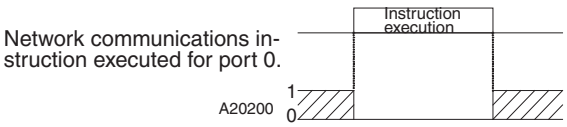
A20015: Initial Task Flag

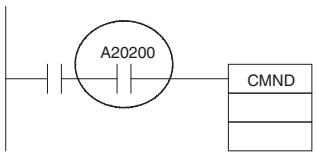
A20015 will turn ON during the first time a task is executed after it has reached executable status. It will be ON only while the task is being executed and will not turn ON if following cycles.



A20200 to A20207: Communications Port Enabled Flags

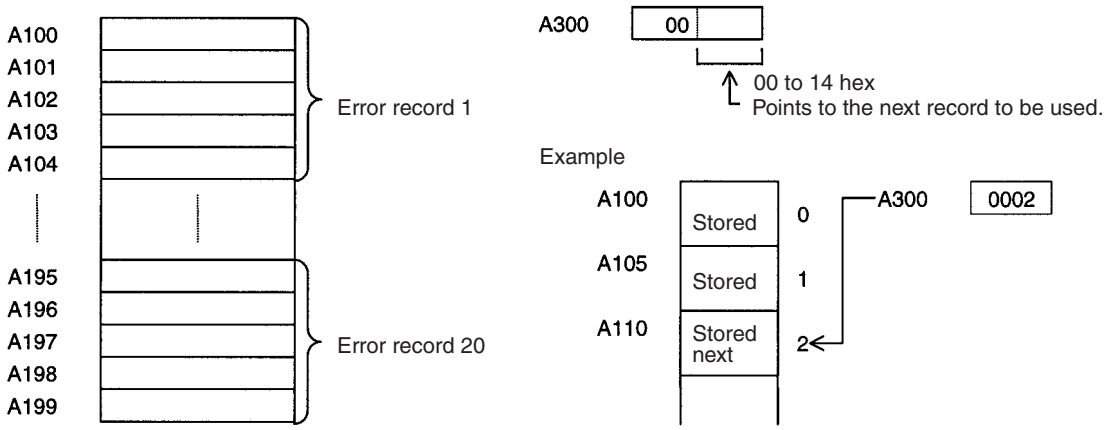




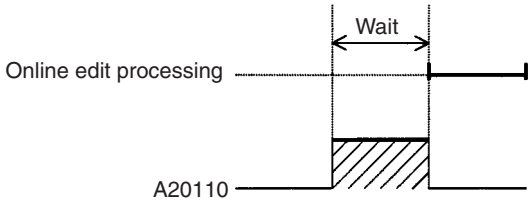


The program is designed so that CMND(490) will be executed only when A20200 is ON.

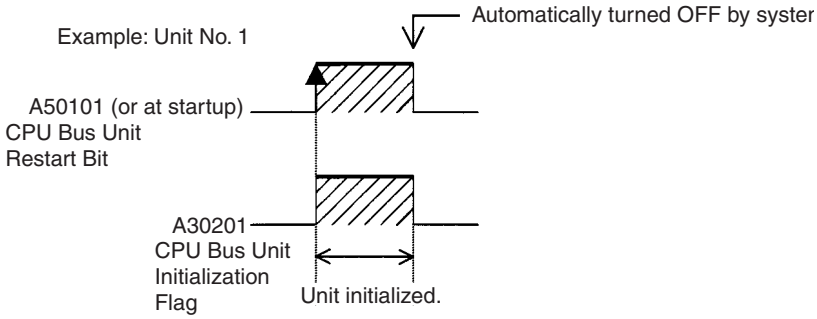
A300: Error Record Pointer



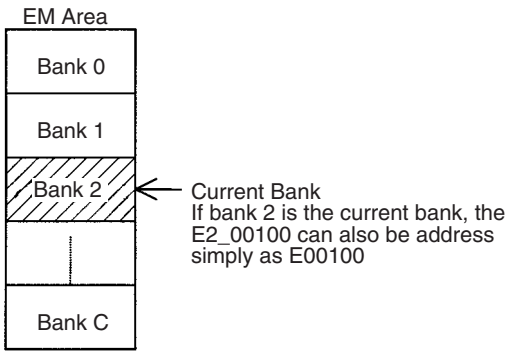
A20110: Online Editing Wait Flag



A50100 to A50115: CPU Bus Unit Restart Bits



A301: Current EM Bank



A40109: Program Error

Error	Address
UM Overflow Error Flag	A29515
Illegal Instruction Flag	A29514
Distribution Overflow Error Flag	A29513
Task Error Flag	A25912
No END(001) Error Flag	A29511
Illegal Area Access Error Flag	A29510
Indirect DM/EM Addressing Error Flag	A29509

Appendix C
Memory Map of PLC Memory Addresses

PLC Memory Addresses

PLC memory addresses are set in Index Registers (IR00 to IR15) to indirectly address I/O memory. Normally, use the MOVE TO REGISTER (MOVR(560)) and MOVE TIMER/COUNTER PV TO REGISTER (MOVRW(561)) instructions to set PLC memory addresses into the Index Registers.

Some instructions, such as DATA SEARCH (SRCH(181)), FIND MAXIMUM (MAX(182)), and FIND MINIMUM (MIN(183)), output the results of processing to an Index Register to indicate an PLC memory address.

There are also instructions for which Index Registers can be directly designated to use the PLC memory addresses stored in them by other instructions. These instructions include DOUBLE MOVE (MOVL(498)), some symbol comparison instructions (=L, <>L, <L, >L, <=L, and >=L), DOUBLE COMPARE (CMPL(060)), DOUBLE DATA EXCHANGE (XCGL(562)), DOUBLE INCREMENT BINARY (++L(591)), DOUBLE DECREMENT BINARY (– –L(593)), DOUBLE SIGNED BINARY ADD WITHOUT CARRY (+L(401)), DOUBLE SIGNED BINARY SUBTRACT WITHOUT CARRY (–L(411)), SET RECORD LOCATION (SETR(635)), and GET RECORD LOCATION (GETR(636)).

The PLC memory addresses all are continuous and the user must be aware of the order and boundaries of the memory areas. As reference, the PLC memory addresses are provided in a table at the end of this appendix.

Note Directly setting PLC memory addresses in the program should be avoided whenever possible. If PLC memory addresses are set in the program, the program will be less compatible with new CPU Unit models or CPU Units for which changed have been made to the layout of the memory.

Memory Configuration

There are two classifications of the RAM memory (with battery backup) in a CS-series CPU Unit.

Parameter Areas: These areas contain CPU Unit system setting data, such as the PLC Setup, CS-series CPU Bus Unit Setups, etc. An illegal access error will occur if an attempt is made to access any of the parameter areas from an instruction in the user program.

I/O Memory Areas: These are the areas that can be specified as operands in the instructions in user programs.

Memory Map

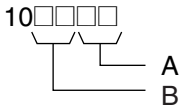
Do not access words that are reserved by the system.

Classification	PLC memory addresses (hex)	User addresses	Area
Parameter areas	00000 to 0B0FF	---	PLC Setup Area Registered I/O Table Area Routing Table Area CPU Bus Unit Setup Area Real I/O Table Area Unit Profile Area
I/O memory areas	0B100 to 0B1FF	---	Reserved for system.
	0B200 to 0B7FF	---	Reserved for system.
	0B800 to 0B801	TK00 to TK31	Task Flag Area
	0B802 to 0B83F	---	Reserved for system.
	0B840 to 0B9FF	A000 to A447	Read-only Auxiliary Area
	0BA00 to 0BBFF	A448 to A959	Read/Write Auxiliary Area
	0BC00 to 0BDFF	---	Reserved for system.
	0BE00 to 0BEFF	T0000 to T4095	Timer Completion Flags
	0BF00 to 0BFFF	C0000 to C4095	Counter Completion Flags
	0C000 to 0D7FF	CIO 0000 to CIO 6143	CIO Area
	0D800 to 0D9FF	H000 to H511	Holding Area
	0DA00 to 0DDFF	H512 to H1535	Holding Area This is a function block dedicated area.
	0DE00 to 0DFFF	W000 to W511	Work Area
	0E000 to 0EFFF	T0000 to T4095	Timer PVs
	0F000 to 0FFFF	C0000 to C4095	Counter PVs
	10000 to 17FFF	D00000 to D32767	DM Area
	18000 to 1FFFF	E0_00000 to E0_32767	EM Area bank 0
	20000 to 27FFF	E1_00000 to E1_32767	EM Area bank 1
	28000 to 2FFFF	E2_00000 to E2_32767	EM Area bank 2
	30000 to 37FFF	E3_00000 to E3_32767	EM Area bank 3
	38000 to 3FFFF	E4_00000 to E4_32767	EM Area bank 4
	40000 to 47FFF	E5_00000 to E5_32767	EM Area bank 5
	48000 to 4FFFF	E6_00000 to E6_32767	EM Area bank 6
	50000 to 57FFF	E7_00000 to E7_32767	EM Area bank 7
	58000 to 5FFFF	E8_00000 to E8_32767	EM Area bank 8
	60000 to 67FFF	E9_00000 to E9_32767	EM Area bank 9
	68000 to 6FFFF	EA_00000 to EA_32767	EM Area bank A
	70000 to 77FFF	EB_00000 to EB_32767	EM Area bank B
	78000 to 7FFFF	EC_00000 to EC_32767	EM Area bank C
	D8000 to DFFFF	E18_00000 to E18_32767	EM Area bank 18
	F8000 to FFFFF	E0000 to E32767	EM Area, current bank (See note.)

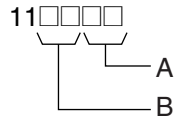
Note The contents of the EM Area bank currently specified in the program is stored at these addresses. For example, if bank 8 is specified, the same contents as at 58000 to 5FFFF will be stored at F8000 to FFFFF.

Appendix D
PLC Setup Coding Sheets for Programming Console

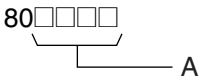
Use the following coding sheets when setting the PLC Setup from a Programming Console.



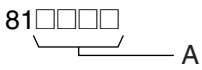
	Value (hex)	Rack 0, Slot 0 I/O Response Time
A	00	8 ms
	10	No filter
	11	0.5 ms
	12	1 ms
	13	2 ms
	14	4 ms
	15	8 ms
	16	16 ms
	17	32 ms
B	00	8 ms
	10	No filter
	11	0.5 ms
	12	1 ms
	13	2 ms
	14	4 ms
	15	8 ms
	16	16 ms
	17	32 ms



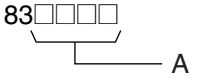
	Value (hex)	Rack 0, Slot 2 I/O Response Time
A	00	8 ms
	10	No filter
	11	0.5 ms
	12	1 ms
	13	2 ms
	14	4 ms
	15	8 ms
	16	16 ms
	17	32 ms
	Value (hex)	**Rack 0, Slot 3 I/O Response Time**
B	00	8 ms
	10	No filter
	11	0.5 ms
	12	1 ms
	13	2 ms
	14	4 ms
	15	8 ms
	16	16 ms
	17	32 ms



	Value (hex)	IOM Hold Bit Status at Startup	Forced Status Hold Bit Status at Startup
A	C000	Retained	Retained
	8000	Retained	Cleared
	4000	Cleared	Retained
	0000	Cleared	Cleared



	Value (hex)	Startup Mode
A	PRCN	Mode on Programming Console's mode switch
	PRG	PROGRAM mode
	MON	MONITOR mode
	RUN	RUN mode



	Value (hex)	Startup Condition
A	8000	Don't wait.
	0000	Wait for all Units and Boards.

84□□□□
A

	Value (hex)	Inner Board Setting
A	8000	Don't wait.
	0000	Wait for all Boards.

95□□□□
A

	Value (hex)	Primary/Secondary Duplex Communications Unit Settings	
A	0000	Not duplex for unit numbers 0 to 15.	Bits 00 to 14 correspond to unit numbers 0 to 14.
	0001	Unit number 0 set as primary Unit.	
	to		
	4000	Unit number 14 set as primary Unit.	

Note The unit number of the secondary Unit is one higher than that of the primary Unit.

96□□□□ (Duplex CPU Systems only)
A

	Value (hex)	Duplex Transfer Settings	
		Program transfer	EM Area transfer
A	0000	Transfer program	Transfer together
	8000	Don't transfer program	Transfer together
	40□□	Transfer program	Transfer over multiple scans
	C0□□	Don't transfer program	Transfer over multiple scans

Note The above settings assume that both bit 11 (Inner Board parameter area) and bit 10 (Inner Board variable area) are set to 0.

121□□□□
A

	Value (hex)	Duplex Communications Unit Settings	
A	0000	Not duplex for unit numbers 0 to 15.	Bits 00 to 15 correspond to unit numbers 0 to 15.
	0001	Duplex for only unit number 0.	
	to		
	8000	Duplex for only unit number 15.	

Note Up to three bits may be turned ON at the same time.

122□□□□
A

	Value (hex)	Multiple Unit Online Replacement
A	0000	Allow only one Unit to be replaced online at a time.
	8000	Allow simultaneous online replacement of more than one Unit.

123□□□□ (Duplex CPU Systems only)

A

	Value (hex)	Operation during Duplex Initialization	Automatic Recovery to Duplex Operation
A	0000	Don't run during initialization.	Don't recover automatically.
	4000	Run during initialization.	Don't recover automatically.
	8000	Don't run during initialization.	Recover automatically.
	C000	Run during initialization.	Recover automatically.

125□□□□ (Duplex CPU Systems only)

A

	Value (hex)	When an operation switching error occurs in the Active CPU Unit, the Standby CPU Unit will become the Active CPU Unit and start operating
A	0000	Operation does not start.
	2000	Operation starts (See note 1.)

Note 1. This setting is enabled when the operation during duplex initialization setting is enabled.

2. Do not set this setting to any value other than those indicated above.

127□□□□ (Duplex CPU Systems only)

A

	Value (hex)	Standby CPU Unit RS-232C Port Setting
A	0000	Disable use of RS-232C port on standby CPU Unit.
	5AA5	Enable use of RS-232C port on standby CPU Unit.

128□□□□

A

	Value (hex)	Low Battery Voltage Detection	Interrupt Task Error Detection
A	C000	Do not detect	Do not detect
	8000	Do not detect	Detect
	4000	Detect	Do not detect
	0000	Detect	Detect

Note Interrupt task errors are detected only for Single CPU Systems.

129□□□□

A

	Value (hex)	FAL Error Log Registration
A	8000	Don't store user-defined FAL error in error log.
	0000	Store user-defined FAL error in error log.

130□□□□

Not

A

	Value (hex)	Memory Card Duplex Setting
A	0	Disabled.
	8	Enable duplex check for Memory Card.

131□□□□ (Duplex CPU Systems only)

A

	Value (hex)	Enabling Unit Removal without a Programming Device
A	Any value except 5AA5	Disabled.
	5AA5	Enabled.

132□□□□ (Duplex CPU Systems only)

A

B

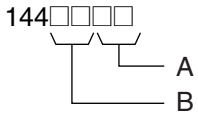
	Value (hex)	Turning ON the Special I/O Unit or CPU Bus Unit Error Flag when Special I/O Unit or CPU Bus Unit Is Removed
A	Any value except AA	Disabled.
	AA	Enabled.

	Value (hex)	Enabling Unit Removal/Addition without Programming Device
B	Any value except AA	Disabled.
	AA	Enabled.

136□□□□

A

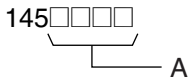
	Value (hex)	EM File Memory Conversion
A	0000	None
	0080	EM File Memory Enabled: Bank No. 0
	0081	EM File Memory Enabled: Bank No. 1
	to	to
	008C	EM File Memory Enabled: Bank No. C



Peripheral Port

	Value (hex)	Data bits	Stop bits	Parity
A	00	7 bits	2 bits	Even
	01	7 bits	2 bits	Odd
	02	7 bits	2 bits	None
	04	7 bits	1 bit	Even
	05	7 bits	1 bit	Odd
	06	7 bits	1 bit	None
	08	8 bits	2 bits	Even
	09	8 bits	2 bits	Odd
	0A	8 bits	2 bits	None
	0C	8 bits	1 bit	Even
	0D	8 bits	1 bit	Odd
	0E	8 bits	1 bit	None

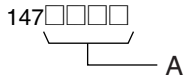
	Value (hex)	Communications mode
B	00	Default (Rightmost 2 digits ignored.)
	80	Host link
	82	NT link
	84	Peripheral bus
	85	Host link



Peripheral Port

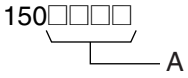
	Value (hex)	Baud rate
A	0000	9,600 bps
	0001	300 bps
	0002	600 bps
	0003	1,200 bps
	0004	2,400 bps
	0005	4,800 bps
	0006	9,600 bps
	0007	19,200 bps
	0008	38,400 bps
	0009	57,600 bps
	000A	115,200 bps

Note Set 0000 to 0009 hex for standard NT Links and 000A hex for high-speed NT Links.



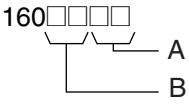
Peripheral Port

	Value (hex)	Host link Unit No.
A	0000	No. 0
	0001	No. 1
	0002	No. 2
	to	to
	001F	No. 31



Peripheral Port

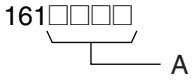
	Value (hex)	NT Link Mode Maximum Unit No.
A	0000	No. 0
	0001	No. 1
	to	to
	0007	No. 7



RS-232C Port

	Value (hex)	Data bits	Stop bits	Parity
A	00	7 bits	2 bits	Even
	01	7 bits	2 bits	Odd
	02	7 bits	2 bits	None
	04	7 bits	1 bit	Even
	05	7 bits	1 bit	Odd
	06	7 bits	1 bit	None
	08	8 bits	2 bits	Even
	09	8 bits	2 bits	Odd
	0A	8 bits	2 bits	None
	0C	8 bits	1 bit	Even
	0D	8 bits	1 bit	Odd
	0E	8 bits	1 bit	None

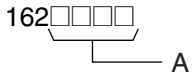
	Value (hex)	Communications mode
B	00	Default (Rightmost 2 digits ignored.)
	80	Host link
	82	NT link
	83	No-protocol
	84	Peripheral bus
	85	Host link



RS-232C Port

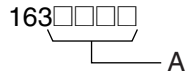
	Value (hex)	Baud rate
A	0000	9,600 bps
	0001	300 bps
	0002	600 bps
	0003	1,200 bps
	0004	2,400 bps
	0005	4,800 bps
	0006	9,600 bps
	0007	19,200 bps
	0008	38,400 bps
	0009	57,600 bps
	000A	115,200 bps

Note Set 0000 to 0009 hex for standard NT Links and 000A hex for high-speed NT Links.



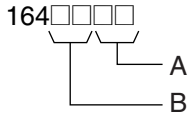
RS-232C Port

	Value (hex)	No-protocol mode delay
A	0000	0 ms
	0001	10 ms
	to	to
	270F	99,990 ms

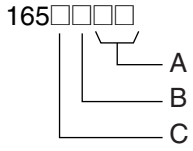


RS-232C Port

	Value (hex)	Host link Unit No.
A	0000	No. 0
	0001	No. 1
	0002	No. 2
	to	to
	001F	No. 31

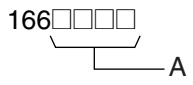


	Value (hex)	No-protocol Mode End Code
A	00	00
	to	to
	FF	FF
	Value (hex)	**No-protocol Mode Start Code**
B	00	00
	to	to
	FF	FF



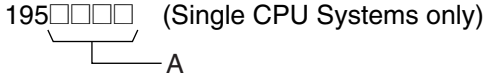
RS-232C Port

	Value (hex)	No-protocol Mode reception data volume
A	00	256
	01	1
	to	to
	FF	256
	Value (hex)	**No-protocol Mode end code setting**
B	0	None (Specify the amount of data being received)
	1	Yes (Specify the end code)
	2	End code is set to CF+LF
	Value (hex)	**No-protocol Mode start code setting**
C	0	None
	1	Yes

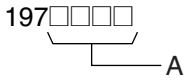


RS-232C Port

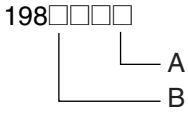
	Value (hex)	Maximum Unit No. in NT Link Mode
A	0000	No. 0
	0001	No. 1
	to	to
	0007	No. 7



	Value (hex)	Scheduled Interrupt Time Unit
A	0000	10 ms
	0001	1.0 ms

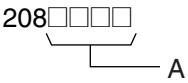


	Value (hex)	Instruction Error Operation
A	0000	Continue operation
	8000	Stop operation

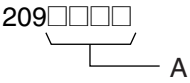


Background Processing Settings (Single CPU Systems Only)

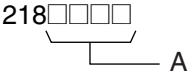
	Value (hex)	Communications Port for Background Processing	
A	0 to 7	Communications port 0 to 7	
	Value (hex)	**Background Processing**	
B	0 to E	Bit 12	No background processing
		Bit 13	ON: Process data shifting instructions in background.
		Bit 14	ON: Process text string instructions in background.
		Bit 15	ON: Process table data instructions in background.



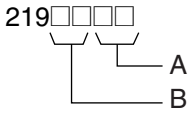
	Value (hex)	Minimum Cycle Time
A	0000	Cycle time not fixed
	0001	Cycle time fixed: 1 ms
	to	to
	7D00	Cycle time fixed: 32,000 ms



	Value (hex)	Watch Cycle Time
A	0000	Default: 1,000 ms (1 s)
	8001	10 ms
	to	to
	8FA0	40,000 ms

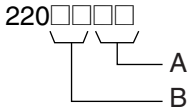


	Value (hex)	Fixed Peripheral Servicing Time
A	0000	Default (4% of the cycle time)
	8000	00 ms
	8001	0.1 ms
	to	to
	80FF	25.5 ms



	Value (hex)	Time Slice Peripheral Servicing Time (See note.)
A	00	Do not use Peripheral Servicing Priority Mode.
	01 to FF	Time Slice Peripheral Servicing Time (0.1 to 25.5 ms in 0.1-ms increments)
	Value (hex)	**Time Slice Instruction Execution Time (See note.)**
B	00	Do not use Peripheral Servicing Priority Mode.
	05 to FF	Time Slice Instruction Execution Time (5 to 255 ms in 1-ms increments)
	Value (hex)	**Parallel Processing Mode (See note.)**
	00	Do not use Parallel Processing Mode.
	01	Synchronous memory access
	02	Asynchronous memory access

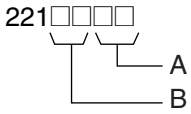
Note Single CPU Systems only.



Special Peripheral Servicing Unit Numbers (See note.)

	Value (hex)	Special Peripheral Servicing Unit Number
A	00	No special servicing
	10 to 1F	CPU Bus Units 0 to 15 (unit number + 10 hex)
	20 to 7F	Special I/O Units 0 to 95 (unit number + 20 hex)
	FC	RS-232C port
	FD	Peripheral port
	Value (hex)	**Special Peripheral Servicing Unit Number**
B	00	No special servicing
	10 to 1F	CPU Bus Units 0 to 15 (unit number + 10 hex)
	20 to 7F	Special I/O Units 0 to 95 (unit number + 20 hex)
	FC	RS-232C port
	FD	Peripheral port

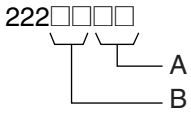
Note Single CPU Systems only.



Special Peripheral Servicing Unit Numbers (See note.)

	Value (hex)	Special Peripheral Servicing Unit Number
A	00	No special servicing
	10 to 1F	CPU Bus Units 0 to 15 (unit number + 10 hex)
	20 to 7F	Special I/O Units 0 to 95 (unit number + 20 hex)
	FC	RS-232C port
	FD	Peripheral port
	Value (hex)	**Special Peripheral Servicing Unit Number**
B	00	No special servicing
	10 to 1F	CPU Bus Units 0 to 15 (unit number + 10 hex)
	20 to 7F	Special I/O Units 0 to 95 (unit number + 20 hex)
	FC	RS-232C port
	FD	Peripheral port

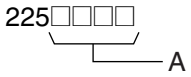
Note Single CPU Systems only.



Special Peripheral Servicing Unit Numbers (See note.)

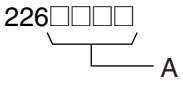
A	Note used.	
	Value (hex)	**Special Peripheral Servicing Unit Number**
B	00	No special servicing
	10 to 1F	CPU Bus Units 0 to 15 (unit number + 10 hex)
	20 to 7F	Special I/O Units 0 to 95 (unit number + 20 hex)
	FC	RS-232C port
	FD	Peripheral port

Note Single CPU Systems only.



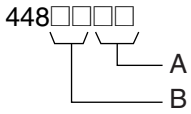
	Value (hex)	Power-OFF Interrupt Task	Power OFF Detection Delay Time
A	0000	Disabled	0 ms
	0001		1 ms
	to		to
	000A		10 ms
	8000	Enabled	0 ms
	8001		1 ms
	to		to
	800A		10 ms

Note Single CPU Systems only.



	Value (hex)	Special I/O Unit Cyclic Refreshing 0: Yes 1: No															
		Unit number															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	0003	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
	0004	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	0005	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
	to																
	FFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

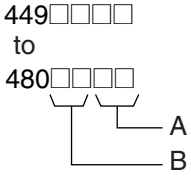
Addresses 227 through 231 are the same as 226.



Use FINS Write Protection and Number of Node Excluded from Write Protection

	Value (hex)	Number of Nodes Excluded from Write Protection
A	00	Set the number of nodes excluded from write protection in Programming Console addresses 448 to 480. 00 to 20 hex (0 to 32 nodes)
	to	
	20	
	Value (hex)	**Use FINS Write Protection**
B	80	Write protection enabled
	00	Write protection disabled

Note Single CPU Systems only.



Nodes Excluded from Write Protection (Protection Releasing Addresses, 32 Nodes Maximum)

	Value (hex)	FINS Source Node Address
A	01	Node address of a node to be excluded from write protection.
	to	
	FE	
	FF	All nodes in specified network.
	Value (hex)	**FINS Source Network Address**
B	00	Network address of the node to be excluded from write protection.
	to	
	7F	

Note Single CPU Systems only.

Appendix E
Precautions in Replacing CS1-H PLCs with CS1D PLCs

Observe the following precautions when replacing a CS1-H system (see note) with a CS1D system, and make sure the new system is suitable for the application conditions.

Note The information in the following table is based on CS1-H CPU Unit Ver. 4.1. Refer to the *CS Series PLC Operation Manual* (W339) for differences between unit versions.

Item		Duplex CPU Systems	Single CPU Systems	CS1-H (See note.)
Units	CPU Unit	CPU Units for Duplex CPU Systems required. CS1D-CPU□□H When using FB/ST/SFC, use the CS1D-CPU□□HA.	CPU Units for Single CPU Systems required. CS1D-CPU□□S When using FB/ST/SFC, use the CS1D-CPU□□SA.	CS1-H CPU Units required. CS1G/H-CPU□□H
	Power Supply Unit	CS1D Power Supply Units required. CS1D-PA/PD□□□□	CS1D Power Supply Units required. CS1D-PA/PD□□□□	C200HW Power Supply Units required. C200HW-PA/PD□□□□
	CPU Backplane	CPU Backplanes for Duplex CPU Systems required. • Duplex CPU, Dual I/O Expansion Systems: CS1D-042D • Duplex CPU, Single I/O Expansion Systems: CS1D-BC052	CPU Backplanes for Duplex CPU Systems required. CS1D-BC082S	CS1W CPU Backplanes required. CS1W-BC□□3 CS1W-BC□□2
	Expansion Backplane	CS1D Expansion Backplane required. • Duplex CPU, Dual I/O Expansion Systems: CS1D-BI082D • Duplex CPU, Single I/O Expansion Systems: CS1D-BI092	CS1D Expansion Backplane required. CS1D-BI092	CS1D or C200H Expansion Backplane required. CS1W-BI□□3 CS1W-BI□□2 C200HW-BI□□1(-V1)

Item		Duplex CPU Systems	Single CPU Systems	CS1-H (See note.)
Performance	System overhead time	1.9 ms	0.5 ms (normal mode) 0.4 ms (Parallel Processing Mode)	0.3 ms (normal mode on CS1-H) 0.2 ms (Parallel Processing Mode on the CS1-H) 0.5 ms (CS1)
	Instruction Execution Times	Refer to *9-5 Instruction Execution Times and Number of Steps*.	Refer to *9-5 Instruction Execution Times and Number of Steps*.	---
	Increase in cycle time for duplex initialization	The cycle time will be increased for any cycle in which duplex initialization is required. Refer to *SECTION 9 CPU Unit Operation and the Cycle Time* for details. Set the maximum cycle time in consideration of this increase.	--- (There is no need to consider the time required for duplex initialization.)	---
	Increase in cycle time for online editing	Approximately 8 ms, but duplex initialization is required after online editing (see above).	Approx. 8 ms (No precautions in converting from the CS1-H.)	CS1-H CPU Units: Approx. 8 ms (CHU6□)
	CPU execution modes	Only the normal execution mode is supported.	No precautions in converting from the CS1-H.	The CS1-H also supports Parallel Processing and Peripheral Servicing Priority Modes.

Item		Duplex CPU Systems	Single CPU Systems	CS1-H (See note.)
I/O processing	Number of slots for 1 CPU Rack and 7 Expansion Racks	• Duplex CPU, Dual I/O Expansion Systems: 52 slots with duplexed Connecting Cables (3 on CPU Rack and 7 each on Expansion Racks) or 60 slots with single Connecting Cable (4 on CPU Rack and 8 each on Expansion Racks) • Duplex CPU, Single I/O Expansion Systems: 68 slots, 5 on CPU Rack and 9 each on Expansion Racks	71 slots, 8 on CPU Rack and 9 each on Expansion Racks	80 slots, 10 on CPU Rack and 10 each on Expansion Racks
	I/O refresh methods	Immediate refreshing (with !) is not supported. Use IORF as required for special refreshing.	No precautions in converting from the CS1-H.	Immediate refreshing (with !), IORF refreshing, and cyclic refreshing are supported.
	First word settings	First words on Racks can be set. First words for slots cannot be set.	No precautions in converting from the CS1-H.	First words on Racks can be set. First words for slots can be set for up to 64 slots.
	Inner Board restrictions	Duplex Inner Boards cannot be mounted and can be used only by using a Process-control CPU Unit, which has a built-in CS1D-LCB05D Inner Board.	No precautions in converting from the CS1-H.	CS-series Inner Boards can be mounted.
	C200H Units	C200H Units cannot be mounted.	C200H Units cannot be mounted.	C200H Units can be mounted.
	Interrupt Input Units	Interrupt Input Units can be used only as standard Input Units.	Interrupt Input Units can be used for interrupt inputs. (Only CS-series Input Interrupt Units can be used.)	Interrupt Input Units can be used for interrupt inputs.
	Long-distance Expansion Racks, mounting location of CS1W-IC102	The CS1W-IC102 must be mounted to the CPU Rack. Normal operation will not be possible if it is mounted to an Expansion Rack. The CS1W-IC102 cannot be used in a Duplex CPU, Dual I/O Expansion System.	The CS1W-IC102 must be mounted to the CPU Rack. Normal operation will not be possible if it is mounted to an Expansion Rack.	The CS1W-IC102 can be mounted to the CPU Rack or to the first Expansion Rack (Rack number 1).
	SYSMAC BUS	Not supported.	Not supported.	Supported.
	Connections on CS1 bus interface	Connection not supported and will result in I/O bus error.	Connection not supported and will result in I/O bus error.	Connection supported with one of the following cables: ITNC-EIS02-CST ITNC-EIX02-CST ITBC-CST01
Instructions and tasks	- Interrupt control instruction - Background execution of text string processing instructions, table data instructions, and some data shift instructions	Interrupt control instructions MSKS, MSKR, and CKI cannot be used. Instructions to disable and enable peripheral servicing (IOSP and IORS) cannot be used. Background processing of text string, data shifting, and table data instructions is not supported.	No precautions in converting from the CS1-H.	Supported.

Item		Duplex CPU Systems	Single CPU Systems	CS1-H (See note.)
Instructions and tasks, contd	ER Flag operation	The ER Flag will turn ON if the active and standby CPU Units cannot be synchronized for instructions requiring synchronization, including IORF, DLNK, IORD, IOWR, RXD, FREAD, FWRIT, and TWRIT. This does not apply to PID. Write the program to re-execute these instructions if the ER Flag goes ON.	(No precautions in converting from the CS1-H.)	---
	Tasks	Interrupt tasks are not supported, but they can be used as cyclic tasks.	No precautions in converting from the CS1-H.	Interrupt tasks are supported.
	Interrupts	I/O interrupts, scheduled interrupts, power OFF interrupts, and interrupts from Inner Boards are not supported.	No precautions in converting from the CS1-H.	I/O interrupts, scheduled interrupts, power OFF interrupts, and interrupts from Inner Boards are supported.
	Automatic allocation of communications ports	Supported in CPU Units with unit version 1.3 or later.	No precautions in converting from the CS1-H.	Supported.
	Using IORD/IOWR for CPU Bus Units	Not supported. (Can be used only for Special I/O Units.)	No precautions in converting from the CS1-H.	Supported.
	Downloading tasks individually	Not supported. (The entire program must be downloaded.)	No precautions in converting from the CS1-H.	Supported, but only in PROGRAM mode.
	Function blocks	Supported by the CS1D-CPU□□HA.	Supported by the CS1D-CPU□□HS.	Supported.
	Function Block (FB) Function - Online editing - Support for in-out variable (array specification is possible for in-out variable) - STRING data (type) and string processing function is supported in Structured Text	Supported by the CS1D-CPU□□HA.	Supported by the CS1D-CPU□□SA.	Supported.
	Structured Text can be used in a task program	Supported by the CS1D-CPU□□HA.	Supported by the CS1D-CPU□□SA.	Supported
	SFC language can be used in a task program	Supported by the CS1D-CPU□□HA.	Supported by the CS1D-CPU□□SA.	Supported
	Multi-interlock instructions: MILH, MILR, and MILC	Not supported.	No precautions in converting from the CS1-H.	Supported.
	Time comparison instructions: =DT, <>DT, <DT, <=DT, >DT, and >=DT	Not supported.	No precautions in converting from the CS1-H.	Supported.

Item		Duplex CPU Systems	Single CPU Systems	CS1-H (See note.)
Instructions and tasks, contd	Expansion data comparison instruction: BCMP2	Not supported.	No precautions in converting from the CS1-H.	Supported.
	Gray scale conversion instruction: GRY	Not supported.	Supported. (No precautions in converting from the CS1-H.)	Supported.
	Time-proportional output instruction: TPO	Not supported.	Supported. (No precautions in converting from the CS1-H.)	Supported.
	Convenient instructions: DSW, TKY, HKY, MTR, and 7SEG	Not supported.	Supported. (No precautions in converting from the CS1-H.)	Supported.
	Explicit message instructions: EXPLT, EGATR, ESATR, ECHRD, and ECHWR	Not supported.	Supported. (No precautions in converting from the CS1-H.)	Supported.
	TXD, RXDinstruction Serial communications board specification	Not supported.	Supported by the CS1D-CPU□□SA.	Supported.
	TXDU and RXDU instructions	Not supported.	Supported by the CS1D-CPU□□SA.	Supported.
	Model conversion instructions: XFERC, DISTC, COLLC, MOVBC, and BCNT	Not supported.	Not supported.	Supported.
	Special function block instruction: GETID	Supported by the CS1D-CPU□□HA.	Supported by the CS1D-CPU□□SA.	Supported.
	Numerical value → ASCII conversion instruction, ASCII → numerical value conversion instruction (NUM4, NUM8, NUM16, STR4, STR8, STR16)	Supported by the CS1D-CPU□□HA.	Supported by the CS1D-CPU□□SA.	Supported.
	Text file write instruction (TWRIT)	Supported by the CS1D-CPU□□HA.	Supported by the CS1D-CPU□□SA.	Supported.
PLC Setup		If CS1 or CS1-H PLC Setups are used, the CS1D will change any setting that it does not support (e.g., interrupt settings for the CPU Unit, CPU execution modes for peripheral servicing, etc.)	All settings in the PLC Setup for the CS1-H can be used. (No precautions in converting from the CS1-H.)	---

Item		Duplex CPU Systems	Single CPU Systems	CS1-H (See note.)
Programming Devices	CX-Programmer restrictions	Supported from CX-Programmer version 3.1. Supported from CX-Programmer version 2.1 or lower with the following restrictions. Version 2.1: Duplex error displays, PLC Setup settings, and online Unit replacement are not supported. Version 3.0: Online Unit replacement are not supported. Supported from CX-Programmer Ver. 9.7.	Supported from CX-Programmer version 4.0. CX-Programmer Version 3.□ or lower cannot be used.	Supported from CX-Programmer version 2.1.
	Device type setting	CX-Programmer Version 3.□ or Lower Select "CS1H-H" as the device type. When using duplex functions, select ***Duplex Settings*** from the Option Menu in the PLC Setup. Duplex operation must be set in the PLC Setup. CX-Programmer Version 4.0 or Higher Select "CS1D-H" as the device type when using a Duplex CPU System. The "CS1H-H" can also be selected as the device type, but if it is, then ***Duplex Settings*** must be selected from the Option Menu in the PLC Setup. Duplex operation must be set in the PLC Setup. CS1D-CPU□□HA does not support an online connection even if "CS1H-H" is selected.	Select "CS1D-S" as the device type. Online connection will not be possible if "CS1D-H" is selected. Duplex operation must be set in the PLC Setup.	Select "CS1H-H" as the device type.
	Connecting to PLC	The Programming Device must be connected to the active CPU Unit; it will not be possible to transfer data or otherwise write data when connected to the standby CPU Unit.	---	---

Item		Duplex CPU Systems	Single CPU Systems	CS1-H (See note.)
Serial communications settings	Built-in RS-232C port	A DIP switch pin on the Duplex Unit is used to switch between automatic detection and PLC Setup settings.	No precautions in converting from the CS1-H.	A DIP switch pin on the CPU Unit is used to switch between automatic detection and PLC Setup settings.
	Peripheral port	Same as above.	Same as above.	Same as above.
	SPMA function of NS-series PTs	Not supported.	No precautions in converting from the CS1-H.	Supported.
	Serial gateway function (Conversion of FINS to CompoWay/F at built-in serial port)	Not supported.	Not supported.	Supported.
	Network levels	Communications supported across up to 3 network levels. Communications will not reach 4th level.	No precautions in converting from the CS1-H.	Communications supported across up to 8 network levels.
	Online connection via networks without I/O tables	Not supported. (I/O tables must be created before online connection via networks is possible.)	No precautions in converting from the CS1-H.	Supported.
Protection	Read protection for individual tasks	Not supported. (Read protection is supported for user memory.)	No precautions in converting from the CS1-H.	Supported. Protection against transfers to Memory Cards also supported.
	FINS write protection	Not supported.	No precautions in converting from the CS1-H.	Supported. Writing across networks can be prohibited for specific nodes.

Item		Duplex CPU Systems	Single CPU Systems	CS1-H (See note.)
File memory operations	Automatic transfer at startup	Must be performed on the active CPU Unit. The results will be automatically transferred to the standby CPU Unit.	No precautions in converting from the CS1-H.	---
	Files required for automatic transfer at startup	Both program file (.obj) and parameter file (.std) must be transferred.	No precautions in converting from the CS1-H.	Transfer is possible for only program file (.obj).
	File memory read/ write instructions	File memory instructions for EM file memory will be executed on both the standby and active CPU Units. File memory instructions for Memory Cards will be executed only for the active CPU Unit. If Memory Card duplex operation is enabled in the PLC Setup, however, write operations will be executed for both the active and standby CPU Units.	No precautions in converting from the CS1-H.	---
	Simple backup operation	Simple backup operations are executed for the Memory Card in the active CPU Unit. There is no need to place a Memory Card in the standby CPU Unit.	No precautions in converting from the CS1-H.	---
	User program overwrite during operation			
	EM file memory settings	Depends on PLC Setup settings. (The specified portion of the EM Areas will be converted to file memory on both the standby and active CPU Units.)	No precautions in converting from the CS1-H.	Depends on PLC Setup settings.
User-customizable switch		The “A39512” switch on the Duplex Unit is used.	No precautions in converting from the CS1-H.	Pin 6 on CPU Unit DIP switch is used.

Appendix F
Connecting to the RS-232C Port on the CPU Unit

Connection Examples

The wiring diagrams for connecting to the RS-232C port are provided in this appendix. In actual wiring, we recommend the use of shielded twisted-pair cables and other methods to improve noise resistance. Refer to *Recommended Wiring Methods* later in this appendix for recommended wiring methods.

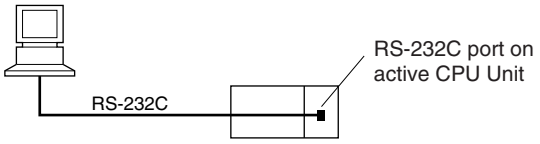
Refer to *Appendix G CJ1W-CIF11 RS-422A Converter* for information on the CJ1W-CIF11 RS-422A Converter.

Connections to Host Computers

Note Connections to a computer running the CX-Programmer are the same as those shown here.

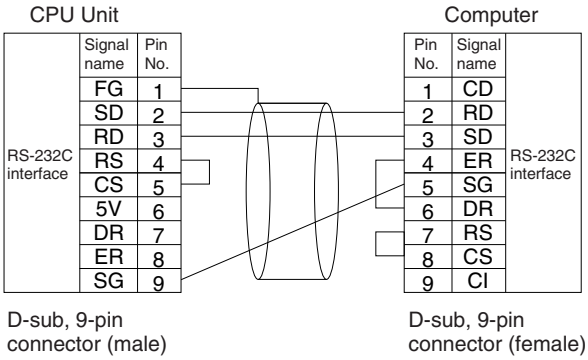
1:1 Connections via RS-232C Port

Connecting to One CPU Unit

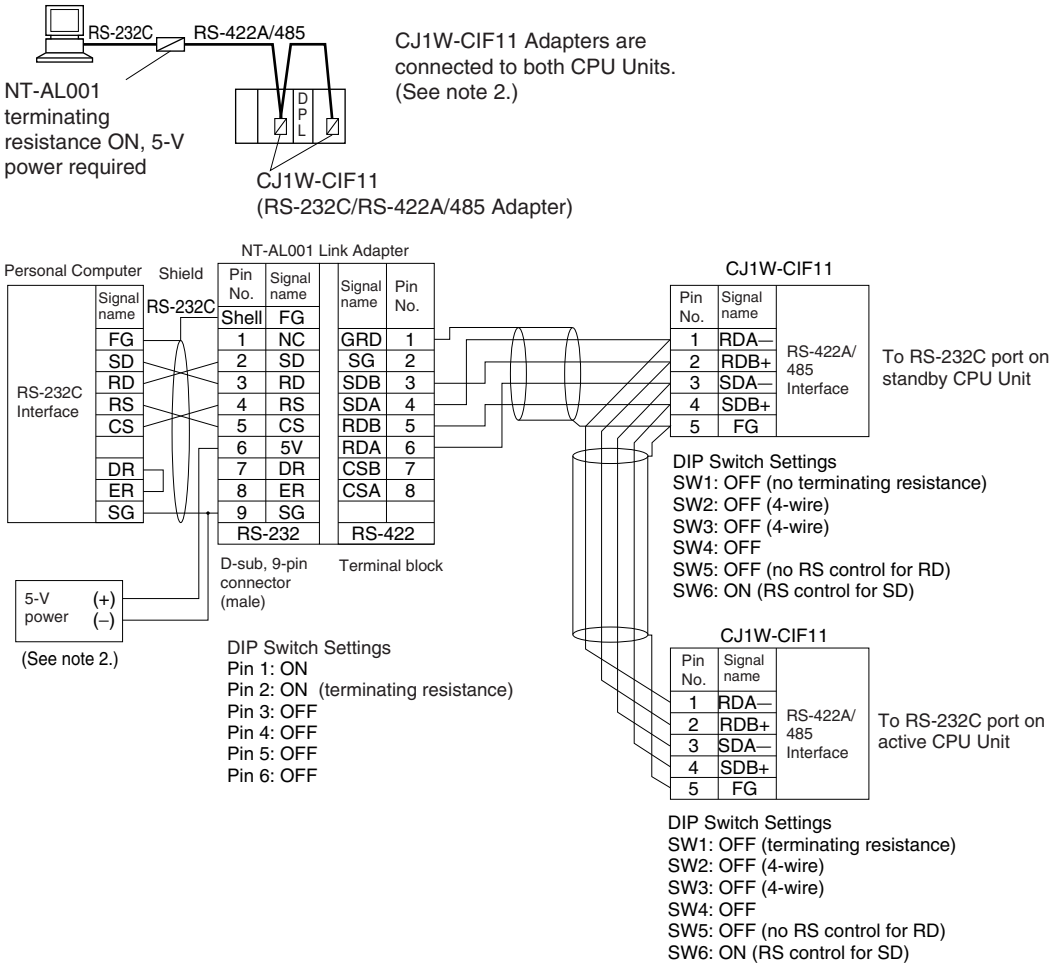


1. The maximum cable length for an RS-232C connection is 15 m. RS-232C communications specifications, however, do not cover transmissions at 19.2 Kbps. Refer to documentation of the device being connected when using this baud rate.
2. With a Duplex CPU System, connect to the active CPU Unit. If the method shown in this connection example is used, however, communications will be disrupted when the active CPU Unit switches.

- IBM PC/AT or Compatible Computer



Duplex Connections to Standby and Active CPU Units for Continuous Communications when Switching to Simplex Operation with Duplex CPU Systems

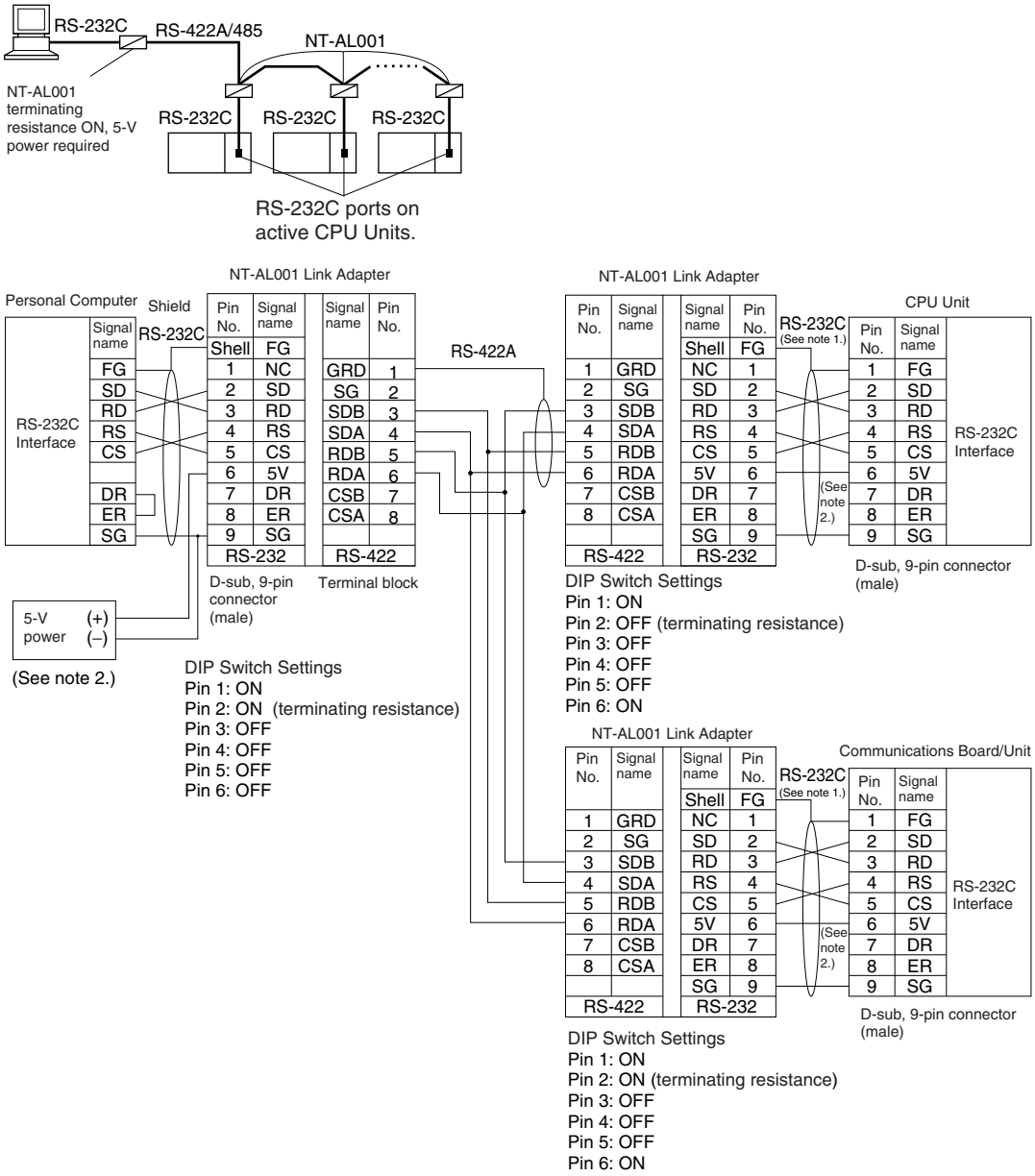


Note 1. When the NT-AL001 Link Adapter is connected to the RS-232C port on the CPU Unit, 5 V is supplied from pin 6, eliminating the need for a 5-V power supply.

2. The CJ1W-CIF11 does not provide isolation. The total length of the transmission path must therefore be 50 m or less. If the transmission distance is greater than 50 m, use the NT-AL001, which provides isolation, and do not include the CJ1W-CIF11 in the transmission path. When only the NT-AL001 is used, the total length of the transmission path can be a maximum of 500 m. Also, connect the shield to ground at one end of each cable.

1:N Connections via RS-232C Port

Connecting to One CPU Unit



Note 1. We recommend using the following NT-AL001 Link Adapter Connecting Cables to connect to NT-AL001 Link Adapters.

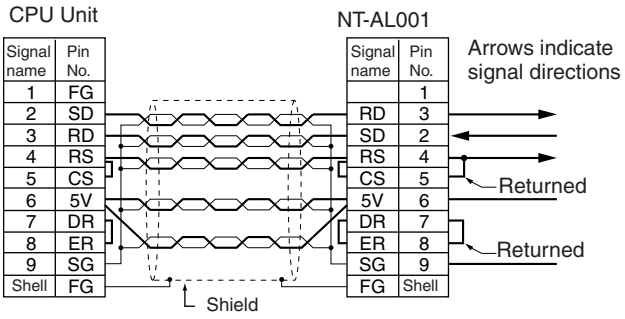
XW2Z-070T-1: 0.7 m
XW2Z-200T-1: 2 m

The recommended cables should be wired as shown below. Each signal wire should be twisted with the SG (signal ground) wire and placed in a shielded cable to prevent the effects of noise in noise-prone environments. The 5-V wires can also be twisted with the SG wire to increase noise immunity.

2. When the NT-AL001 Link Adapter is connected to the RS-232C port on the CPU Unit, 5 V is supplied from pin 6, eliminating the need for a 5-V power supply.

Although this wiring is different from that shown in the example above, it can be used to increase noise immunity if required.

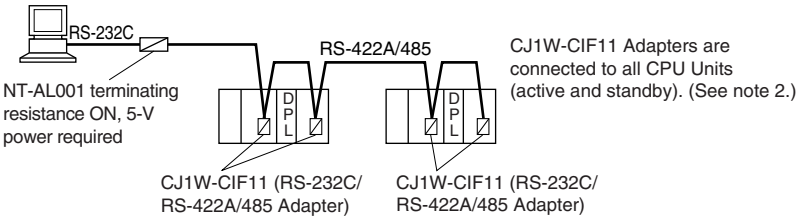
• Wiring with XW2Z-□□0T-1 (10 Conductors)



Note 1. Do not use the 5-V power from pin 6 of the RS-232C port for anything but the NT-AL001/CJ1W-CIF11 Link Adapter, or NV3W-M□20L Programmable Terminal. Using this power supply for any other external device may damage the CPU Unit or the external device

2. The XW1Z-□□0T-1 Cable is designed to connect the NT-AL001 and contains special wiring for the CS and RS signals. Do not use this cable for any other application. Connecting this cable to other devices can damage them.

Duplex Connections to Standby and Active CPU Units for Continuous Communications when Switching to Simplex Operation with Duplex CPU Systems



Actual wiring is the same as 1:1 connections for duplex connects to both CPU Units.

DIP Switch Settings on the NT-AL001 Link Adapter

There is a DIP switch on the NT-AL001 Link Adapter that is used to set RS-422A/485 communications parameters. Set the DIP switch as required for the serial communications mode according to the following table.

Pin	Function	Default setting
1	Not used. (Leave set to ON.)	ON
2	Internal terminating resistance setting. ON: Terminating resistance connected. OFF: Terminating resistance not connected.	ON
3	2-wire/4-wire setting Both pins ON: 2-wire communications Both pins OFF: 4-wire communications	OFF
4		OFF
5	Communications mode (See note.) Both pins OFF: Always send. 5 OFF/6 ON: Send when RS-232C's CS is high. 5 ON/6 OFF: Send when RS-232C's CS is low.	ON
6		OFF

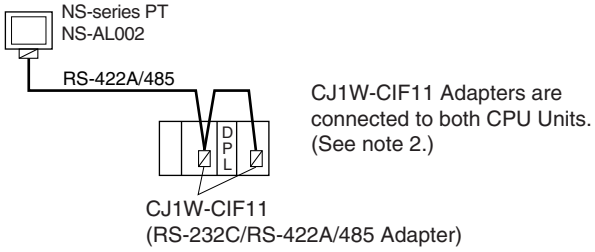
Note 1. Turn OFF pin 5 and turn ON pin 6 when connected to a CS-series CPU Unit.

2. The CJ1W-CIF11 does not provide isolation. The total length of the transmission path must therefore be 50 m or less. If the transmission distance is greater than 50 m, use the NT-AL001, which provides isolation, and do not include the CJ1W-CIF11 in the transmission path. When only the NT-AL001 is used, the total length of the transmission path can be a maximum of 500 m.

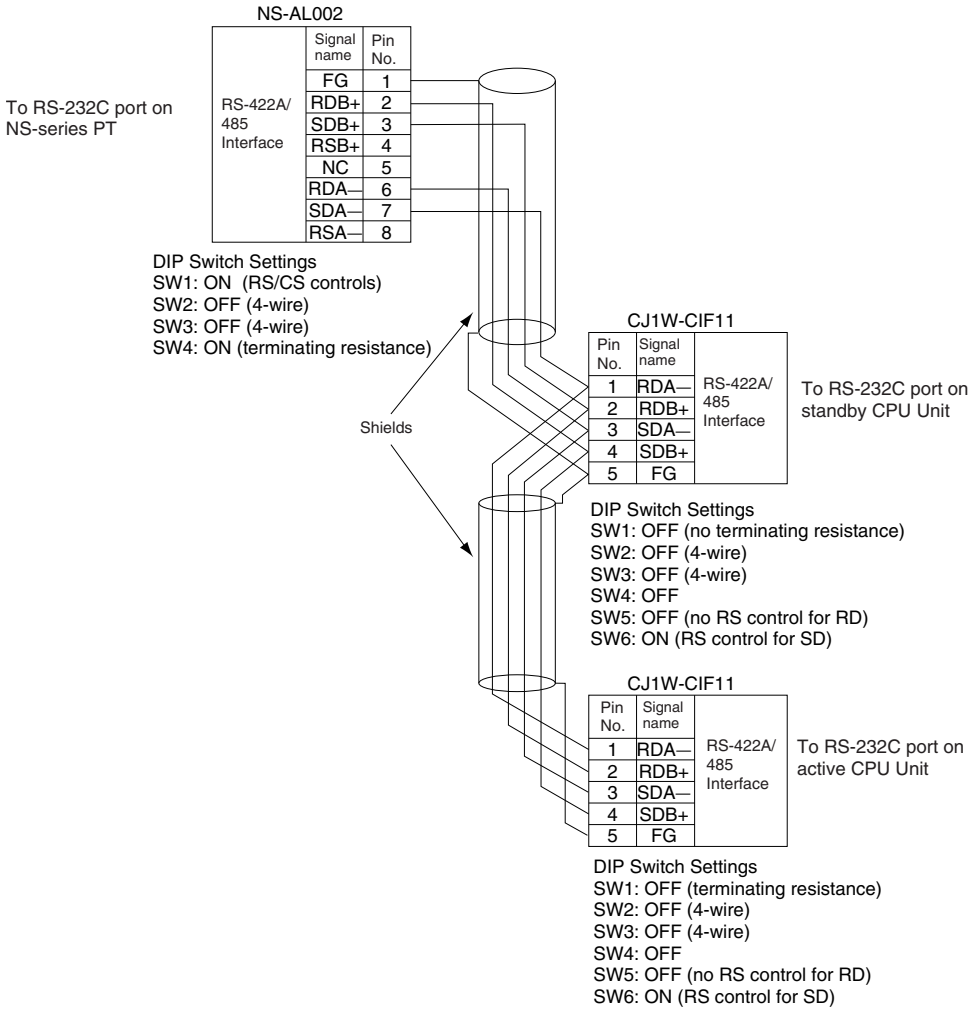
Connection Example to Programmable Terminal (PT)

Direct Connection from RS-232C to RS-232C

Duplex Connections to Standby and Active CPU Units for Continuous Communications when Switching to Simplex Operation



Example for 4-wire Connections



Note 1. The 4-wire connection methods must be used to enable the Programming Console function of the PT.

2. The CJ1W-CIF11 does not provide isolation. The total length of the transmission path must therefore be 50 m or less. If the transmission distance is greater than 50 m, use the NT-AL001, which provides isolation, and do not include the CJ1W-CIF11 in the transmission path. When only the NT-AL001 is used, the total length of the transmission path can be a maximum of 500 m. Also, connect the shield to ground at one end of each cable.

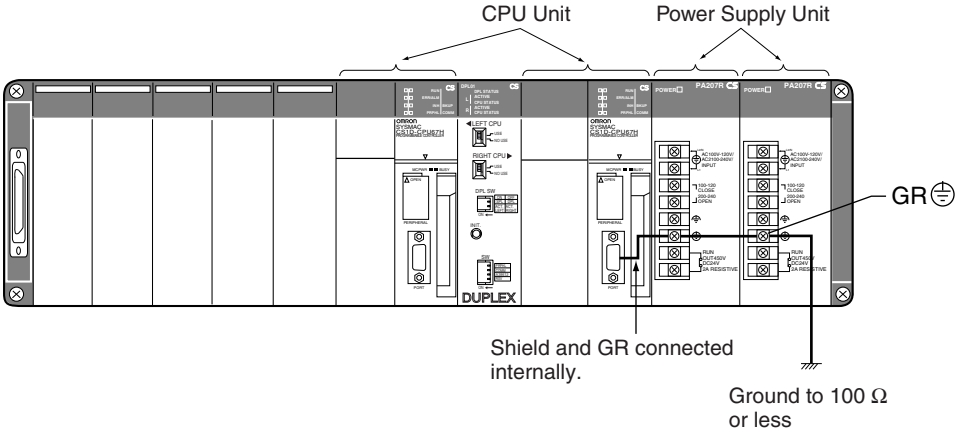
Recommended Wiring Methods

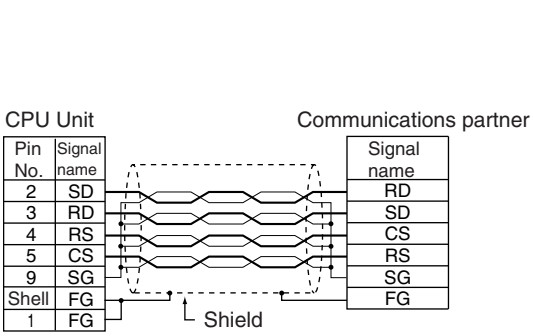
We recommend the following wiring methods for RS-232C, especially in environment prone to noise.

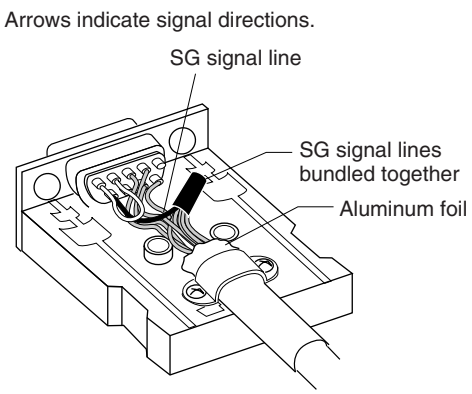
1. Use shielded twisted-pair cable for communications cables. The following RS-232C cables are recommended.

Model	Manufacturer
UL2464 AWG28×5P IFS-RVV-SB (UL approved) AWG28×5P IFVV-SB (not UL approved)	Fujikura Ltd.
UL2464-SB (MA) 5P×28AWG (7/0.127) (UL approved) CO-MA-VV-SB 5P×28AWG (7/0.127) (not UL approved)	Hitachi Cable, Ltd.

2. Use a twisted-pair cable for each signal line and SG (signal ground) to connect the CPU Unit to a communications partner. Also, bundle all the SG lines at the Board/Unit and at the other device and connect them together.
3. Connect the shield line of the communications cable to the hood (FG) of the RS-232C connector at the Board/Unit. Also, ground the protective earth (GR) terminal of the Power Supply Units on the CPU Rack and the Expansion Racks to a resistance of 100 Ω or less. The following example shows connecting SD-SG, RD-SG, RS-SG, and CS-SG for Serial Communications Mode using a twisted-pair cable using the peripheral bus.







Note The hood (FG) is internally connected to the protective earth (GR) terminal on the Power Supply Unit through the CPU Rack or Expansion Rack. FG can thus be connected by connecting the protective earth (GR) terminal on the Power Supply Unit. The hood (FG) is also electrically connected to pin 1 (FG), but the connection resistance between the shield and the FG is smaller for the hood. To reduce contact resistance between the hood (FG) and the FG, connect the shield both to the hood (FG) and to pin 1 (FG).

Wiring Connectors

Use the following procedures to wire connectors.

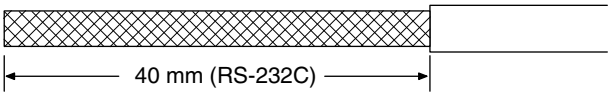
Preparing the Cable

Lengths for steps in the procedure are provided in the diagrams.

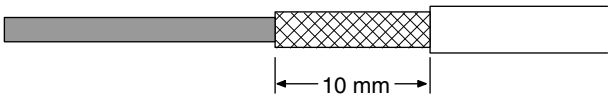
Connecting the Shield Line to the Hood (FG)

1. Cut the cable to the required length, leaving leeway for wiring and laying the cables.

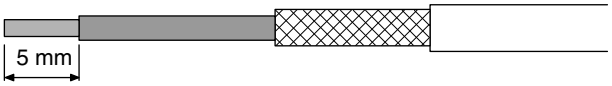
2. Use a razor blade to cut away the sheath, being careful not to damage the braiding.



3. Use scissors to cut away all but 10 mm of the exposed braiding.

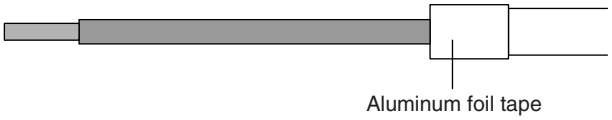


4. Use wire strippers to remove the insulation from the end of each wire.



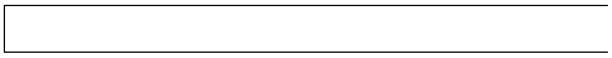
5. Fold the braiding back over the end of the sheath.

6. Wrap aluminum foil tape over the top of the braiding for one and a half turns.

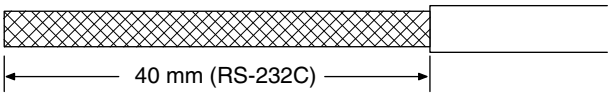


Not Connecting the Shield to the Hood (FG)

1. Cut the cable to the required length, leaving leeway for wiring and laying the cables.



2. Use a razor blade to cut away the sheath, being careful not to damage the braiding.



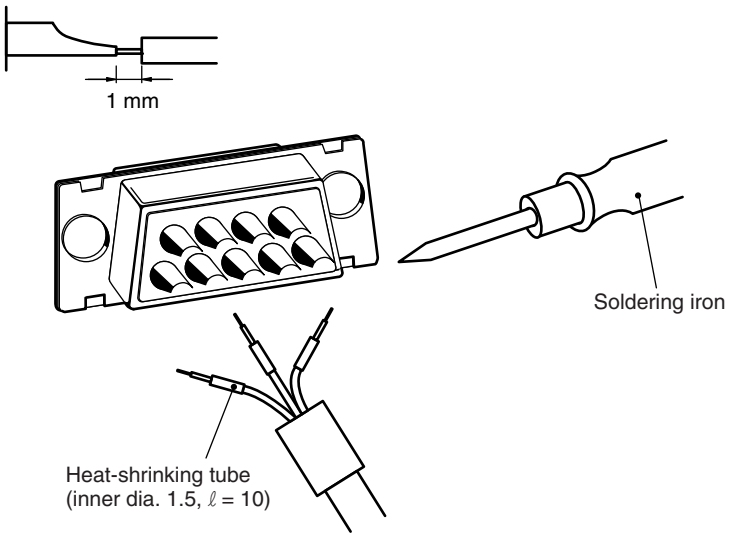
3. Use scissors to cut away the exposed braiding.

4. Use wire strippers to remove the insulation from the end of each wire.

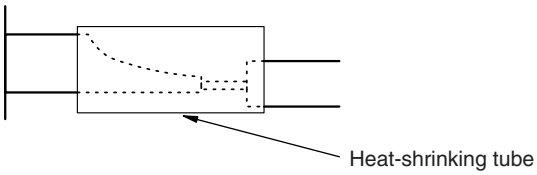
5. Wrap electrician's tape over the top and end of the cut sheath.

Soldering

1. Place heat-shrinking tubes over all wires.
2. Pre-solder all wires and connector terminals.
3. Solder the wires.

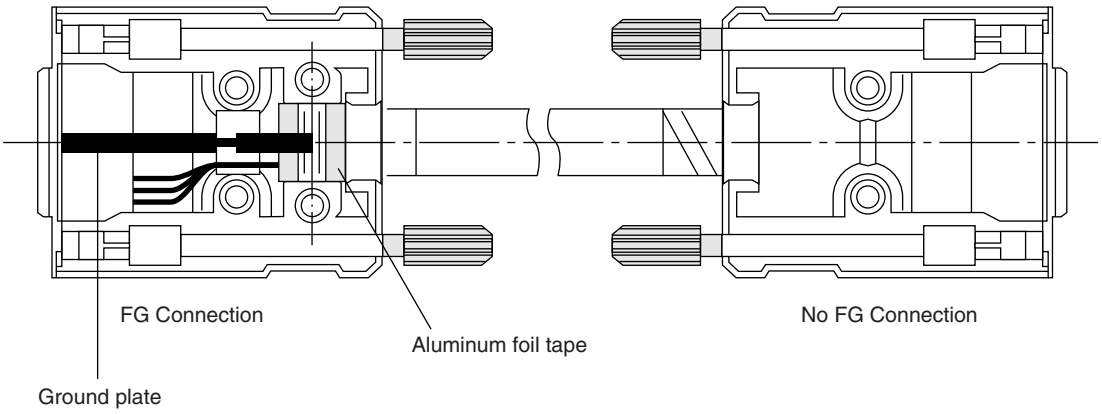


4. Move the heat-shrinking tubes onto the soldered area and shrink them into place.

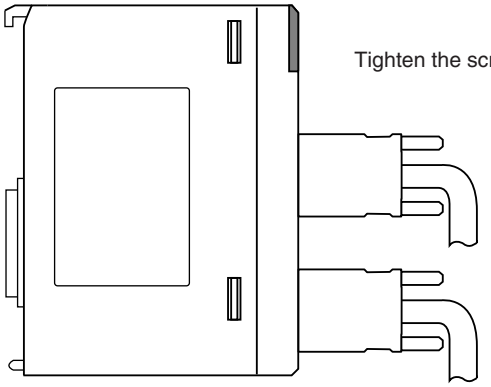


Assembling the Hood

Assemble the connector hood as shown.



Connections to the CPU Unit



- Always turn OFF the power supply to the PLC before connecting or disconnecting communications cables.
- Tighten the communications connector attachment screws to 0.4 N·m.

Appendix G
CJ1W-CIF11 RS-422A Converter

The CJ1W-CIF11 RS-422A Converter converts RS-232C to RS-422A/485.

Specifications

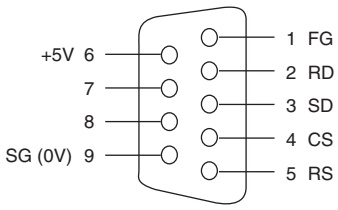
General Specifications

Item	Specifications	
Dimensions	18.2 × 34.0 × 38.8 mm (W × H × D)	
Weight	20 g max.	
Ambient operating temperature	0 to 55°C	
Ambient storage temperature	–29 to 75°C	
Ambient operation humidity	10% to 90% (with no condensation)	
Rated power supply voltage	+5 V	(Supplied from pin 6 of the RS-232C connector.)
Power consumption	40 mA max.	
Atmosphere	Must be free from corrosive gases.	
Vibration resistance	Same as SYSMAC CS/CJ Series.	
Shock resistance	Same as SYSMAC CS/CJ Series.	
Isolation method	Not isolated	
Maximum communications distance	50 m	

Electrical Specifications

RS-232C Connector

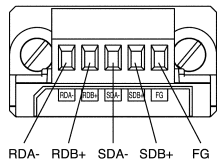
Connector Pin Arrangement for RS-232C Port



Pin No.	Signal name
1	FG
2	RD
3	SD
4	CS
5	RS
6	+5V
7, 8	NC
9	SG (0V)
Food	NC (See note.)

Note The hold will be the same electrical potential as the connector hood on the other end of the cable.

RS-422A/485 Terminal Block



Signal name
RDA–
RDB+
SDA–
SDB+
FG

DIP Switch Settings

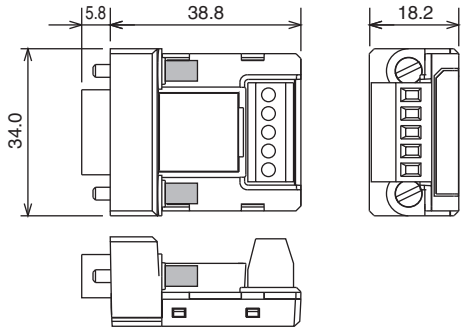
Pin number	Function	ON	OFF
1	Terminating resistance	With (at both ends of the communications path)	Without
2	Two-wire/four-wire method selection (See note 1.)	Two-wire method	Four-wire method
3	Two-wire/four-wire method selection (See note 1.)	Two-wire method	Four-wire method
4	Not used.	---	---
5	Selection of RS control for RD (See note 2.)	With RS control	Without RS control (always ready to receive)
6	Selection of RS control for SD (See note 3.)	With RS control	Without RS control (always ready to send)

Note 1. Set pins 2 and 3 to the same setting (ON for the two-wire method or OFF for the four-wire method).

2. To prohibit echoback, set pin 5 to ON (with RS control).

3. When connecting to several devices using the four-wire method in a 1:N connection, set pin 6 to ON (with RS control). When connecting using the two-wire method, set pin 6 to ON (with RS control).

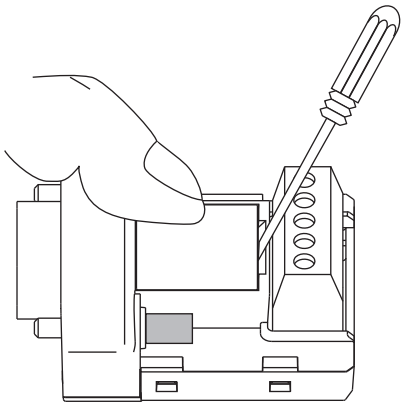
Dimensions



DIP Switch Settings, Wiring, and Installation

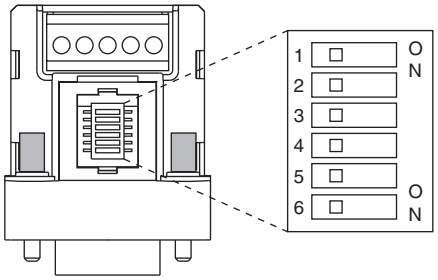
The DIP switch settings must be changed to perform communications according to settings other than the default settings.

1. Remove the DIP switch cover using a flat-bladed screwdriver in the way shown below.



Note Press the cover gently while removing it to prevent it from popping out suddenly.

2. Using a fine pair of tweezers or other tool with a fine point, change the settings of the DIP switch pins to match the desired communications conditions.
3. Be sure to remount the cover after finishing the DIP switch settings.



All the pins are factory-set to OFF.

Wiring the RS-422A/485 Terminal Block

Recommended RS-422A/485 Cable

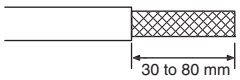
The following cable and wiring methods are recommended to help ensure transmission quality.

Note When using the CJ1W-CIF11, connect all the GR terminals on the PLCs together and ground them at one point to 100 Ω or less.

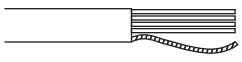
- Use either two-wire or four-wire shielded cable.
  Recommended cable: CO-HC-ESV-3P×7/0.2 (Hirakawa Hewtech)
- Connect the shield wire on the communications cable to the FG terminal on the RS-422A/485 terminal block on the Converter, and ground the ground terminal on the Power Supply Unit of the CPU or Expansion Rack to 100 Ω max.

Wiring Procedure

1. Taking care not to damage the shield, strip between 30 and 80 mm of sheath off the end of the cable.

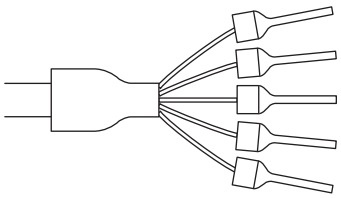


2. Carefully twist the shield mesh together to form a single wire, and carefully cut off the material surrounding the signal wires and any unnecessary signal wires.



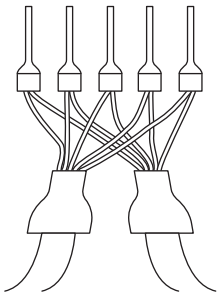
3. Strip the sheath off the signal wires to a length sufficient to attach crimp terminals. Apply vinyl tape or heat-shrinking tube to the sheathes and stripped parts of communications lines.

4. Attach ferrules to ends of the signal lines and crimp them using a crimp tool.
   - Recommended crimp terminals:
     Phoenix Contact
     AI Series
     AI-0.5-8WH-B (serial number: 3201369)
   - Recommended crimp tool:
     Phoenix Contact ZA3

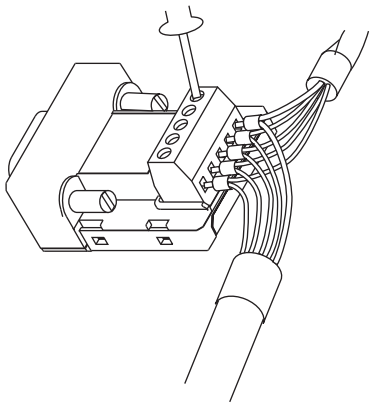


With four-wire cables, insert two signal lines into each crimp terminal together before crimping.

- Recommend crimp terminals:
  Phoenix Contact
  AI Series
  AI-TWIN2×0.5-8WH (serial number: 3200933)
- Recommended crimp tool:
  Phoenix Contact
  UD6 (serial number: 1204436)



5. Connect the signal lines and the shield line to the RS-422A/485 terminal block.

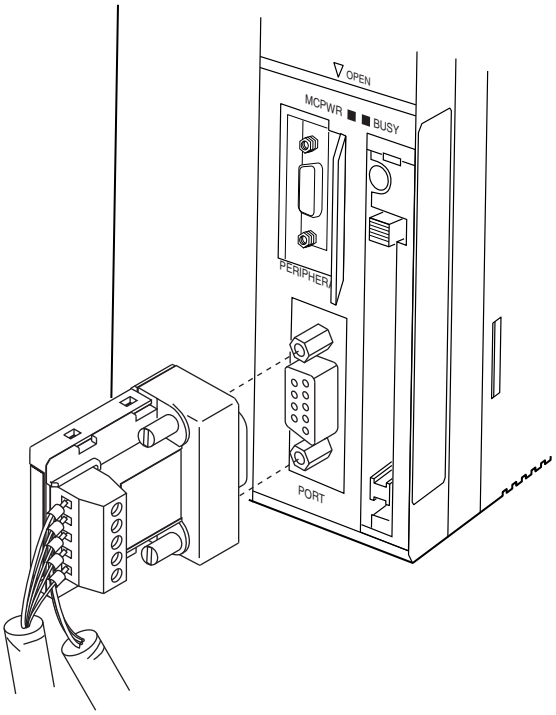


Mounting to the Unit

Mount the Converter to the RS-232C port (D-Sub, 9-pin) of the Unit to be connected in the following way.

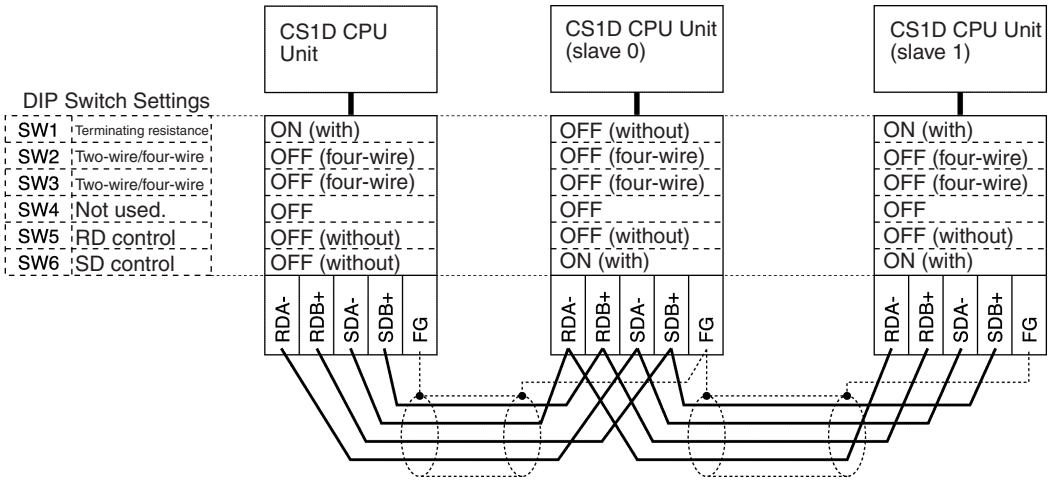
1. Align the Converter's connector with that of the Unit and push it into the Unit's connector as far as possible.
2. Tighten the mounting screws on either side of the Converter. (Tightening torque: 0.3 N·m.)

As an example, connection to a CS1D CPU Unit is shown below.

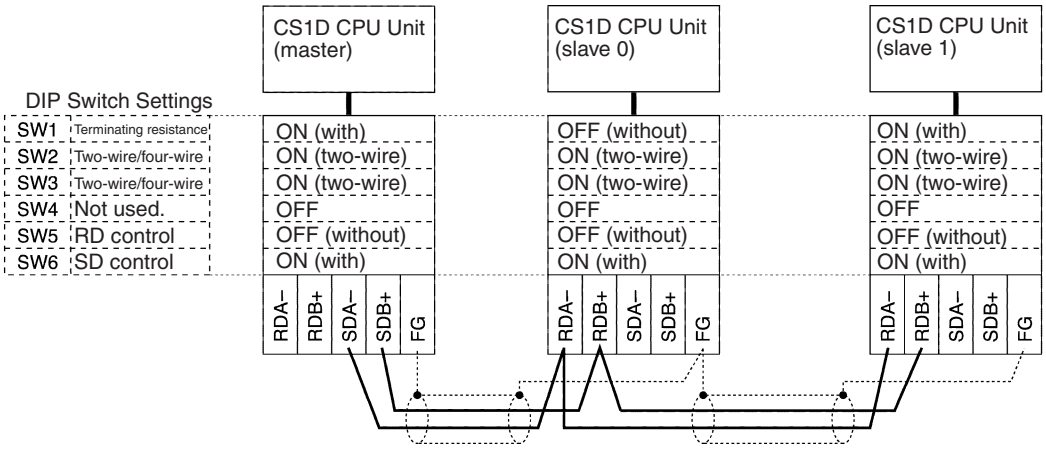


Wiring Examples

Wiring for Four-wire Cable



Wiring for Two-wire Cable



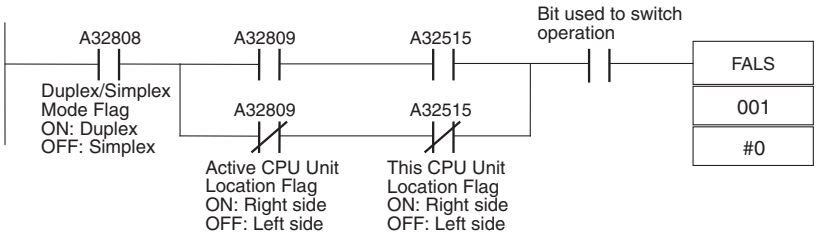
Appendix H
Method of Switching the Operation of a Duplex System by a Program

Intentionally Creating Errors to Switch Operation

With a Duplex CPU System, a hot standby method is used, which means that the standby CPU Unit executes the same program as the active CPU Unit. Thus, if FALS(007) is executed with the same conditions on both the CPU Units, FALS(007) will be executed at the same time in both CPU Units and operation will not switch to the standby, causing the CPU STATUS indicators on the Duplex Unit to flash red for both CPU Units. This is true for other errors causing operation to switch.

To cause the active CPU Unit to switch during debugging operations, either use the USE/NO USE switch on the Duplex Unit or use the following type of programming for FALS(007)

.

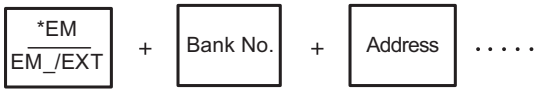


Note If the right and left CPU Units are made to perform different operation, they will not longer be synchronized and a duplex bus error or other error may occur. Do not use the above type of programming with A32515 (This CPU Unit Location Flag) for any other application.

Appendix I
Method of specifing the EM Bank from the Program Console

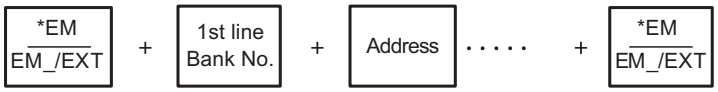
The procedure for specifying the EM Bank from the program console is as follows.

- Specify from EM 0 to 9 (Hex)



- Specify from EM A to F (Hex)

- Specify from EM 10 to 18 (Hex)



* Appears as X on the 2nd line.

In EM Bank 10: X0_12345

In EM Bank 18: X8_67890

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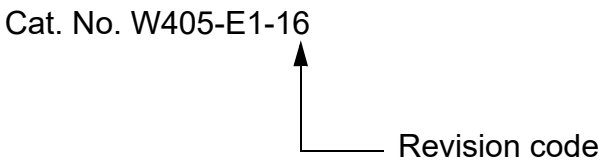
Revision History

A manual revision code appears as a suffix to the catalog number on the front cover of the manual.



The following table outlines the changes made to the manual during each revision. Page numbers refer to the previous version.

Revision code	Date	Revised content
01	September 2002	Original production
02	April 2003	"PC" was globally changed to "PLC" in the sense of Programmable Controller (except for page 299, where "PLC" was changed to "PC" for consistency with device displays). **Page xvii:** Bulleted item added about current consumption when using duplex Power Supply Units. **Page xviii:** Standards for EMS and EMI corrected. **Pages 2, 86, and 94:** Note added about production lot number for CS1D CPU Units. **Pages 5, 48, 61, 62, 126, 374, 381, 428, 438, 440, and 441**: Notes added. **Pages 8, 13, and 25:** Model number and availability information changed in tables for Duplex Inner Board. **Page 15:** Information added on Memory Card restrictions. **Page 21:** Both AC and DC Power OFF detection times included in table. **Page 22:** Change to standards names. **Page 28:** Output capacity for CS1D Power Supply Unit changed. **Page 36:** Indicator status information changed. **Page 38:** Model number and availability information changed for Loop Control Board in lower drawing. **Page 41:** Caution and note on handling DIP switch changed. **Page 46:** Memory Card functions description and table changed. **Page 63:** Note at bottom of page revised and additional information added to the same note about current consumption when using duplex Power Supply Units. Graphic changed in section 2-7-3. **Page 64:** DC input information added below table. **Pages 66 and 67:** Sentence added in top graphic. **Pages 73, 74, 81, and 257:** Reference page numbers and section numbers changed. **Page 74:** Note below table revised. **Page 77:** Additional information added to section 2-11 about current consumption when using duplex Power Supply Units. **Page 86:** Information changed in note. **Page 93:** Value A added to cycle times in bottom table and description added below. **Page 94:** Information changed in note. **Page 106:** Address changed in table from 126 to 127. **Page 125:** Note added and title revised on connecting Long-distance Expansion Racks. **Page 130:** Information on RUN output added to upper note. **Page 132:** Last item on page changed. **Page 133:** Information and graphic added. **Page 146:** Information on duplex Memory Cards added to table. **Page 150:** Notes on Inner Boards eliminated from below two tables. **Page 151:** Information on Memory Card duplex settings added to table. **Page 152:** Information in Inner Board notes below two tables revised. **Page 178:** Information on reserving words the CX-Programmer added. **Page 213:** File memory information changed in table. **Page 218:** Information added on non-fatal Inner Board errors. **Page 237:** Precaution on using auto-incrementing and auto-decrementing added. **Page 254:** "See note." removed from three table cells. **Page 255:** Information on Inner Boards removed from note. **Page 270:** Value A added to cycle times in top table and description added below. Value B added to cycle times in bottom table and description added below. **Page 315:** Item about power supply selector added under "Is voltage selector set correctly?". **Page 319:** Top left box in Program Error Check corrected. **Page 325:** Information on 24 V CD supply voltage added to bottom table. **Page 334:** Introduction to 11-4 changed and not added after table. **Pages 335 and 341:** Information on SYSMAC Link Units added to table. **Page 338:** Restriction added at beginning of 11-4-2. **Page 339:** Parts at beginning of 11-4-3 changed. **Page 357:** Note added in last cell of table. **Page 381:** Input current voltage and graphics changed. **Page 397:** Information on Inner Board non-fatal errors added to table. **Pages 402 to 404:** Address bits revised for words A343 and A355 and information added. **Page 438:** Line added to pin No. 5 in figure. **Page 407:** Descriptions for A39506 and A39507 reversed. **Page 414:** Sentence removed from description of A50014. **Page 428:** Precaution added at top of page. **Page 439:** Sentence added at top of page. **Page 422:** "CJ1W-CIF11" added. **Page 447:** Model number changed in information on Inner Board restrictions. **Page 450:** Appendix added.

Revision code	Date	Revised content
03	June 2003	"CS1D-PA207R Power Supply Unit" was globally changed to "CS1D-PA/PD□□□ Power Supply Unit." **Page 7:** CS1D-PD024 Power Supply Unit information added to table. **Page 22:** CS1D-PD024 Power Supply Unit information added to table. **Page 23:** CS1D-PD024 Power Supply Unit information added as Note number 4. **Pages 24 and 28:** CS1D-PD024 Power Supply Unit information added to CS1D Power Supply Unit table. **Page 64:** CS1D-PD024 Power Supply Unit information added to CS1D Power Supply Unit Model table, and to the Note below it. **Page 65:** CS1D-PA207R title added to dimensions diagram, and new title and dimensions diagram added for CS1D-PD024 Power Supply Unit. **Page 78:** CS1D-PD024 Power Supply Unit information added to table, and note added below it. **Page 129:** "AC Power Supply Models" title added. **Page 131:** New section on "DC Power Supply Models" added. **Page 193:** Terminal diagram changed. **Page 319:** CS1D-PD024 Power Supply Unit information added to table.
04	December 2003	New products added to the manual, including those for Single CPU Systems. (Extensive changes too numerous to list.)
05	July 2005	Revisions were made throughout the manual to add information on the CS1D-PD025 Power Supply Units, CPU Units Ver. 1.2, and add the -V1 suffix to various Unit models, particularly the CS11W-DRM21-V1 DeviceNet Units, including the following changes. **Page v:** Added information on general precautions notation. **Pages x, xi, 16, 28, and 35:** Added information to table. **Page xvii:** Added information on CJ1H Loop-control CPU Units to table. **Page xviii:** Added and changed information in table. Information on warranty and liability also added. **Pages xxiv, xxv, xxvi, and xxvii:** Added precautions. **Pages xxviii and xxix:** Changed EC Directives standard EN50081-2 to 61000-6-4. **Pages 5, 30, 38, 74, and 76:** Added note. **Page 6:** Added and changed information in table. **Pages 7 and 8:** Added reference to CS1D-PD025 to graphic and table. **Pages 9, 10, 29, and 30:** Added information on CS1D Expansion Racks to graphic. **Pages 13 and 43:** Changed information in table. **Pages 24 and 25:** Added column to table for information on CS1D-PD025. **Pages 27, 31, 71, 87, and 376:** Added row to table for information on CS1D-PD025. **Page 33:** Added reference to CS1D-PD025 to table. Note also added to table. **Pages 34, 75, and 76:** Removed reference to "available soon." **Page 44:** Changed references in graphic. **Pages 69, 70, 518, 519, 520, and 521:** Removed the suffix "-E" from NT-AL001-E. **Pages 73 and 150:** Added reference to CS1D-PD025 to graphic. **Page 88:** Added notes on duplexing to top of page. **Pages 89 to 95, 317, 318, 319, and 403:** Changed information in tables to add new models (-V1) and correct other model information. **Page 144:** Added information on bracket for securing expansion cable. **Page 150:** Added information on CS1D-PD025 power consumption. **Page 168:** Changed table and added notes. **Pages 193 and 196:** Added table and notes. **Page 207:** Replaced screen and added information on CX-Programmer Ver. 6.0. **Page 215:** Changed reference from Section 11 to Section 10. **Page 251:** Added information to table and notes. **Pages 355, 371, and 372:** Added information on basic I/O errors to table. **Page 390:** Changed information on battery replacement. **Page 394:** Changed information on online Unit replacement. **Page 407:** Added new subsection with information on online Unit replacement without a Programming Device. **Page 455:** Added information on A09911 to table. **Page 491:** Added information on 009A to table. **Page 500:** Added information on 125□□□□ and 131□□□□. **Pages 509 and 510:** Changed "CS1 Series" to "CS Series" in manual name.
06	December 2006	Corrections and additions were made for CPU Units for Duplex CPU Systems with unit version 1.3 for the addition of Duplex CPU Dual I/O Expansion Systems. Also, information on the following products for Duplex CPU Dual I/O Expansion Systems was added: CS1D-BC042D CPU Backplane, CS1D-DPL02D Duplex Unit, CS1D-IC102D I/O Control Unit, CS1D-BI082D Expansion I/O Backplane, and CS1DII102D I/O Interface Unit.

Revision code	Date	Revised content
07	January 2008	**Page ix:** Added references to notes in middle of table. **Page x:** Changed note 3 and added note 4. **Page xi:** Deleted Note 1 deleted. **Page 7:** Removed “L” from beginning of model number in bottom table. **Page 18:** Added model numbers and unit version in bottom middle cell of table. **Page 28:** Replaced specifications for *Multiple-level communications.* **Page 102:** Added heading inside figure (“96-point Units”). **Pages 151 and 280:** Added note. **Page 275:** Added programming example. **Pages 296 and 528:** Changed slot number ranges for A40400 to A40407. **Pages 405 and 407:** Added interrupt task error to table. **Page 565:** Changed first sentence. **Page 567:** Changed number of slots to 71 at top of page. **Page 583:** Added “(0V)” to signal name.
08	June 2008	**Page 22:** Changed description of specifications for accuracy of timer instructions in Duplex CPU Systems. **Page 28:** Changed description of specifications for control output signals.
09	October 2009	Made corrections for upgraded version of manual.
10	December 2010	**Page viii:** Modified table. **Pages xxvi, 4, 20, 108, 109, 127, 352, and 445:** Added CLK13 and CLK53 to Controller Link Unit model numbers. **Page xxxii:** Added precaution to bottom of page. **Page 130:** Added paragraph below table. **Page 227:** Added note. **Page 245:** Added paragraph to top note. **Page 247:** Added information on restrictions of final rack above section 7-7-2. **Page 313:** Corrected reference section and manual number in middle of page. **Page 399:** Added paragraph to possible remedy for A29512. **Page 403:** Changed possible remedy for A317. **Page 409:** Changed entire flowchart. **Page 413:** Changed contents for A29512 at top of flowchart. **Page 457:** Changed item 3 at top of page and added notes after item 4. **Pages 574 and 575:** Added FG above NC in figure for Link Adapter.
11	October 2015	Added upgraded unit versions of CPU Units and corrected mistakes. • Added CS1D-H/P CPU Units with unit version 1.4. • Added CS1D-S CPU Units with unit version 2.1.
12	September 2016	Changed accessories. Corrected mistakes.
13	December 2018	Revision due to addition of following CPU Units and correction of incorrect descriptions • Added CS1D-CPU□□HA • Added CS1D-CPU□□SA
14	April 2019	Added descriptions and corrected mistakes.
15	August 2022	Revisions for adding safety precautions regarding security.
16	September 2024	Corrected mistakes.

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